Synchronous Rectified Buck MOSFET Driver IC

PX3516

November 22nd - 2012

Published by Infineon Technologies AG

http://www.infineon.com/DCDC

Power Management

Synchronous Rectified Buck MOSFET Driver IC

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Applications:

- Core power regulation for Intel® and AMD® micropocessors server motherboard and notebook market.
- POL power converters for memory, DSP, FPGA, ASIC
- High current DC-DC converters
- Memory

Features:

- Dual MOSFET driver for synchronous rectified bridge converters
- Single 5V supply for both logic and MOSFET gate drive voltages for optimal efficiency
- Fast rise and fall times supports switching rates of up to 2MHz
- Capable of sinking more than 4A peak current for low switching losses
- Shoot through protection
- Three-state PWM input for output stage shutdown
- VCC under-voltage protection
- Lead-free (RoHS compliant) TDSON-10-2 package

Type	Package	Order info
PX3516	PG-TDSON-10-2	PX3516ADDG-R4

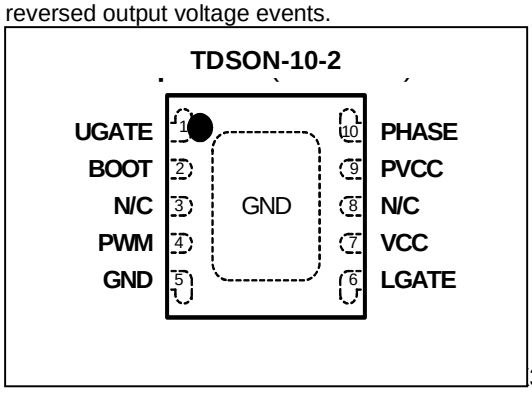
General Description

The PX3516 is a dual high speed driver designed to drive a wide range of high-side and low-side power N-channel MOSFET in synchronous rectified buck converters. When combined with Infineon's Primarion™ Controller Family of Digital Multi-phase Controllers and N-channel MOSFET, the PX3516 forms a complete core-voltage regulator solution for advanced micro and graphics processors as well as point-of-load applications.

The PX3516 provides the capability of driving the high-side gate and low-side gate with a single 5V supply for optimized operation. This 5V supply with suitable decoupling can also be used to provide the supply for the onboard logic. The input voltage for the power stage can range from 5V up to 24V making the driver suitable for Notebook applications.

Shoot-through protection is integrated into the IC which prevents both upper and lower MOSFET from conducting simultaneously and to minimize dead time. The PX3516 has a minimized propagation delay from input to output with fast rise and fall times.

The PX3516 driver also feature a three-state PWM input which, when used together with Infineon's Primarion™ Digital Controllers, eliminates the need for Schottky diodes that are often used in systems to protect the load from reversed output voltage events.



BLOCK DIAGRAM

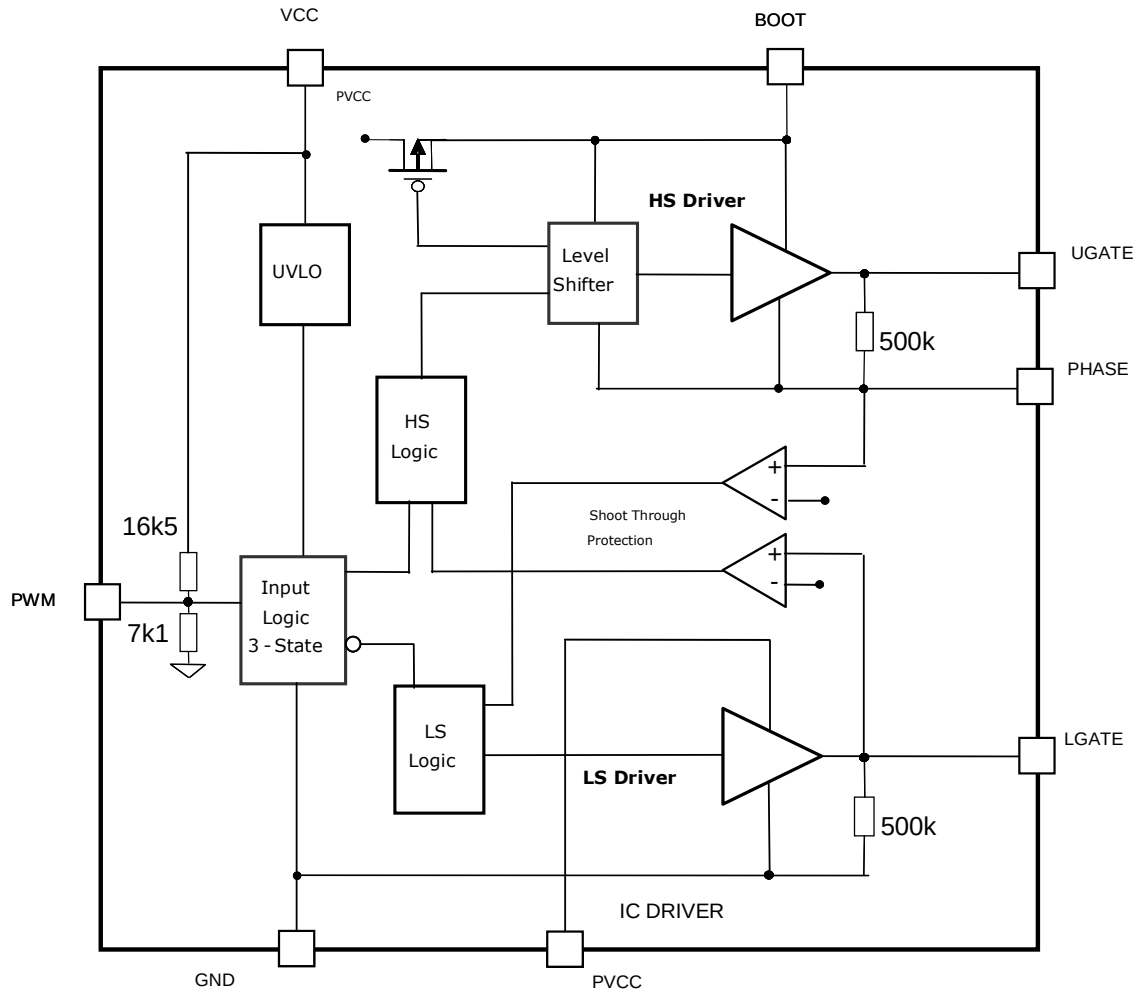


Figure 1 : block diagram of the PX3516

Typical VR12 Multiphase Application

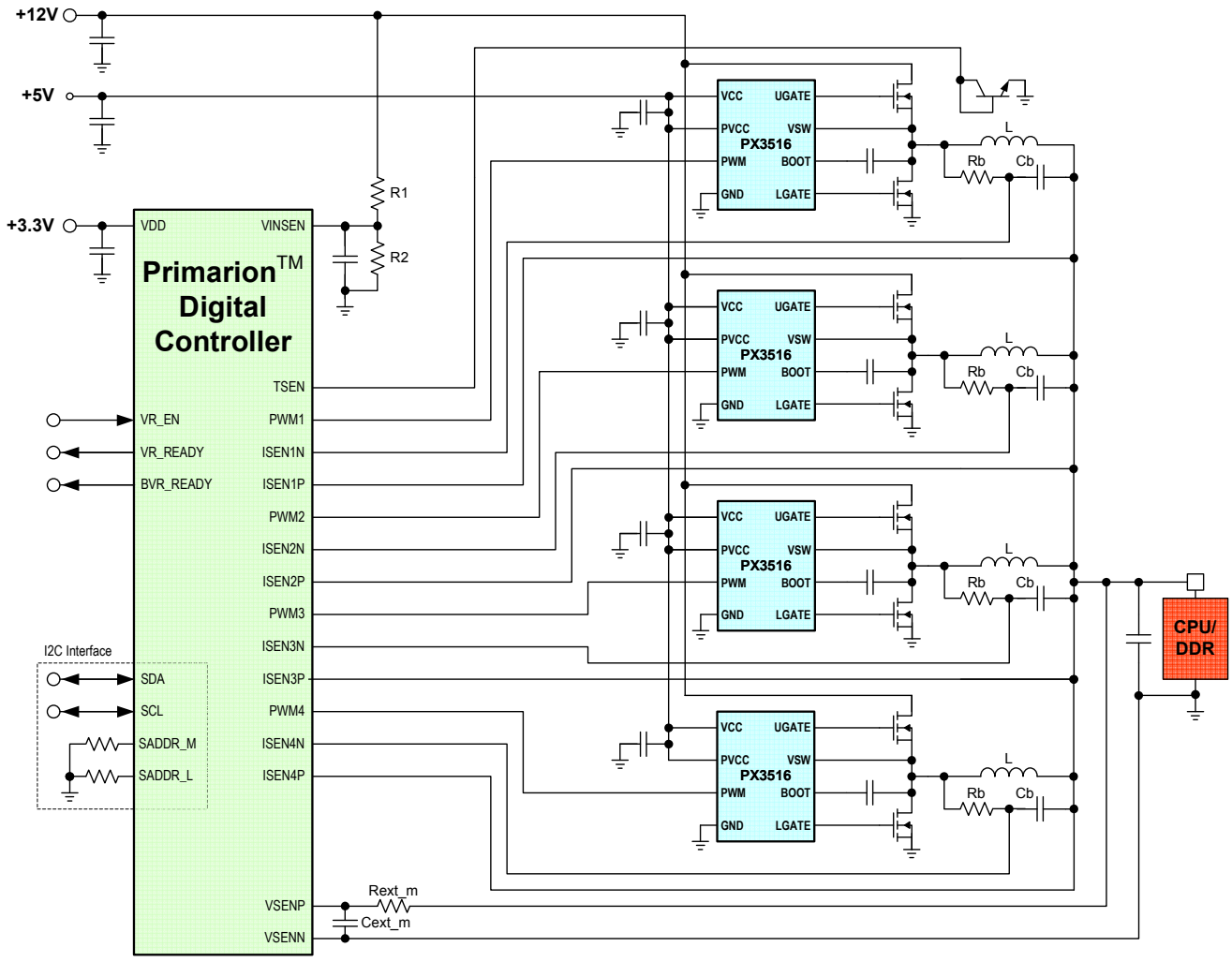


Figure 2 : Typical application diagram of the PX3516

Absolute Maximum Ratings

Stresses above those listed in Table 1 “Absolute Maximum Ratings” may cause permanent damage to the device. These are absolute stress ratings only and operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of this specification.

Table 1. Absolute Maximum Ratings[1]

	Description	Min	Max	Units	Conditions
V_{VCC}	VCC supply voltage (DC)	-0.3	+7	V	
V_{PVCC}	PVCC supply voltage (DC)	-0.3	+7	V	
V_{BOOT}	BOOT voltage	-0.3	+30	V	Referenced to GND
V_{BOOT} - V_{PHASE}	BOOT to PHASE voltage	-1	+7	V	Referenced to PHASE
V_{PHASE}	PHASE voltage, DC	-1	+30	V	DC
V_{PHASE}	PHASE voltage, pulsed	-10	+35	V	Pulse width < 30ns
V_{PWM}	Input voltage	-0.3	+5.5	V	
	UGATE	V_{PHASE} – 0.3	V_{BOOT} + 0.3	V	
	LGATE	-0.3	V_{PVCC} + 0.3	V	
T_J	Junction temperature	-25	150	°C	
T_{STG}	Storage temperature	-55	150	°C	

[1] At T_J = 25℃, unless otherwise specified

Recommended Operating Conditions

Table 2. Recommended Operating Conditions

Symbol	Description	Min	Nom	Max	Units
V_{VCC}	VCC supply voltage rising edge: dv_{CC}/dt>5V/50ms	+4.5	+5.0	+6.5	V
V_{PVCC}	PVCC supply voltage	+4.5	+5.0	+6.5	V
f_{PWM}	PWM signal transition frequency	0.1		2	MHz
T_J	Junction temperature	0		125	°C
$T_{AMBIENT}$	Operating ambient temperature	0		85	°C
$\Theta_{JA(0)}$	Thermal resistance, junction-to-air, note [2]		48		K/W
Θ_{JC}	Thermal resistance, junction-to-case, note [3]		7		K/W

Electrical Characteristics[4]

Table 3. Electrical Characteristics

Parameter	Conditions	Symbol	Min	Typ	Max	Units
Supply Characteristics						
VCC supply current	V_{PWM} = 0V	I_{VCC}		400		µA
PVCC supply current	V_{PWM} = 0V	I_{PVCC}		22		µA
Quiescent current	V_{PWM} = Open	$I_{PVCCQ}+I_{VCCQ}$		410		µA
PVCC Supply current	f_{PWM}=300kHz			2.4		mA
VCC rising threshold	rising edge: dv_{CC}/dt>5V/50ms			3.3	3.9	V
VCC falling threshold			2.7	3.0		V
PWM Input						
Input current	V_{PWM} = +3.3V	I_{PWM_H}		380		µA
	V_{PWM} = 0V	I_{PWM_L}		-310		µA
Sink/source impedance	V_{PWM} = 1V	R_{PWM}	3	5	7	kΩ
Shutdown window (3-state)		V_{PWM_SD}	1.37	1.5	1.77	V
PWM open voltage		V_{PWM_O}		1.5		V
PWM rising threshold		V_{PWM_H}	1.9	2.1	2.4	V
PWM falling threshold		V_{PWM_L}	0.7	1.15	1.3	V
Minimum pulse width high side	pulse width on PWM	$t_{on\_min\_PWM}$		25		ns
Minimum off time	pulse width on PWM	$t_{off\_min\_PWM}$		100		ns
Upper Gate (UGATE) Output						
Shutdown hold off time	Note[5], no load	t_{SSHD_UG}		170		ns
UGATE rise time	Note[5], 3nF load	t_{r_UG}		10		ns
UGATE fall time	Note [5], 3nF load	t_{f_UG}		10		ns

[2] Θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air
[3] For Θ_{JC}, the case temperature location is the center of the exposed metal pad on the underside of the package
[4] Operating conditions: VCC = +5.0V, PVCC = +5.0V, T_A = 25°C, unless otherwise specified.

Parameter	Conditions	Symbol	Min	Typ	Max	Units
3-state to high propagation delay	Note[5], no load	t_{PDTS_UG}		12		ns
UGATE turn-on propagation delay	Note[5], no load	$t_{D(ON)\_UG}$		35		ns
UGATE turn-off propagation delay	Note[5], no load	$t_{D(OFF)\_UG}$		20		ns
Lower Gate (LGATE) Output						
Shutdown hold-off time	Note[5], no load	t_{SSHD_LG}		170		ns
LGATE rise time	Note[5], 3nF load	t_{r_LG}		10		ns
LGATE fall time	Note[5], 3nF load	t_{f_LG}		5		ns
3-state to low propagation delay	Note[5], no load	t_{PDTS_LG}		11		ns
LGATE turn-on propagation delay	Note[5], no load	$t_{D(ON)\_LG}$		23		ns
LGATE turn-off propagation delay	Note[5], no load	$t_{D(OFF)\_LG}$		7		ns
Output Characteristics						
Upper drive source current	Note[5], current pulse <	I_{SRC_UG}		2		A
Upper drive source impedance	I_{SRC_UG} = 200mA	R_{SRC_UG}		0.9		Ω
Upper drive sink current	Note[5], current pulse <	I_{SNK_UG}		2		A
Upper drive sink impedance	I_{SINK_UG} = 200mA	R_{SNK_UG}		0.95		Ω
Lower drive source current	Note[5], current pulse <	I_{SRC_LG}		2		A
Lower drive source impedance	I_{SRC_UG} = 2A	R_{SRC_LG}		0.95		Ω
Lower drive sink current	Note[5], current pulse <	I_{SNK_LG}		4		A
Lower drive sink impedance	I_{SINK_UG} = 200mA	R_{SNK_LG}		0.47		Ω

[5] Parameter verified by design.

Timing Diagram

1.37V<PWM<1.77V

Figure 3 : Timing Diagram

Table 4. Pin Function Description

Pin #	Name	Description
1	UGATE	Upper gate drive output. Connect to the gate of high-side power N-channel MOSFET
2	BOOT	Floating bootstrap supply pin for the upper gate drive. Connect the bootstrap capacitor between this pin and the PHASE pin. The bootstrap capacitor provides the charge to turn on the upper MOSFET. See the Internal Bootstrap Device section herein for guidance in choosing the capacitor value.
3	N/C	No connection
4	PWM	The PWM signal is the control input for the driver and is to be connected to the PWM output of the controller. The PWM signal can enter three distinct states during operation. See figure 1 for further details.
5	GND	Can be left N/C since main GND connection to circuit board is via die pad. Must not be used as single ground connection.
6	LGATE	Lower gate drive output. Connect to the gate of the low-side power N-channel MOSFET
7	VCC	This pin supplies housekeeping/logic power to the IC, it is rated for +5V operation. Place a high quality low ESR ceramic capacitor from this pin to GND.
8	N/C	No connection
9	PVCC	This pin supplies power to the lower and upper gate, rated for +5V. Place a high quality low ESR ceramic capacitor from this pin to GND.
10	PHASE	Connect this pin to the source of the upper MOSFET and the drain of the lower MOSFET. This pin provides a return path for the upper gate drive.
Die Pad		Bias and reference ground. All signals are referenced to this node. It is also the power ground return of the driver. It is mandatory to connect the die paddle electrically and thermally to the circuit board.

Mode of operation

The PX3516 functionality is enabled by the VCC pin. When the VCC pin voltage overcomes the VCC rising voltage threshold the driver begins to operate depending on the PWM status. Before the VCC voltage reaches the VCC rising threshold both MOSFET are kept in OFF state. For VCC is recommended to have a slope for the rising edge higher then 5V/50ms. On the PVCC pin no UVLO function is implemented.

The VCC (as well the PVCC) can range between 4.5V and 6.5V; this gives the flexibility to work with the 5V bus or in case optimize the efficiency choosing a different driving voltage.

The PX3516 functionality is driven by the PWM signal transitions. When the PWM signal performs a transition between low state to high state (PWM voltage higher than 2.4V) the Low Side MOSFET is turned off, after the turn off delay propagation time. Then the High Side MOSFET is turned on, after the turn on propagation delay time. Once the on time is expired the PWM signal provides a transition between the high states to the low state (PWM voltage lower than 1V). This will drive the High Side MOSFET from the ON state to the OFF state, after the turn off propagation delay time. The PX3516 is also capable to drive the two external MOSFET both in off state. When the PWM signal enters in the shut down window or 3-state (typically between 1.37V and 1.77V) after the shut down hold off time both MOSFET are switched off. This feature is useful when the IC controller wants to reduce the number of active phases in order to reduce the power consumption. In principle the 3-state status can be used also to improve the transition between high loads to low load.

The PX3516 implements an embedded resistors network, which forces the PWM pin of the device in the middle of the shut down window, if the PWM input is left floating from the controller.

In order to avoid cross conduction between the High Side MOSFET and the Low Side MOSFET an anti-shoot-through control is implemented with the adaptive scheme. The adaptive scheme is implemented in order to use a variety of different power MOSFET for different kind of conversion. Nevertheless the dead time is kept as short as possible in order to increase the efficiency of the overall solution.

The driver includes gate drive functionality to protect against shoot through. In order to protect the power stage from overlap, both High Side and Low Side MOSFET being on at the same time, the adaptive control circuitry monitors the voltage at the “PHASE” pin. When the PWM signal goes low, the High Side MOSFET will begin to turn off. Once the “PHASE” pin falls below 1V, the Low Side MOSFET is gated on. Additionally, the gate to source voltage of the High Side MOSFET is also monitored. When VGS(High Side) is discharged below 1V, a threshold known to turn High Side MOSFET off, a secondary delay is initiated, which results in Low Side being gated “ON” regardless of the state of the “VSWH” pin. This way it will be ensured that the converter can sink current efficiently and the bootstrap capacitor will be refreshed appropriately during each switching cycle.

During the start up depending on several factors it can be that the power input for the conversion (12V) rise before the 5V input. In this case it could happen that the high side has an induced turn on. In order to avoid this undesirable effect the PX3516 embeds a resistance of 500 kOhm between UGATE pin and PHASE pin.

Current capability and Internal Bootstrap

The PX3516 implements high current capability and low ohmic pull down resistances for the driving stages. The high current capability ensures fast switching transition for the MOSFET in order to reduce the switching losses (2A of driving source/sink current for the upper MOSFET) even with high gate charge high side. The low ohmic pull down resistance (Low driver sink impedance 0.5 Ohm) is mainly important to avoid the induced turn on phenomenon on the low side during the fast turn on of the high side MOSFET.

The high side is powered through the bootstrap circuitry The PX3516 provides embedded bootstrap diode, so to complete the power network only a capacitance between PHASE and BOOT is needed. In many cases the PX3516 is optimized for the best switching behavior so an external resistance is not needed. The bootstrap capacitance is chosen depending on the high side gate charge. The following formula is giving a good estimation of the voltage drop across the bootstrap capacitance due to the charging of the high side:

$$CBOOT > QGATE/\Delta VBOOT$$

Where the $\Delta VBOOT$ is the desired variation of the bootstrap voltage.

The low side driver is powered through the PVCC pin. Same considerations and formula done for the bootstrap capacitance can be done for the capacitance used to filter the PVCC pin.

The driving stage of the PX3516 is optimized for the 5V driving voltage. This design makes the PX3516 driver more suitable than other variable driving voltage drivers optimized for 10V – 12V range. In this case superior performance are expected using an optimized 5V driver at 6V of driving voltage compared to a optimized 12V driver used at the same driving voltage.

Power dissipation

The power dissipation of the driver is given by gate charge of the external power MOSFET. The following formulas held:

Pdiss=PVCC*FSW*(QGHS+QGLS)

Where FSW is the switching frequency and QGHS and QGLS are respectively the gate charge of the high side and the gate charge of the low side at the PVCC driving voltage.

The very low thermal resistance package used for the PX3516 allows the device to avoid any usage of external resistances to decrease the power dissipation inside the driver. Anyway since the thermal resistance is strongly influenced by the numbers of layers used in the board, it is recommended to check roughly the expected junction temperature via the power calculation.

Layout Considerations

The PX3516 has a good protection systems against unwanted overshoot and undershoot; the PHASE pin can range between dynamically -10V to 35V (30ns).

Anyway the parasitic inductances of the PCB and of the power devices' packaging (both upper and lower MOSFET) can cause serious ringing, exceeding absolute maximum rating of the devices. Careful layout can help minimize such unwanted stress. The following advice is meant to lead to an optimized layout:

- Keep decoupling loops (PVCC-GND and BOOT-PHASE) as short as possible.
- Minimize trace inductance, especially on low-impedance lines. All power traces (UGATE, PHASE, LGATE, GND, PVCC) should be short and wide, as much as possible.
- Minimize the area of the PHASE node. Ideally, the source of the upper and the drain of the lower MOSFET should be as close as thermally allowable.
- Minimize the current loop of the output and input power trains. Short the source connection of the lower MOSFET to ground as close to the transistor pin as feasible. Input capacitors (especially ceramic decoupling) should be placed as close to the drain of upper and source of lower MOSFET as possible.

To optimize heat spreading, copper should be placed directly underneath the IC. The copper area can be extended beyond the bottom area of the IC and/or connected to buried copper plane(s) with thermal vias. This combination of vias for vertical heat escape, extended copper plane, and buried planes for heat spreading allows the IC to achieve its full thermal potential.

Thresholds variations

The possibility to use a wide range of power supply voltages (from 4.5V up to 6.5V) implies a shifting in the thresholds voltages for the following parameters: VPWM_O, VPWM_H, VPWM_L, VPWM_SD_L, VPWM_SD_H (where VPWM_SD_L/H are respectively the low and high thresholds for the shut down windows). The typical behavior of these thresholds with the power supply is shown in the following graph.

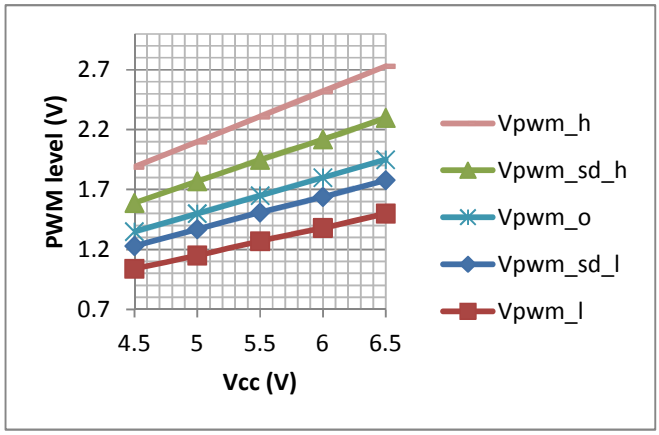


Figure 4 : Variation of the PWM input threshold versus the VCC supply voltage

Physical Characteristics (PG-TDSON-10-2 package)

Figure 5. Physical Dimensions of the package.

Suggested land pattern

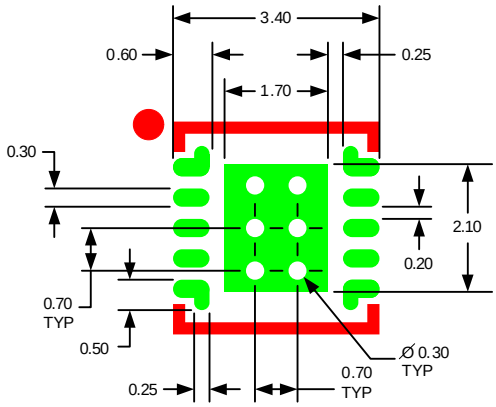


Figure 6: Physical dimensions of the PCB footprint.

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Published by
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