OBSOLETE

MICRON TECHNOLOGY, INC.

MT5C1008
128K x 8 SRAM

SRAM

128K x 8 SRAM

WITH OUTPUT ENABLE

FEATURES

- High speed: 12, 15, 20 and 25
- Available in 300 mil- and 400 mil-wide SOJ packages
- High-performance, low-power, CMOS double-metal process
- Single +5V ±10% power supply
- Easy memory expansion with $\overline{CE1}$, CE2 and $\overline{OE}$ options
- All inputs and outputs are TTL-compatible
- Fast $\overline{OE}$ access time: 6ns

OPTIONS — MARKING

- Timing

12ns access	-12
15ns access	-15
20ns access	-20
25ns access	-25

- Packages

Plastic DIP (400 mil)	None
Plastic SOJ (400 mil)	DJ
Plastic SOJ (300 mil)	SJ

- 2V data retention (optional) — L
- 2V data retention, low power (optional) — LP

- Temperature

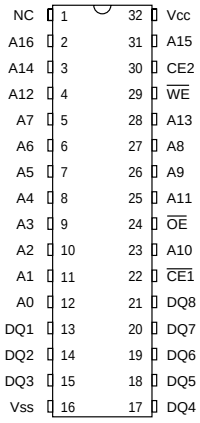
Commercial	(0°C to +70°C)	None
Industrial	(-40°C to +85°C)	IT
Automotive	(-40°C to +125°C)	AT
Extended	(-55°C to +125°C)	XT

- Part Number Example: MT5C1008DJ-20 L

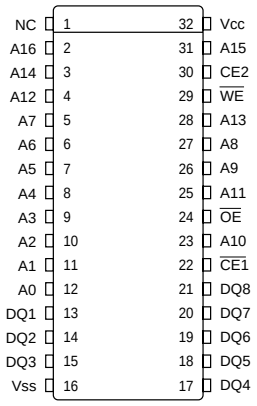
NOTE: Not all combinations of operating temperature, speed, data retention and low power are necessarily available. Please contact the factory for availability of specific part number combinations.

PIN ASSIGNMENT (Top View)

32-Pin DIP
(SA-6)



32-Pin SOJ
(SD-4, SD-5)



GENERAL DESCRIPTION

The MT5C1008 is organized as a 131,072 x 8 SRAM using a four-transistor memory cell with a high-speed, low-power CMOS process. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

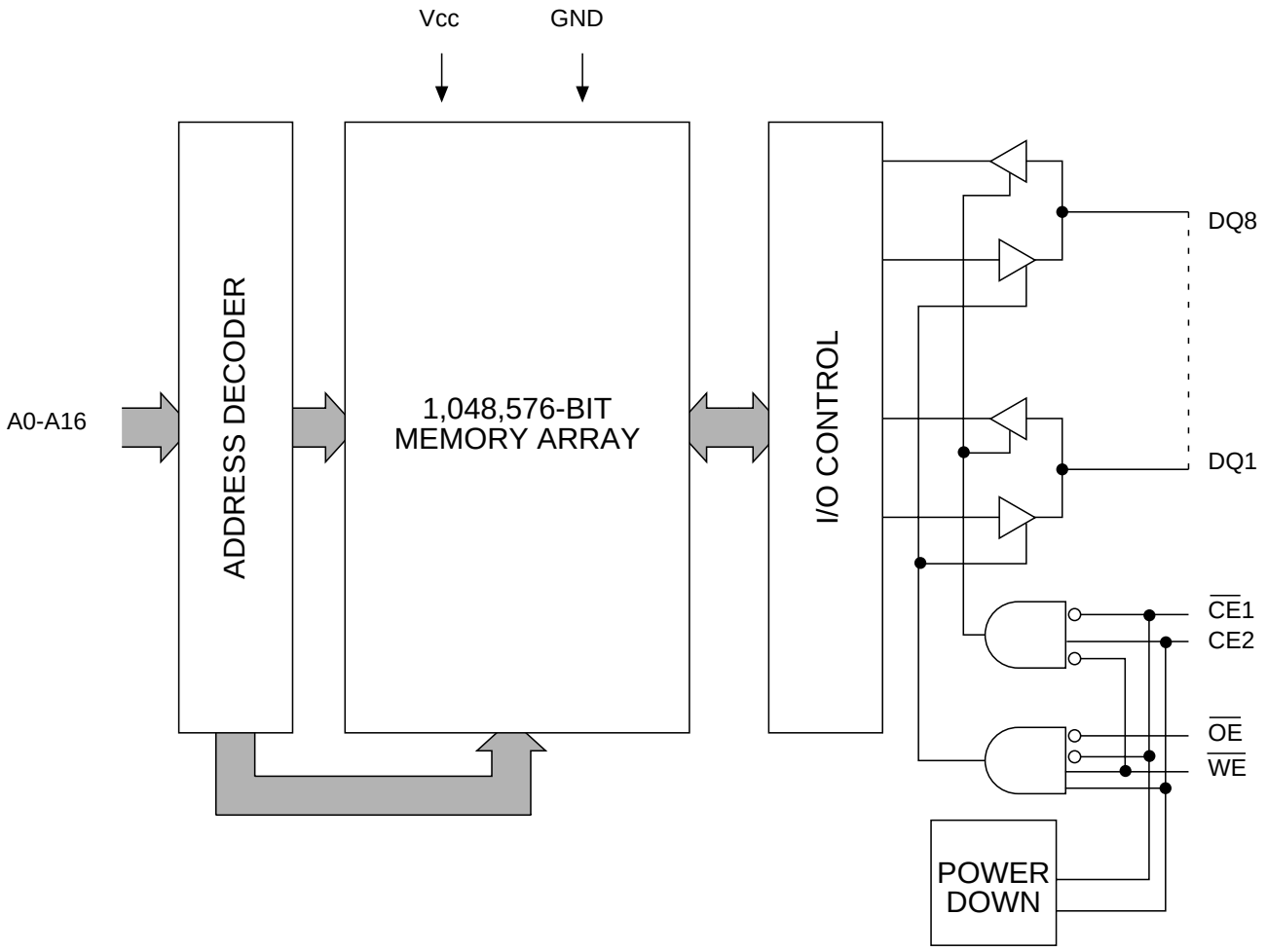
For flexibility in high-speed memory applications, Micron offers dual chip enables ($\overline{CE1}$, CE2) and an output enable ($\overline{OE}$). This enhancement can place the outputs in High-Z for additional flexibility in system design.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE1}$ inputs are both LOW and CE2 is HIGH. Reading is accomplished when $\overline{WE}$ and CE2 remain HIGH and $\overline{CE1}$ and $\overline{OE}$ go LOW. The device offers reduced power standby modes when disabled. This allows system designers to meet low standby power requirements.

The "L" and "LP" versions each provide a 70% reduction in CMOS standby current (I_{SB2}) over the standard version. The "LP" version also provides a 90% reduction in TTL standby current (I_{SB1}). This is achieved by including gated inputs on the $\overline{WE}$, $\overline{OE}$ and address lines. The gated inputs also facilitate the design of battery backed systems where the designer needs to protect against inadvertent battery current drain during power-down, when inputs may be at undefined levels.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL-compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE1}$	CE2	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	X	HIGH-Z	STANDBY
STANDBY	X	X	L	X	HIGH-Z	STANDBY
READ	L	L	H	H	Q	ACTIVE
NOT SELECTED	H	L	H	H	HIGH-Z	ACTIVE
WRITE	X	L	H	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -1V to +7V
Storage Temperature (plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA
Voltage on Any Pin Relative to V_{SS} ..... -1V to V_{CC} +1V

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC} +1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}	I_{LI}	-5	5	µA	
Output Leakage Current	Output(s) disabled 0V ≤ V_{OUT} ≤ V_{CC}	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		V_{CC}	4.5	5.5	V	1

				MAX					
DESCRIPTION	CONDITIONS	SYMBOL	TYP	-12	-15	-20	-25	UNITS	NOTES
Power Supply Current: Operating	CE2 ≥ V_{IH}; $\overline{CE1}$ ≤ V_{IL}; V_{CC} = MAX; f = MAX = 1/ ^tRC; outputs open	I_{CC}	107	195	170	145	130	mA	3, 14
Power Supply Current: Standby	CE2 ≤ V_{IH} or $\overline{CE1}$ ≥ V_{IH}; V_{CC} = MAX; f = MAX = 1/ ^tRC; outputs open	I_{SB1}	37	75	65	50	45	mA	14
	LP version only	I_{SB1}	1.3	3	3	3	3	mA	14
	CE2 ≤ V_{SS} +0.2V; $\overline{CE1}$ ≥ V_{CC} -0.2V; V_{CC} = MAX; V_{IN} ≤ V_{SS} +0.2V or V_{IN} ≥ V_{CC} -0.2V; f = 0	I_{SB2}	0.4	5	5	5	5	mA	14
	L and LP versions only	I_{SB2}	0.3	1.5	1.5	1.5	1.5	mA	14

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz; V_{CC} = 5V	C_I	6	pF	4
Output Capacitance		C_O	6	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) ($0°C \le T_A \le 70°C$; V_{CC} = 5V ±10%)

DESCRIPTION		-12		-15		-20		-25			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle											
READ cycle time	^tRC	12		15		20		25		ns	
Address access time	^tAA		12		15		20		25	ns	
Chip Enable access time	^tACE		12		15		20		25	ns	
Output hold from address change	^tOH	3		3		3		5		ns	
Chip Enable to output in Low-Z	^tLZCE	3		5		5		5		ns	7
Chip disable to output in High-Z	^tHZCE		6		6		8		10	ns	6, 7
Chip Enable to power-up time	^tPU	0		0		0		0		ns	
Chip disable to power-down time	^tPD		12		15		20		25	ns	
Output Enable access time	^tAOE		5		6		6		8	ns	
Output Enable to output in Low-Z	^tLZOE	0		0		0		0		ns	
Output disable to output in High-Z	^tHZOE		4		5		6		10	ns	6
WRITE Cycle											
WRITE cycle time	^tWC	12		15		20		25		ns	
Chip Enable to end of write	^tCW	8		10		12		15		ns	
Address valid to end of write	^tAW	8		10		12		15		ns	
Address setup time	^tAS	0		0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		0		ns	
WRITE pulse width	$^tWP1$	8		9		12		15		ns	
WRITE pulse width	$^tWP2$	10		12		15		15		ns	
Data setup time	^tDS	6		7		8		10		ns	
Data hold time	^tDH	0		0		0		0		ns	
Write disable to output in Low-Z	^tLZWE	3		3		3		3		ns	7
Write Enable to output in High-Z	^tHZWE		6		6		8		10	ns	6, 7

INDUSTRIAL TEMPERATURE SPECIFICATIONS (IT)

The following specifications are to be used for Industrial Temperature (IT) MT5C1001 SRAMs.
(-40°C ≤ T_A ≤ 85°C)

				MAX			
DESCRIPTION	**CONDITIONS**	**SYMBOL**	**TYP**	**-20**	**-25**	**UNITS**	**NOTES**
Power Supply Current: Operating	$\overline{CE2} \geq V_{IH}$; $\overline{CE1} \leq V_{IL}$; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{CC}	107	155	140	mA	3, 13
Power Supply Current: Standby	$\overline{CE2} \leq V_{IH}$ or $\overline{CE1} \geq V_{IH}$; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{SB1}	37	50	45	mA	13
LP version only	$\overline{CE2} \leq V_{IH}$ or $\overline{CE1} \geq V_{IH}$; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{SB1}	1.3	6	6	mA	13
	$\overline{CE2} \leq V_{SS}$ +0.2V; $\overline{CE1} \geq V_{CC}$ -0.2V; V_{CC} = MAX $V_{IN} \leq V_{SS}$ +0.2V or $V_{IN} \geq V_{CC}$ -0.2V; f = 0	I_{SB2}	0.4	6	6	mA	13
L version and LP version	$\overline{CE2} \leq V_{SS}$ +0.2V; $\overline{CE1} \geq V_{CC}$ -0.2V; V_{CC} = MAX $V_{IN} \leq V_{SS}$ +0.2V or $V_{IN} \geq V_{CC}$ -0.2V; f = 0	I_{SB2}	0.3	2	2	mA	13

DATA RETENTION ELECTRICAL CHARACTERISTICS (L version only)

DESCRIPTION	**CONDITIONS**		**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNITS**	**NOTES**
Data Retention Current	$\overline{CE1} \geq$ (Vcc -0.2V) or $\overline{CE2} \leq$ (Vss +0.2V) $V_{IN} \geq$ (V_{CC} -0.2V) or ≤ 0.2V	V_{CC} = 2V	I_{CCDR}		35	170	µA	14
		V_{CC} = 3V	I_{CCDR}		60	325	µA	14

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

Refer to commercial temperature timing parameters for specifications not listed here.
(Notes 5, 14) (-40°C ≤ T_A ≤ 85°C; V_{CC} = 5V ±10%)

DESCRIPTION		**-20**		**-25**			
	SYM	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
WRITE Cycle							
Address hold from end of write	^tAH	1		1		ns	
Address setup time	^tAS	1		1		ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(-40°C ≤ T_A ≤ 85°C; Vcc = 5V ±10%)

DESCRIPTION	**CONDITIONS**	**SYMBOL**	**MIN**	**MAX**	**UNITS**	**NOTES**
Input High (Logic 1) Voltage		V_{IH}	2.3	V_{CC}+1	V	1

AUTOMOTIVE AND EXTENDED TEMPERATURE SPECIFICATIONS (AT AND XT)

The following specifications are to be used for Automotive Temperature (AT) and Extended Temperature (XT) MT5C1001 SRAMs.
(-40°C ≤ T_A ≤ 125°C - AT) (-55°C ≤ T_A ≤ 125°C - XT)

				MAX			
DESCRIPTION	**CONDITIONS**	**SYMBOL**	**TYP**	**-20**	**-25**	**UNITS**	**NOTES**
Power Supply Current: Operating	CE2 ≥ V_{IH}; $\overline{CE1}$ ≤ V_{IL}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{CC}	107	155	140	mA	3, 13
Power Supply Current: Standby	CE2 ≤ V_{IH} or $\overline{CE1}$ ≥ V_{IH}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{SB1}	37	60	55	mA	13
	CE2 ≤ V_{SS} +0.2V; $\overline{CE1}$ ≥ V_{CC} -0.2V; V_{CC} = MAX V_{IN} ≤ V_{SS} +0.2V or V_{IN} ≥ V_{CC} -0.2V; f = 0	I_{SB2}	0.4	7	7	mA	13
L version only	CE2 ≤ V_{SS} +0.2V; $\overline{CE1}$ ≥ V_{CC} -0.2V; V_{CC} = MAX V_{IN} ≤ V_{SS} +0.2V or V_{IN} ≥ V_{CC} -0.2V; f = 0	I_{SB2}	0.3	6	6	mA	13

DATA RETENTION ELECTRICAL CHARACTERISTICS (L version only)

DESCRIPTION	**CONDITIONS**		**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNITS**	**NOTES**
Data Retention Current	$\overline{CE1}$ ≥ (Vcc -0.2V) or CE2 ≤ (Vss +0.2V) V_{IN} ≥ (V_{CC} -0.2V) or ≤ 0.2V	V_{CC} = 2V	I_{CCDR}		35	1,000	µA	14
		V_{CC} = 3V	I_{CCDR}		60	1,500	µA	14

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

Refer to commercial temperature timing parameters for specifications not listed here.
(Notes 5, 14) (-40°C ≤ T_A ≤ 125°C - AT; -55°C ≤ T_A ≤ 125°C - XT; V_{CC} = 5V ±10%)

DESCRIPTION		**-20**		**-25**			
	SYM	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
READ Cycle							
Output hold from address change	^tOH	3		3		ns	
Chip Enable to output in Low-Z	^tLZCE	3		3		ns	7
Address setup time	^tAS	1		1		ns	
WRITE Cycle							
Address hold from end of write	^tAH	1		1		ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(-40°C ≤ T_A ≤ 125°C - AT; -55°C ≤ T_A ≤ 125°C - XT; Vcc = 5V ±10%)

DESCRIPTION	**CONDITIONS**	**SYMBOL**	**MIN**	**MAX**	**UNITS**	**NOTES**
Input High (Logic 1) Voltage		V_{IH}	2.3	V_{CC}+1	V	1

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

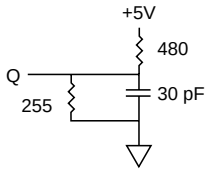


Fig. 1 OUTPUT LOAD EQUIVALENT

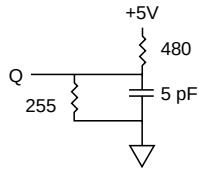


Fig. 2 OUTPUT LOAD EQUIVALENT

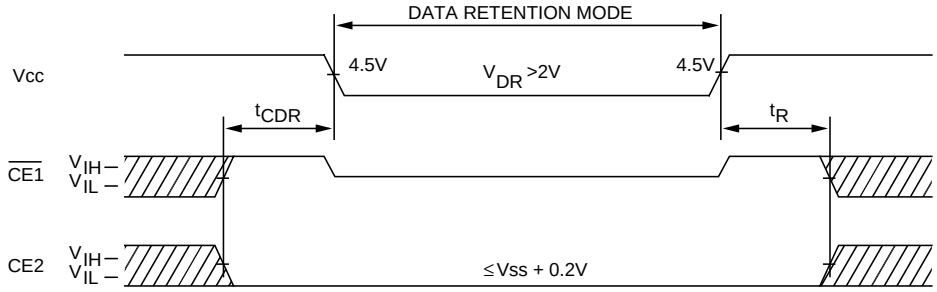
NOTES

1. All voltages referenced to V_{SS} (GND).
2. -3V for pulse width < ${}^{t}RC/2$.
3. I_{CC} is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ${}^{t}HZCE$, ${}^{t}HZOE$ and ${}^{t}HZWE$ are specified with C_L = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ${}^{t}HZCE$ is less than ${}^{t}LZCE$ and ${}^{t}HZWE$ is less than ${}^{t}LZWE$.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables and output enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ${}^{t}RC$ = Read Cycle Time.
12. CE2 timing is the same as $\overline{CE1}$ timing. The waveform is inverted.
13. Chip enable and write enable can initiate and terminate a WRITE cycle.
14. Typical values are measured at 5V, 25°C and 20ns cycle time.
15. Typical currents are measured at 25°C.

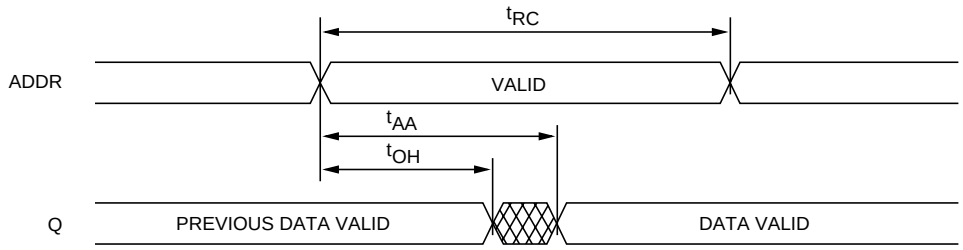
DATA RETENTION ELECTRICAL CHARACTERISTICS (L and LP versions only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
V_{CC} for Retention Data			V_{DR}	2			V	
Data Retention Current L version	$\overline{CE1} \geq (V_{CC}$ -0.2V) or CE2 ≤ (V_{SS} +0.2V) $V_{IN} \geq (V_{CC}$ -0.2V) or ≤ 0.2V	Vcc = 2V	I_{CCDR}		35	150	µA	15
		Vcc = 3V	I_{CCDR}		60	250	µA	15
Data Retention Current LP version	$\overline{CE1} \geq (V_{CC}$ -0.2V) or CE2 ≤ (V_{SS} +0.2V)	Vcc = 2V	I_{CCDR}		35	150	µA	15
		Vcc = 3V	I_{CCDR}		60	250	µA	15
Chip Deselect to Data Retention Time			${}^{t}CDR$	0			ns	4
Operation Recovery Time			${}^{t}R$	${}^{t}RC$			ns	4, 11

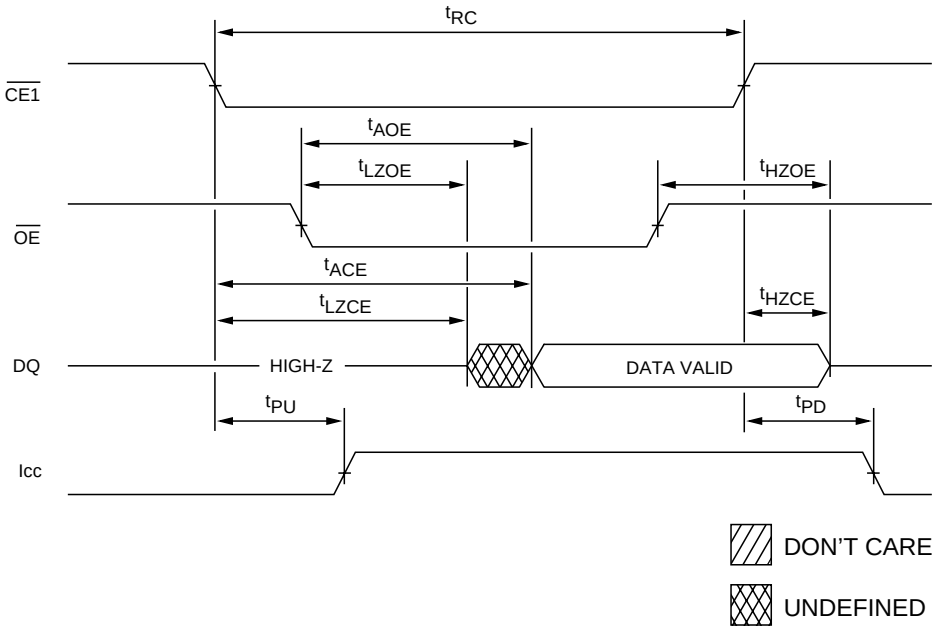
LOW Vcc DATA RETENTION WAVEFORM



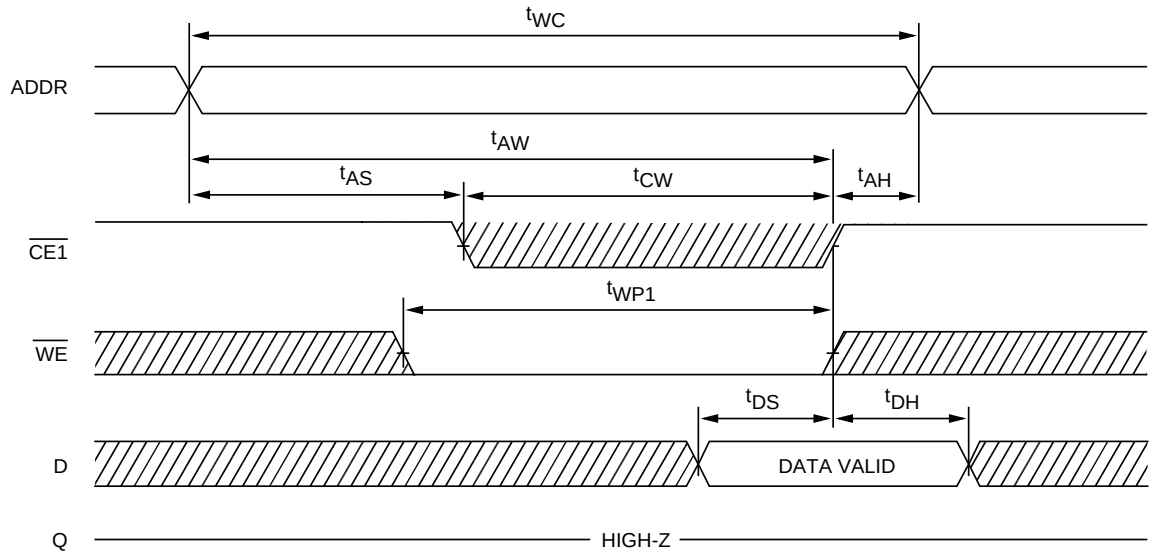
READ CYCLE NO. 1 [8, 9]



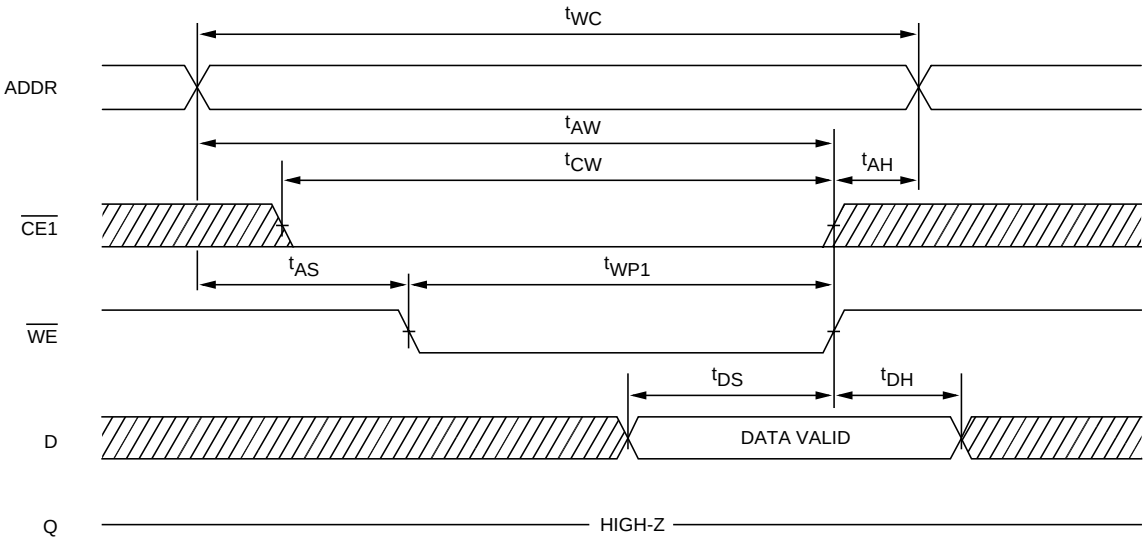
READ CYCLE NO. 2 [7, 8, 10, 12]

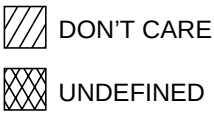


WRITE CYCLE NO. 1 [12, 13]
(Chip Enable Controlled)



WRITE CYCLE NO. 2 [12, 13]
(Write Enable Controlled)

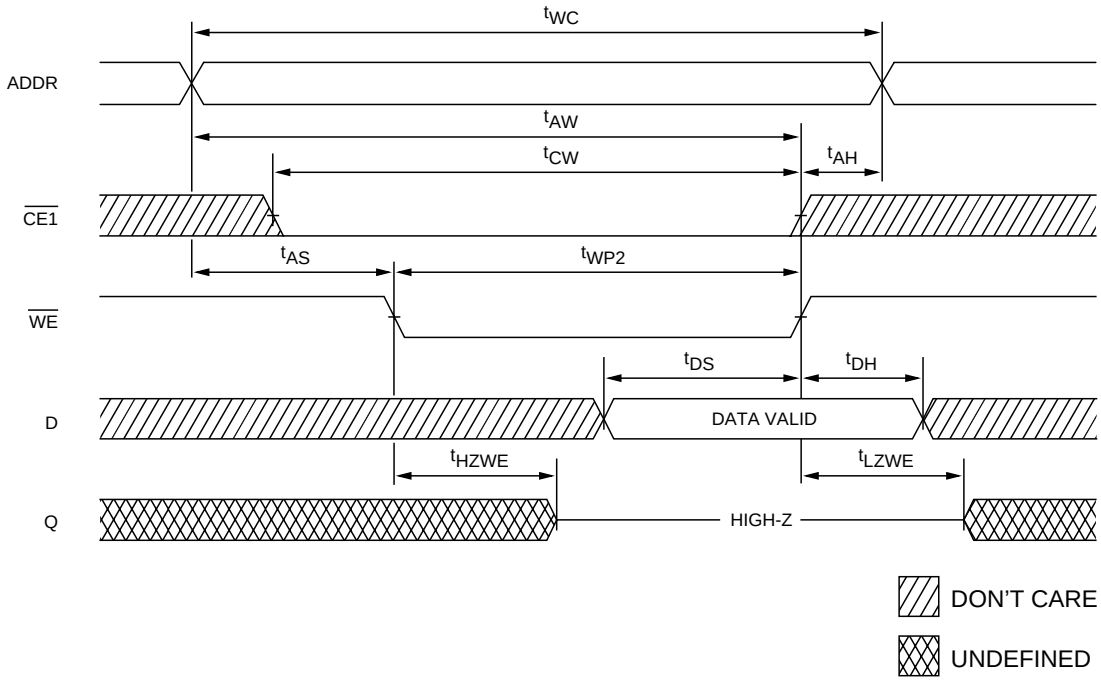




NOTE: Output enable ($\overline{OE}$) is inactive (HIGH).

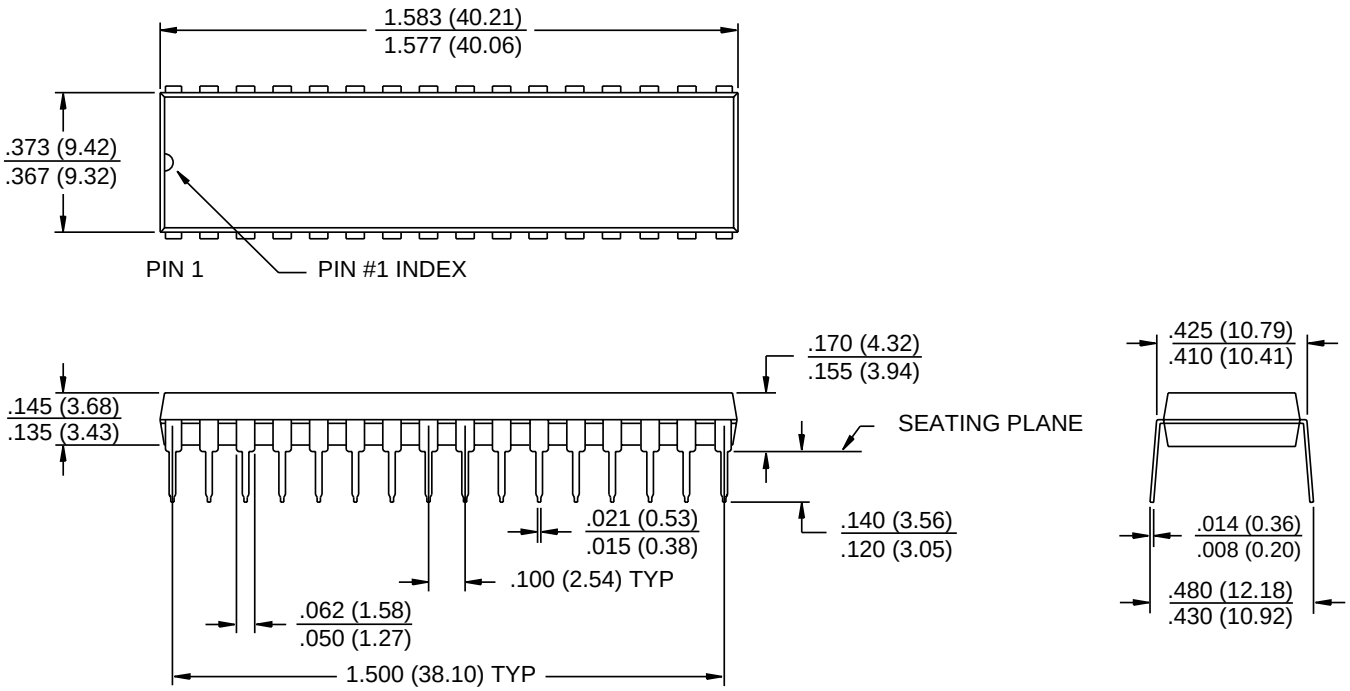
WRITE CYCLE NO. 3 [7, 12, 13]

(Write Enable Controlled)



NOTE: Output enable ($\overline{OE}$) is active (LOW).

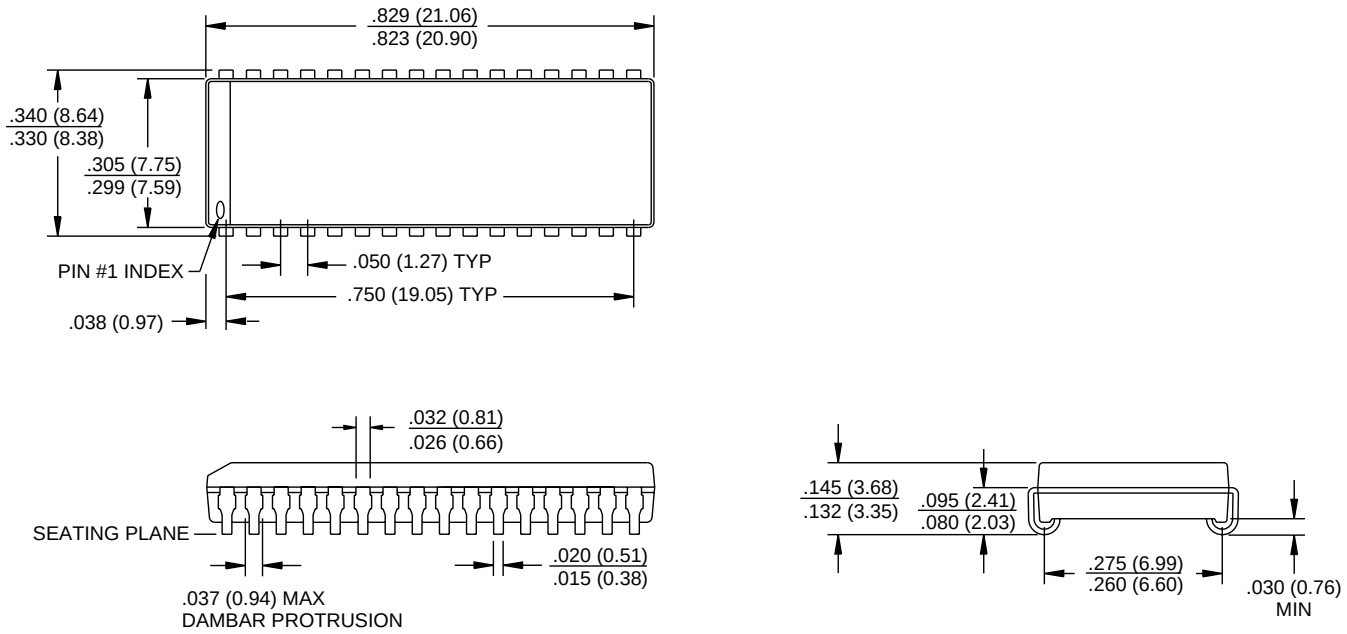
32-PIN PLASTIC DIP



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

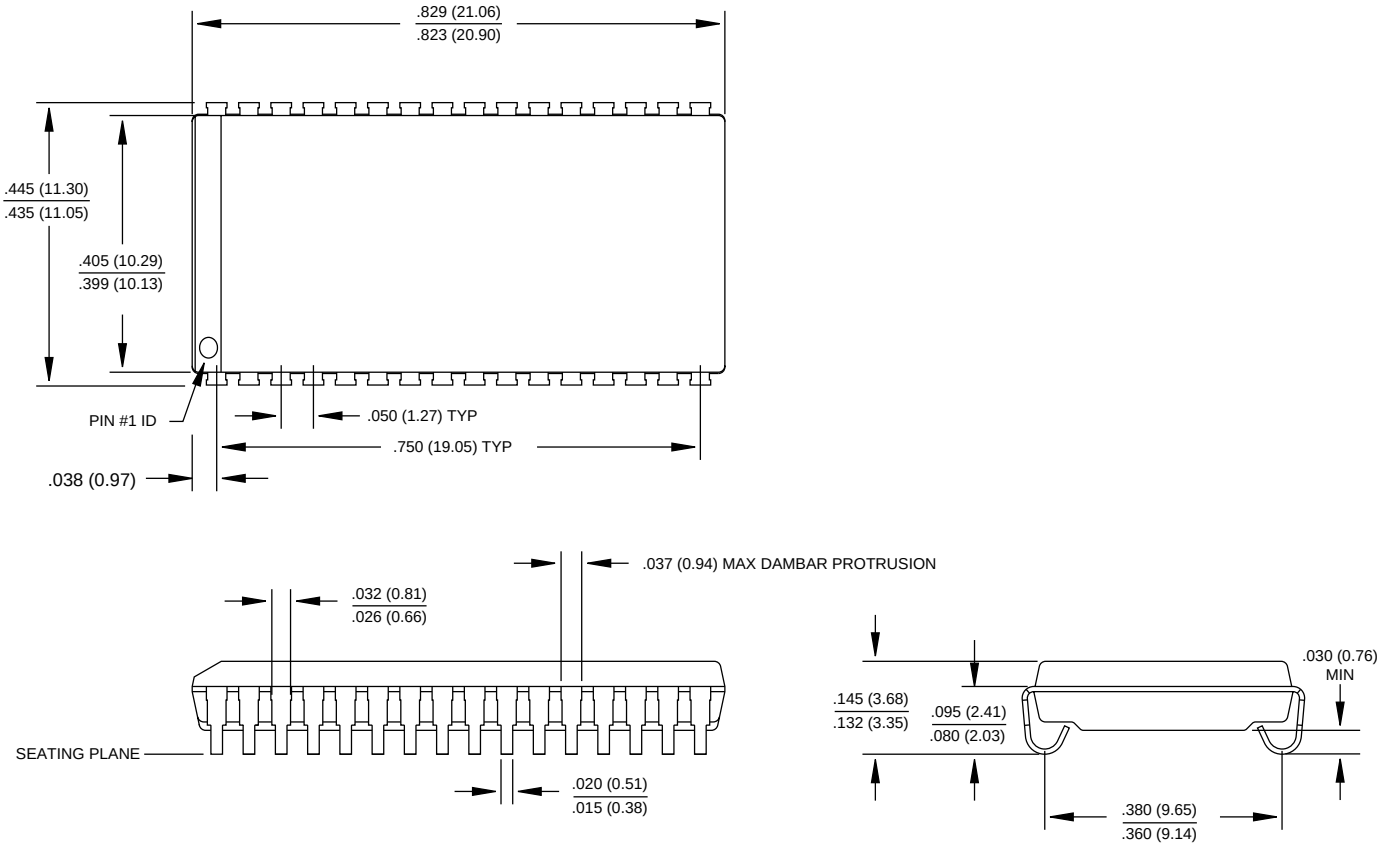
32-PIN PLASTIC SOJ



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

32-PIN PLASTIC SOJ



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

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