



## 2.7Gbps Dual Mux/Buffer with Loopback

MAX3783

### General Description

The MAX3783 is a dual serial multiplexer (mux) and buffer with selectable line-side loopback for system interconnect and serial backplane applications up to 2.7Gbps. Each independent channel consists of a transmitter with fanout of two and a receiver with a 2:1 input mux. Selectable loopback paths support system testing.

Operating from a single 3.3V supply, this device has current-mode logic (CML) inputs and outputs, which can be AC-coupled for PECL compatibility, if desired. The IC is packaged in a compact 48-pin TQFP-EP package with exposed pad. Typical power consumption is 1.12W.

### Applications

2.7Gbps Serial Communications  
System Interconnect  
Serial Backplane  
Fail-Over and Protection Switching

*Typical Application Circuit appears at end of data sheet.*

### Features

- ◆ Provides Redundant Serial I/O
- ◆ 11ps Deterministic Jitter
- ◆ Selectable Loopback
- ◆ On-Chip 50Ω Termination Resistors
- ◆ 3.3V Power Supply
- ◆ Two-Port Integration

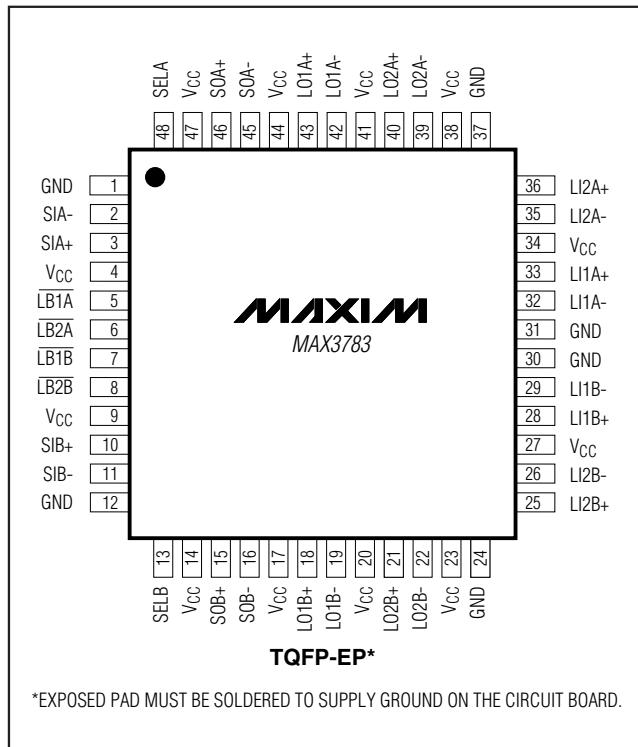
### Ordering Information

| PART        | TEMP RANGE   | PIN-PACKAGE |
|-------------|--------------|-------------|
| MAX3783UCM  | 0°C to +85°C | 48 TQFP-EP* |
| MAX3783UCM+ | 0°C to +85°C | 48 TQFP-EP* |

\*EP = Exposed pad.

+ Denotes a lead-free package.

### Pin Configuration



# 2.7Gbps Dual Mux/Buffer with Loopback

## ABSOLUTE MAXIMUM RATINGS

|  |                                   |
|--|-----------------------------------|
| Supply Voltage, V <sub>CC</sub> .....  | -0.5V to 4.0V                     |
| Continuous Current at Serial Outputs.....                                      | ±36mA                             |
| Voltage at SEL <sub>_</sub> , LB <sub>_</sub> Pins .....                       | -0.5V to (V <sub>CC</sub> + 0.5V) |
| Common-Mode Input Voltage (SI <sub>_</sub> , LI <sub>_</sub> ) .....           | -0.5V to (V <sub>CC</sub> + 0.5V) |
| Differential Input Voltage (SI <sub>_</sub> , LI <sub>_</sub> ) (Note 1) ..... | ±2.8V                             |

|   |   |       |
|---|---|-------|
| Continuous Power Dissipation (T <sub>A</sub> = +85°C) ..... | 48-Pin TQFP-EP (derate 27mW/°C above +85°C) ..... | 1.76W |
| Storage Ambient Temperature .....                           | -55°C to +150°C                                   |       |
| Lead Temperature (soldering, 10s) .....                     | +300°C  |       |

**Note 1:** The sum of the common-mode voltage and differential voltage on any input pin must be within -0.5V to (V<sub>CC</sub> + 0.5V).

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS

(V<sub>CC</sub> = 3.0V to 3.6V, serial data rate = 2.75Gbps, T<sub>A</sub> = 0°C to +85°C. Typical values at V<sub>CC</sub> = 3.3V, T<sub>A</sub> = +25°C, unless otherwise noted.)

| PARAMETER                          | SYMBOL                          | CONDITIONS  | MIN  | TYP   | MAX  | UNITS |
|------------------------------------|---------------------------------|---|------|-------|------|-------|
| Maximum Serial Data Rate           |                                 |   | 2.75 | 3.125 |      | Gbps  |
| Power Dissipation                  |                                 | AC-coupled inputs, outputs  | 1.12 | 1.68  |      | W     |
| Supply Current                     | I <sub>CC</sub>                 |   | 340  | 466   |      | mA    |
| CML Differential Output Voltage    | V <sub>OD</sub>                 | R <sub>L</sub> = 50Ω to V <sub>CC</sub> , or 100Ω differential (Note 2)   | 1200 | 1500  | 2200 | mVp-p |
| CML Differential Input Voltage     | V <sub>ID</sub>                 |   | 200  | 1600  | 2200 | mVp-p |
| CML Output Impedance               | R <sub>OUT</sub>                | Single ended  | 42.5 | 50    | 57.5 | Ω     |
| CML Input Impedance                | R <sub>IN</sub>                 | Differential  | 85   | 100   | 116  | Ω     |
| Random Jitter                      |                                 | (Note 3)  | 1    | 2     |      | psRMS |
| Deterministic Jitter               |                                 | (Notes 3, 4, 5)   | 11   | 25    |      | psp-p |
| CML Output Edge Speed (20% to 80%) | t <sub>R</sub> , t <sub>F</sub> | 2.5Gbps input (Note 6)  | 70   | 135   |      | ps    |
|                                    |                                 | 1.25Gbps input (Note 3)   | 80   | 200   |      |       |
| Propagation Delay                  |                                 | LI <sub>_</sub> to SO <sub>_</sub> , SI <sub>_</sub> to LO <sub>_</sub> , LI <sub>_</sub> to LO <sub>_</sub> (Note 3) | 340  | 500   |      | ps    |
| Multiplexer Switch Time            |                                 | SEL <sub>_</sub> or LB <sub>_</sub> to valid output   | 9    |       |      | ns    |
| TTL Input Current High             |                                 | V <sub>IH</sub> = +2.0V to (V <sub>CC</sub> +0.3V)  |      | 180   |      | μA    |
| TTL Input Current Low              |                                 | V <sub>IL</sub> = -0.3V to +0.8V  |      | 440   |      | μA    |

**Note 2:** Tested using a repeating 1010 pattern at 500Mbps.

**Note 3:** AC specifications are guaranteed by design and characterization.

**Note 4:** Deterministic jitter is measured with a repeating K28.5 pattern.

**Note 5:** With the peak-to-peak input swing on the selected (transmitted) CML input equal to or greater than that on the nonselected inputs.

**Note 6:** AC specifications are guaranteed by test.

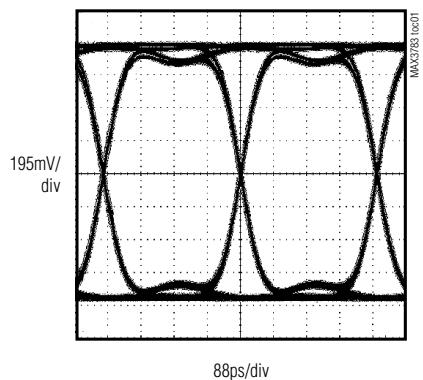
# 2.7Gbps Dual Mux/Buffer with Loopback

MAX3783

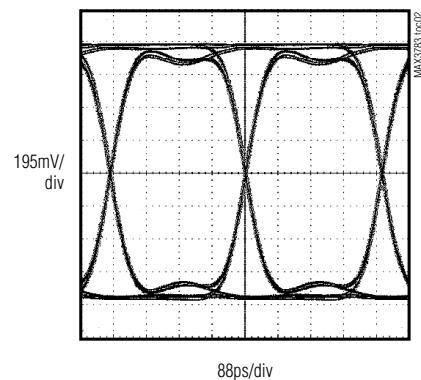
## Typical Operating Characteristics

( $V_{CC} = 3.3V$ ,  $T_A = +25^\circ C$ , unless otherwise noted.)

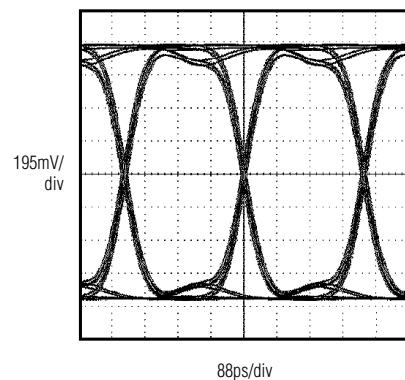
**ELECTRICAL EYE DIAGRAM**  
2.75 Gbps,  $2^{23}$  - 1 PRBS PATTERN



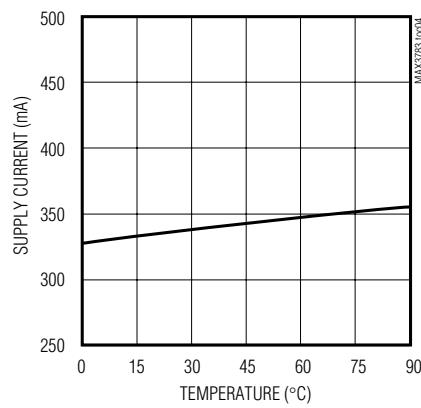
**ELECTRICAL EYE DIAGRAM**  
2.75 Gbps, K28.5 PATTERN



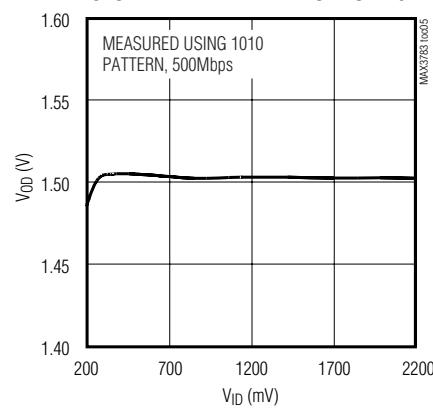
**ELECTRICAL EYE DIAGRAM**  
3.125 Gbps, K28.5 PATTERN



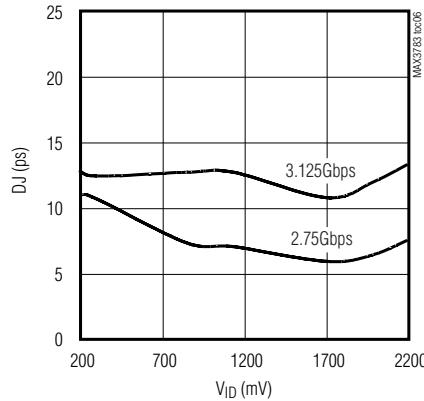
**SUPPLY CURRENT vs. TEMPERATURE**



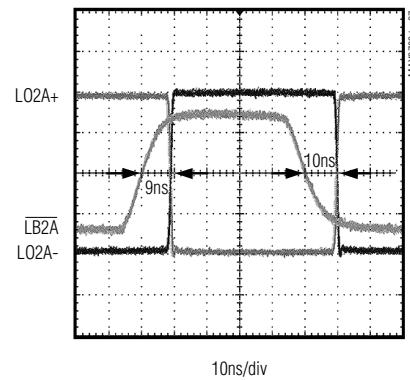
**CML DIFFERENTIAL OUTPUT VOLTAGE**  
vs. CML DIFFERENTIAL INPUT VOLTAGE



**DETERMINISTIC JITTER vs. CML**  
DIFFERENTIAL INPUT VOLTAGE



**MUXPLEXER SWITCH TIME**



## 2.7Gbps Dual Mux/Buffer with Loopback

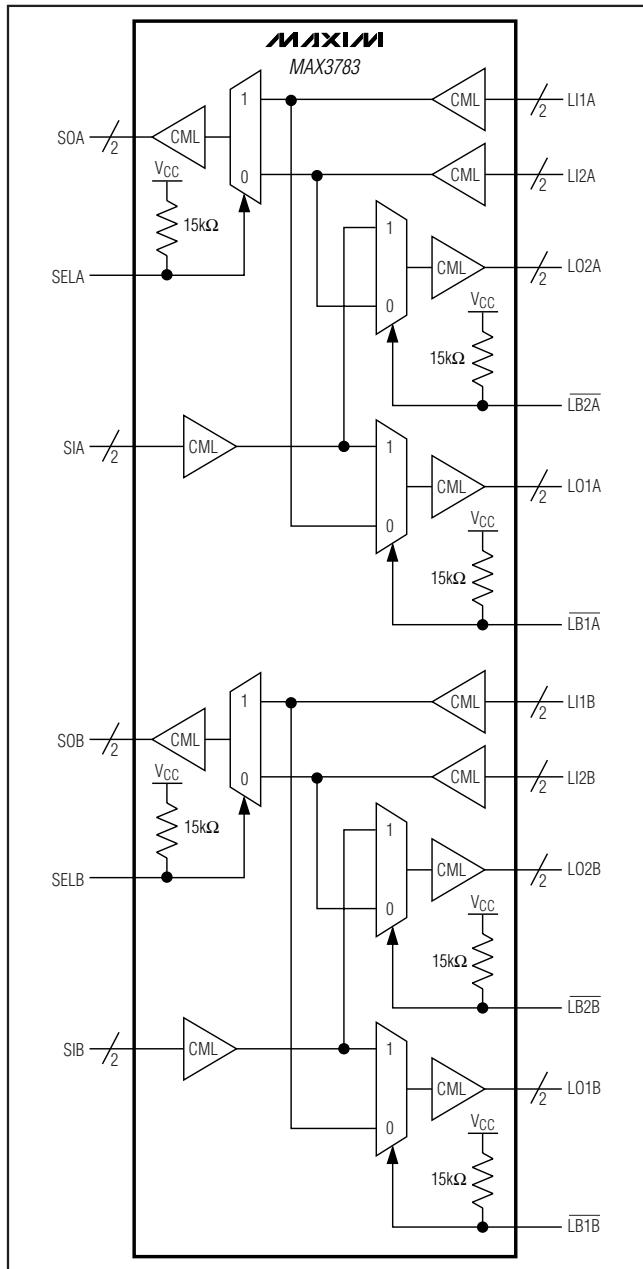
### Pin Description

| PIN   | NAME        | FUNCTION  |
|---|-------------|---|
| 1, 12, 24,<br>30, 31, 37                              | GND         | Supply Ground   |
| 2   | SIA-        | Serial Input A Negative, CML  |
| 3   | SIA+        | Serial Input A Positive, CML  |
| 4, 9, 14, 17,<br>20, 23, 27,<br>34, 38, 41,<br>44, 47 | VCC         | +3.3V Supply  |
| 5   | LB1A        | Line Out 1A Loopback Mode Select. TTL low selects loopback.   |
| 6   | LB2A        | Line Out 2A Loopback Mode Select. TTL low selects loopback.   |
| 7   | LB1B        | Line Out 1B Loopback Mode Select. TTL low selects loopback.   |
| 8   | LB2B        | Line Out 2B Loopback Mode Select. TTL low selects loopback.   |
| 10  | SIB+        | Serial Input B Positive, CML  |
| 11  | SIB-        | Serial Input B Negative, CML  |
| 13  | SELB        | Serial Output B Input Select, TTL   |
| 15  | SOB+        | Serial Output B Positive, CML   |
| 16  | SOB-        | Serial Output B Negative, CML   |
| 18  | LO1B+       | Line Out 1B Positive, CML   |
| 19  | LO1B-       | Line Out 1B Negative, CML   |
| 21  | LO2B+       | Line Out 2B Positive, CML   |
| 22  | LO2B-       | Line Out 2B Negative, CML   |
| 25  | LI2B+       | Line In 2B Positive, CML  |
| 26  | LI2B-       | Line In 2B Negative, CML  |
| 28  | LI1B+       | Line In 1B Positive, CML  |
| 29  | LI1B-       | Line In 1B Negative, CML  |
| 32  | LI1A-       | Line In 1A Negative, CML  |
| 33  | LI1A+       | Line In 1A Positive, CML  |
| 35  | LI2A-       | Line In 2A Negative, CML  |
| 36  | LI2A+       | Line In 2A Positive, CML  |
| 39  | LO2A-       | Line Out 2A Negative, CML   |
| 40  | LO2A+       | Line Out 2A Positive, CML   |
| 42  | LO1A-       | Line Out 1A Negative, CML   |
| 43  | LO1A+       | Line Out 1A Positive, CML   |
| 45  | SOA-        | Serial Output A Negative, CML   |
| 46  | SOA+        | Serial Output A Positive, CML   |
| 48  | SELA        | Serial Out A Input Select, TTL  |
| EP  | Exposed Pad | Ground. Must be soldered to the circuit board for proper thermal and electrical performance (see the Exposed-Pad (EP) Package section). |

# 2.7Gbps Dual Mux/Buffer with Loopback

**MAX3783**

## Functional Diagram



## Detailed Description

The MAX3783 is a 2.7Gbps dual serial mux/buffer with selectable line-side loopback for system test. Each half of the MAX3783 provides a transmitter with a fanout of two and a receiver with a 2:1 mux, as shown in the functional diagram.

## Input Stages

The input amplifiers accept CML or AC-coupled PECL signals and each input has an on-chip  $100\Omega$  differential impedance for optimal termination, as shown in Figure 1.

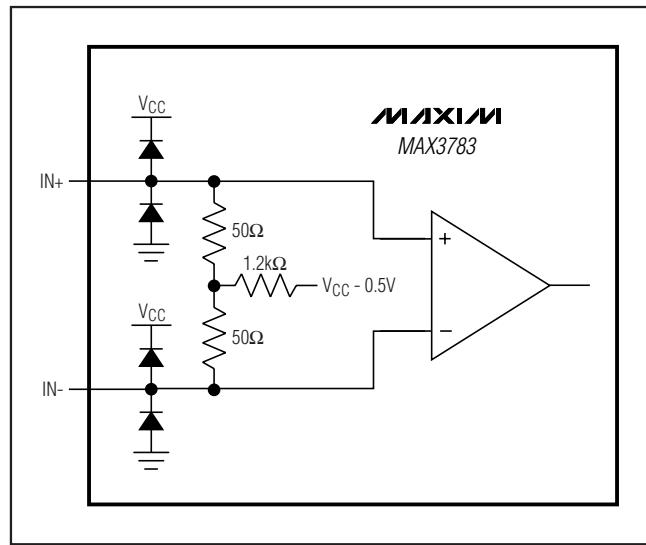


Figure 1. Input Structure

## Control Lines

TTL-compatible control lines are provided to select the MAX3783's operating mode (Table 1). SELA and SELB set the mux for channels A and B, respectively, to select  $LI1_{\_}$  or  $LI2_{\_}$  to connect to the  $SO_{\_}$  output.  $LB1A$ ,  $LB1B$ ,  $LB2A$ , and  $LB2B$  enable loopback mode for each of the four  $LO_{\_}$  outputs. All control lines are internally pulled high through  $15k\Omega$  resistors.

## Table 1. Operating Modes

| SEL <sub>_</sub> | SO <sub>_</sub>  |
|------------------|------------------|
| 0                | LI2 <sub>_</sub> |
| 1                | LI1 <sub>_</sub> |

| LB <sub>_</sub> | LO <sub>_</sub> |
|-----------------|-----------------|
| 0               | LI <sub>_</sub> |
| 1               | SI <sub>_</sub> |

## Output Buffers

The outputs are high-speed CML interfaces with  $50\Omega$  back termination, as shown in Figure 2.

## Exposed-Pad (EP) Package

The exposed pad on the 48-pin TQFP-EP provides a very low thermal-resistance path for heat removal from the IC. The pad is also electrical ground on the MAX3783 and must be soldered to the circuit board for proper thermal and electrical performance.

## 2.7Gbps Dual Mux/Buffer with Loopback

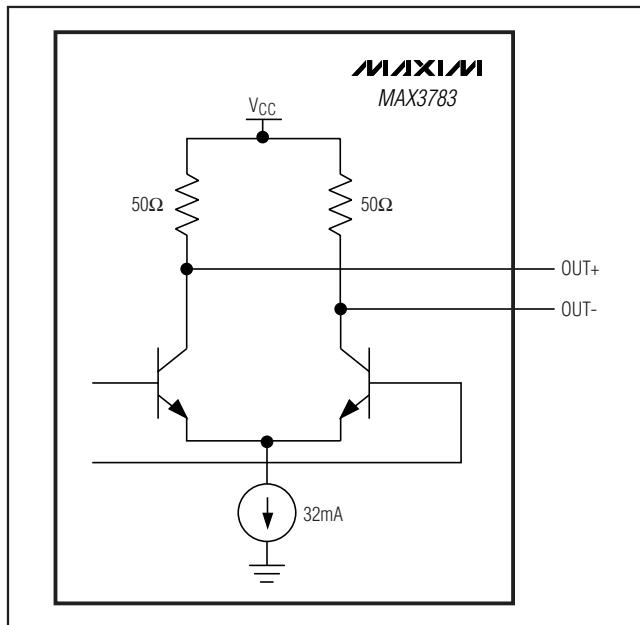


Figure 2. CML Output Structure

### Chip Information

TRANSISTOR COUNT: 2816

PROCESS: BIPOURAL

### Package Information

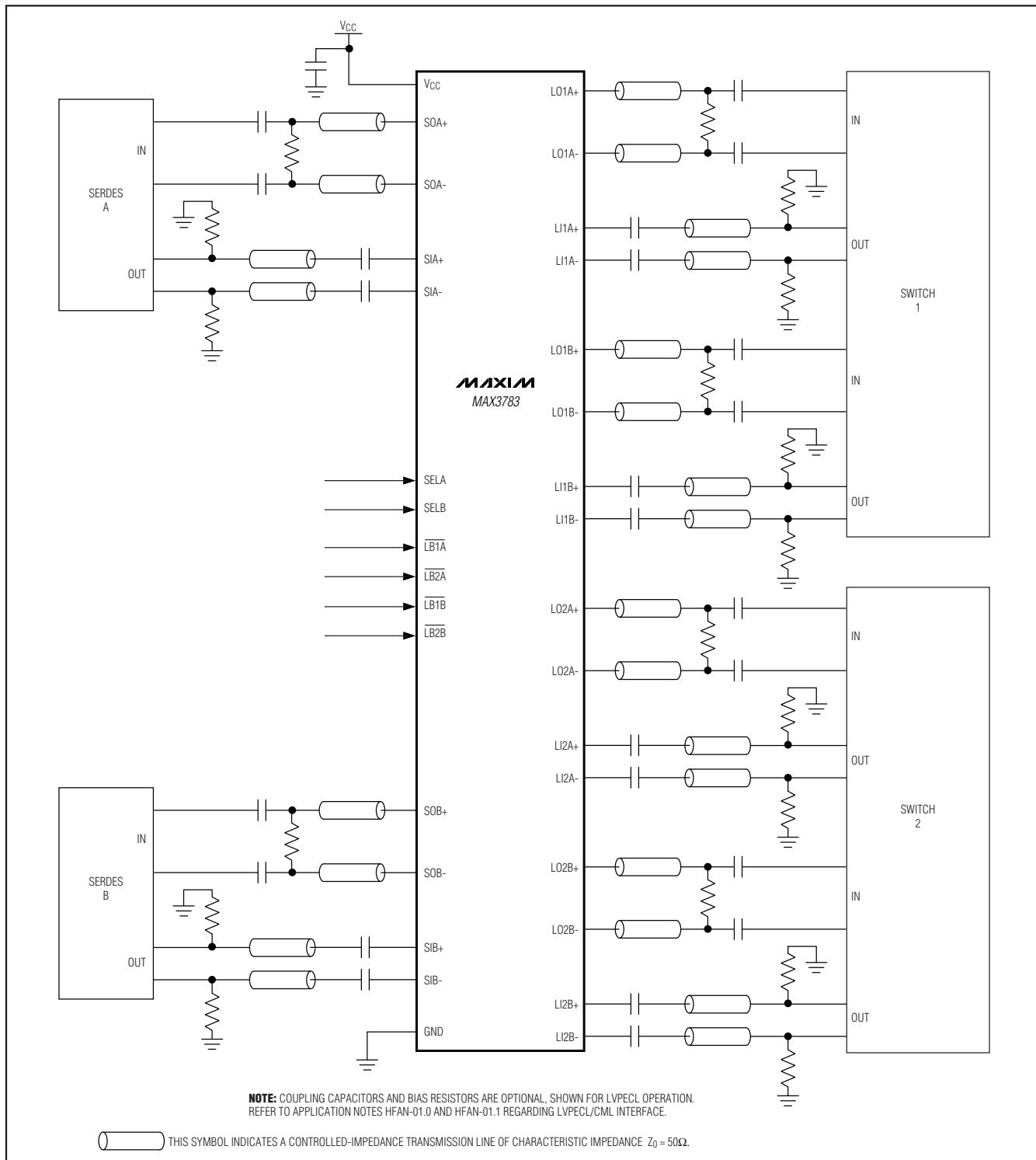
(For the latest package outline information, go to  
[www.maxim-ic.com/packages](http://www.maxim-ic.com/packages).)

| PACKAGE TYPE | DOCUMENT NO.            |
|--------------|-------------------------|
| 48 TQFP-EP   | <a href="#">21-0065</a> |

## 2.7Gbps Dual Mux/Buffer with Loopback

MAX3783

Typical Application Circuit



## 2.7Gbps Dual Mux/Buffer with Loopback

### Revision History

| REVISION NUMBER | REVISION DATE | DESCRIPTION   | PAGES CHANGED |
|-----------------|---------------|---|---------------|
| 0               | 10/01         | Initial release.  | —             |
| 1               | 3/06          | Added lead-free device to the Ordering Information table.   | 1             |
| 2               | 1/08          | In the Electrical Characteristics table, modified Note 2 and added Note 6 for $t_R$ , $t_F$ ; replaced package outline drawings with table. | 2, 8, 9       |

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