MB86930

SPARClite™ DRAM CONTROL INTERFACE

FUJITSU

APPLICATION NOTE 1

FUJITSU MICROELECTRONICS, INC.
ADVANCED PRODUCTS DIVISION

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INTRODUCTION

This application outlines the design used on the Fujitsu SPARClite™ Evaluation Board to interface the MB86930 with the DRAM subsystem. The main objective is to show the simplicity of the external design requirements, while still achieving high performance of three CPU cycle page mode access at 40 MHz.

The Bus Interface Unit (BIU) provides full 32-bit data and address buses. The separate data and address buses help in building fast systems. At the same time the on-chip circuitry like the address decoder, 16-bit timer, Chip Selects and Same Page Detect logic, reduce the external hardware requirements. The Same Page Detect output from the MB86930 allows designers to take advantage of the fast, consecutive accesses within Page Mode DRAM's like the MB81C1000 series. Address latches are not required because the address is provided by the MB86930 throughout a transaction.

The complete DRAM controller is implemented with a PAL16R8 and minimal external logic without resorting to expensive off-the-shelf DRAM controllers. A simplified block diagram for the memory interface logic is shown in Figure 1. A 40 MHz master clock is employed in this design.

DRAM

Figure 2 shows the complete schematic of the DRAM subsystem.

Four 8-bit wide DRAM SIMM modules are organized in parallel to provide 32-bit access. Parts with 80ns access time are chosen for availability and price advantages. Due to the 40 MHz design 70ns and 60ns devices do not provide any distinctive performance enhancement. 1 Meg and 4 Meg modules are supported giving total capacities of 4 MB and 16 MB, respectively. Jumpers are provided to mask address bit 12 as either a row or column address depending on the DRAM size.

Signals required by the DRAM as shown in Figure 2 are –RAS, –CAS<0:3>, –WE, RamAdr<10:0> and Data<31:0>. The generation and function of each signal will be presented in the following sections.

DRAM Address

Row and column addresses, RamAdr<10:0>, are multiplexed derivatives of the actual microprocessor addresses, ADR<23:2>. This design does not need external address latches as the addresses stay valid throughout the transaction. The R/C signal is generated by MEMPAL to select the inputs used for row or column address. The number of inputs to the multiplexer and the number of multiplexers will vary with the size of the memory. For instance, a memory system using 4 MB SIMM modules would use 22 address lines, ADR<2:23>, eleven for the row address and eleven for the column address, to address a total of 16 MB of 32-bit memory. Since the multiplexers can have either inverting or non-inverting outputs without affecting the system, the inverting device is chosen for superior speed and power dissipation characteristics.

Byte Enable

The Byte Enable signals, –BE<3:0>, from SPARClite are used during write cycles to indicate the data size being transferred and not used during read cycles. In this design these signals are gated with –CAS from MEMPAL to activate the proper DRAM module for access while the remaining DRAM module I/O's remain in tri-state which eliminates bus contention. This technique relieves the requirement of bi-directional transceivers which would introduce more stringent timing design considerations and extra cost.

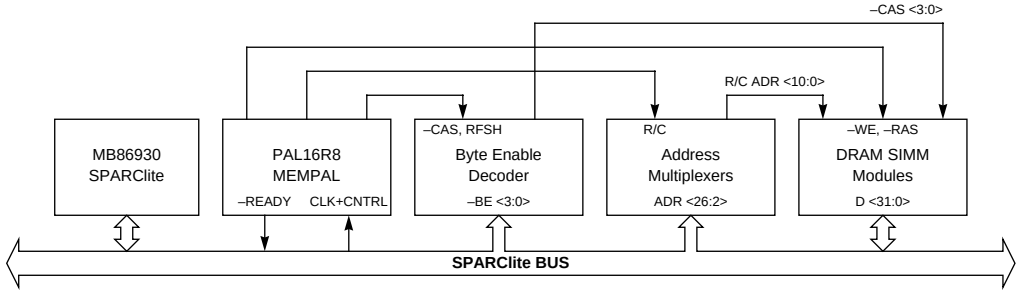

Figure 1. Simplified Block Diagram of DRAM Subsystem

DRAM Refresh

–CAS before –RAS refresh is employed in this example so no external address generation is needed. –WANT_R, a latched equivalent of TIMER_OVF (–RefREQ) from the processor, is used by the MEMPAL state machine to generate the state bit –RFSH. –WANT_R is latched to ensure that it stays active until the refresh request is serviced. –RFSH is gated with –CAS to activate all 4 SIMM modules during a refresh cycle. MEMPAL asserts –RAS, –CAS and –WE as required by the DRAM timing to perform a complete refresh.

MEMPAL

MEMPAL generates most of the control signals required to access the DRAM. As described above, R/C, –RAS, –CAS, –RFSH and –WE are needed for various tasks performed by the DRAM. Along with –RDY, they form a complete set of DRAM control signals. –RDY, equivalent to –READY of SPARClite, is used instead of the internal programmable wait state generator. This is due to the extra wait states needed for refresh in addition to the two different requirements for page mode and non page mode accesses.

–RAS, –CAS, R/C, –RDY and –RFSH are state bits of the state diagram shown in Figure 3. An extra state bit, Q, is used to distinguish between the PC2 and Idle states which are otherwise identical. –WE is a registered signal derived from the SPARClite R/W output. Figure 4, the ABEL™ file for MEMPAL, contains all of the logic equations.

From the state diagram and logic equations the timing of the synchronous DRAM subsystem can be derived. Figures 5 and 6 are examples of random reads and page mode reads respectively. The clock period is 25ns for the 40 MHz system. Clearly, from Figures 5 and 6, the timing requirements of 80ns DRAM are met. These figures also illustrate that page mode access requires three clock cycles and the worst case random access requires eight clock cycles. Timing diagrams of other cycles can be produced, from the state diagrams and

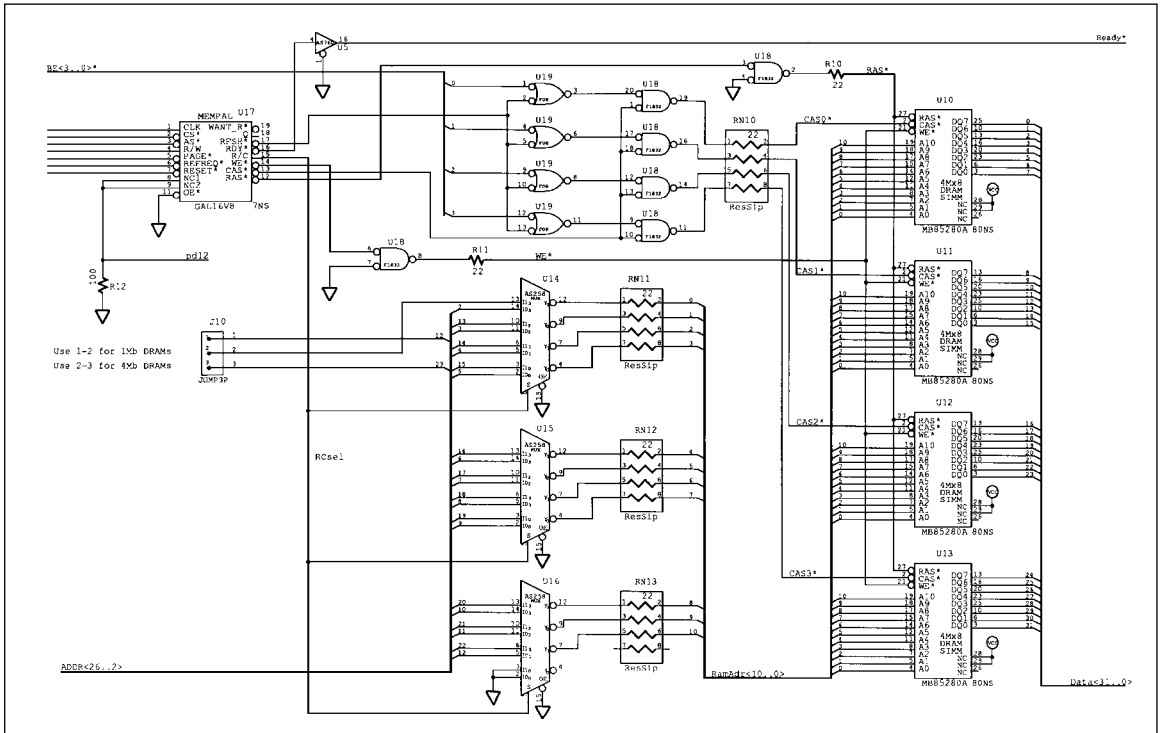

Figure 2. DRAM Subsystem Schematic

logic equations, by the user to confirm proper timing relationships.

The drivers used to buffer the raw signals from MEMPAL are optional depending on the loading requirements. In this design, all signals with more than one load are buffered.

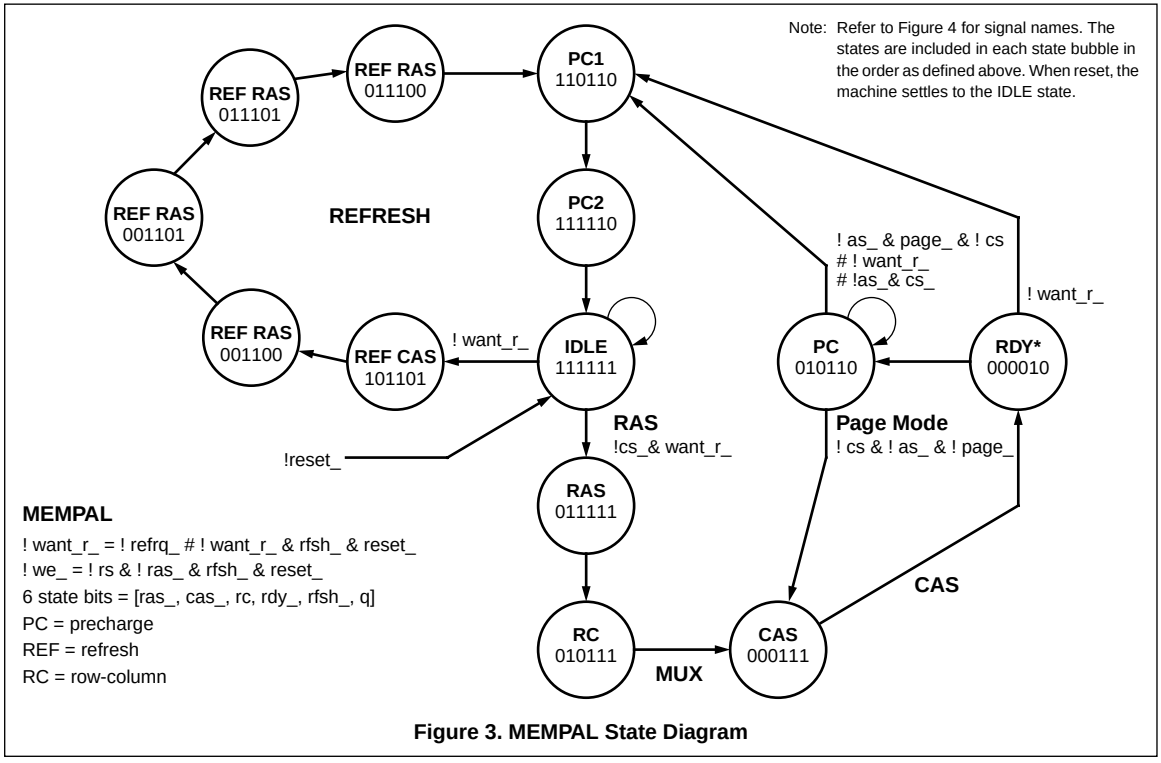

Figure 3. MEMPAL State Diagram

```
module mempal5
title 'Memory Controller for SPARClite'

mempalc device 'P16V8R';

"inputs
clk pin 1;
cs_ pin 2;
as_ pin 3;
rw pin 4;
page_ pin 5;
refrq_ pin 6;
reset_ pin 7;
oe_ pin 11;
vcc pin 20;
gnd pin 10;

"outputs
ras_ pin 12 istype 'reg,invert';
cas_ pin 13 istype 'reg,invert';
we_ pin 14 istype 'invert';
rc pin 15 istype 'reg,invert';
rdy_ pin 16 istype 'reg,invert';
rfsh_ pin 17 istype 'reg,invert';
q pin 18 istype 'reg,invert';
want_r_ pin 19 istype 'reg,invert';
@dcset;
x = .x.;

mem_state = [ras_, cas_, rc, rdy_, rfsh_, q];
"states
prechar1 = ^b110110;
prechar2 = ^b111110;
idle = ^b111111;
ras = ^b011111;
rowcol = ^b010111;
rowcolp = ^b010110;
cas = ^b000111;
ready = ^b000010;
refcas = ^b101101;
refras1 = ^b001100;
refras2 = ^b001101;
refras3 = ^b011101;
refras4 = ^b011100;

equations
"This version has the more efficient page mode and also
" has WE combinatorial instead of reg.
[want_r_,mem_state].C = clk;
```

Figure 4. ABEL file for MEMPAL

```
!want_r_ := !refrq_ # !want_r_.fb & rfsh_.fb & reset_;

!we_ = !rw & !ras_.fb & rfsh_.fb & reset_;


state_diagram mem_state

state prechar1:
 if (!reset_) then idle
 else prechar2;

state prechar2:
 goto idle;

state idle:
 if (!reset_) then idle
 else if (!want_r_.fb) then refcas
 else if (!cs_ & want_r_.fb) then ras
 else idle;

state ras:
 if (!reset_) then idle
 else rowcol;

state rowcol:
 if (!reset_) then idle
 else cas;

state cas:
 if (!reset_) then idle
 else ready;

state ready:
 if (!reset_) then idle
 else if (!want_r_.fb) then prechar1
 else rowcolp;

state rowcolp:
 if (!reset_) then idle
 else if (!want_r_.fb # !as_ & !cs_ & page_
 # !as_ & cs_) then prechar1
 else if (!as_ & !cs_ & !page_) then cas;
 else rowcolp;

state refcas:
 if (!reset_) then idle
 else refras1;

state refras1:
```

Figure 4. ABEL file for MEMPAL (continued)

```
 if (!reset_) then idle
 else refras2;

state refras2:
 if (!reset_) then idle
 else refras3;

state refras3:
 if (!reset_) then idle
 else refras4;

state refras4:
 if (!reset_) then idle
 else prechar1;

test_vectors(
[clk,cs_,as_,rw,page_,refrq_,reset_]->[ras_,cas_,we_,rc,rdy_,rfsh_,q,want_r_])
[.c., 1 , 1 , 1, 1 , 1 , 0 ]->[ x , x , x , x, x , x ,x, x ];
[.c., 1 , 1 , 1, 1 , 1 , 0 ]->[ 1 , 1 , 1 , 1, 1 , 1 ,1, 1 ];
[.c., 1 , 1 , 1, 1 , 1 , 1 ]->[ 1 , 1 , 1 , 1, 1 , 1 ,1, 1 ];
[.c., 1 , 0 , 0, 1 , 1 , 1 ]->[ 1 , 1 , 1 , 1, 1 , 1 ,1, 1 ];
[.c., 1 , 1 , 1, 1 , 1 , 1 ]->[ 1 , 1 , 1 , 1, 1 , 1 ,1, 1 ];
[.c., 0 , 0 , 0, 1 , 1 , 1 ]->[ 0 , 1 , 0 , 1, 1 , 1 ,1, 1 ];
[.c., 0 , 1 , 0, 1 , 1 , 1 ]->[ 0 , 1 , 0 , 0, 1 , 1 ,1, 1 ];
[.c., 0 , 1 , 0, 1 , 1 , 1 ]->[ 0 , 0 , 0 , 0, 1 , 1 ,1, 1 ];
[.c., 0 , 1 , 0, 1 , 0 , 1 ]->[ 0 , 0 , 0 , 0, 0 , 1 ,0, 0 ];
[.c., 0 , 1 , 0, 1 , 1 , 1 ]->[ 1 , 1 , 1 , 0, 1 , 1 ,0, 0 ];
[.c., 1 , 1 , 1, 1 , 1 , 1 ]->[ 1 , 1 , 1 , 1, 1 , 1 ,0, 0 ];
[.c., 1 , 1 , 1, 1 , 1 , 1 ]->[ 1 , 1 , 1 , 1, 1 , 1 ,1, 0 ];
[.c., 1 , 1 , 1, 1 , 1 , 1 ]->[ 1 , 0 , 1 , 1, 1 , 0 ,1, 0 ];
[.c., 1 , 1 , 1, 1 , 1 , 1 ]->[ 0 , 0 , 1 , 1, 1 , 0 ,0, 1 ];
[.c., 1 , 1 , 1, 1 , 1 , 0 ]->[ 1 , 1 , 1 , 1, 1 , 1 ,1, 1 ];

end mempal5
```

Figure 4. ABEL file for MEMPAL (continued)

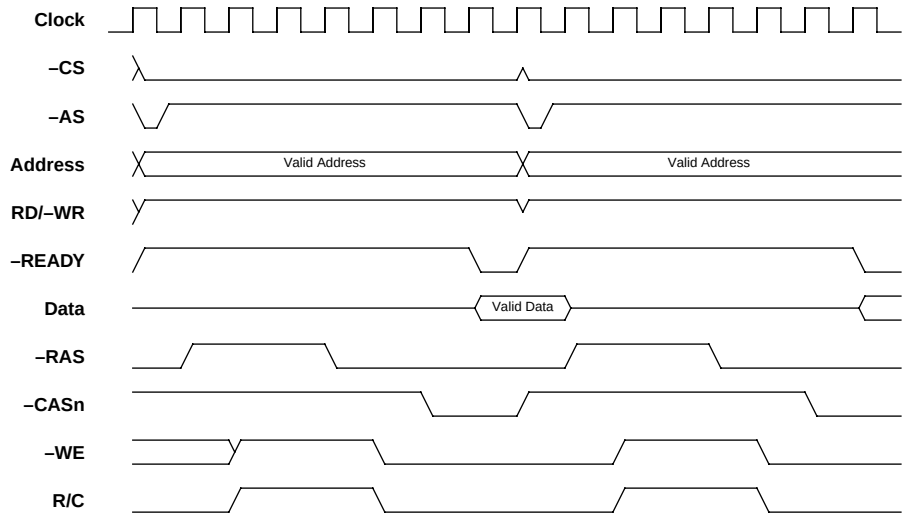

Figure 5. Worst Case Random Read Cycle

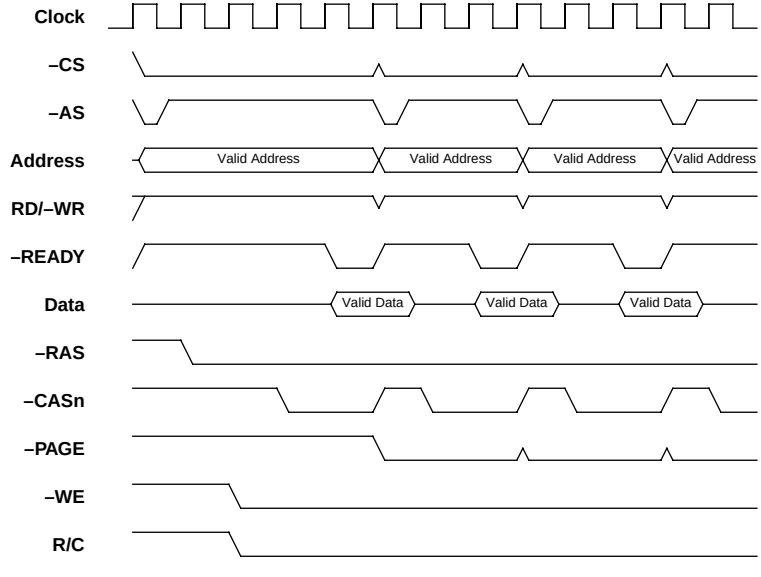

Figure 6. Page Mode Read Cycle

SPARClite SIGNAL DESCRIPTIONS

The MB86930 signals used by MEMPAL and the rest of the DRAM subsystem are listed below with usage explanations. Consult the MB86930 data sheet for a comprehensive discussion of all the signals. The signals are named as in the data sheet with the MEMPAL names in parenthesis.

Signal Name	Description
–CS4 (–CS)	**CHIP SELECT:** This is one of six chip select outputs asserted when the value of the address, including ASI, matches one of the pre-programmed corresponding address range registers. In this case, the range is chosen to be the DRAM. This feature eliminates the need to decode high order bits, for selecting memory mapped subsystems, which traditionally requires a large number of external support logic. The address ranges are software programmable which provides flexibility and convenience to the system designer who can map devices into different locations without modifying the hardware.
–AS (–AS)	**ADDRESS STROBE:** This is a control signal asserted by the microprocessor to indicate the start of a bus transaction.
–READY (–RDY)	**DATA READY:** This is a control signal asserted by the external subsystem to indicate that it is ready to receive data or to indicate that valid data is on the bus. In this case, MEMPAL generates this signal for the DRAM subsystem.
–PAGE_DET (–PAGE)	**SAME PAGE DETECT:** This signal indicates consecutive accesses within a programmable size page. The –PAGE_DET is asserted with –AS and remains active for the entire bus cycle. MEMPAL uses this as an indicator of page mode access. Software update is the only requirement to utilize different page sizes once the hardware is designed.
–BE<3:0> (–BE<3..0>)	**BYTE ENABLE:** These signals specify which bytes are transferred during a write cycle. They are available in the same cycle in which the corresponding address value is asserted on the bus. In this design, these signals are used very intelligently to eliminate the need for bidirectional buffers, on the CPU data bus, which will add considerable cost to the design. By gating these signals with –CAS, the unused I/O's are assured to be in tri-state. This helps to avoid two problems. First, the DRAM I/O will not contend with a CPU write. Second, erroneous data is prevented from being written into memory.
RD/–WR (R/W)	**READ/–WRITE:** This control signal indicates whether the transaction being performed is a READ or a WRITE. When high the chip is performing a READ. When low the chip is performing a WRITE.
–TIMER_OVF (–RefREQ)	**TIMER OVERFLOW:** This signal is asserted by the processor to indicate that the internal 16-bit timer has overflowed. It can be useful for DRAM refresh or other functions which requires periodical pulses. The timer automatically reloads itself and the value loaded is programmable. The software programmable feature is advantageous for custom designs which requires specific timing intervals. In this design, it is used to indicate that a DRAM refresh is due. The timer is set to provide refresh intervals more than eight cycles prior to the maximum allowed refresh time of the DRAM. This ensures proper refresh in the worst case which takes eight states for refresh to occur (See Figure 3).

MEMPAL SIGNAL DESCRIPTIONS

The MEMPAL outputs, defined in Figure 2, which control the activity on the memory are described below.

Signal Name	Description
–RAS	**ROW ADDRESS STROBE:** This is the DRAM input used to strobe in the row address. In general it starts a memory cycle with the exception of –CAS before –RAS refresh, in which case the –CAS signal appears first.
–CAS	**COLUMN ADDRESS STROBE:** This is gated with –RFSH and –BE<3:0> to produce the DRAM –CAS inputs used to strobe in the column address. In general it is asserted after the row address strobe, –RAS. The exception occurs during –CAS before –RAS refresh, in which case it is asserted before –RAS.
–WE	**WRITE ENABLE:** This is the DRAM input used to signify a Write cycle.
R/C	**ROW/COLUMN SELECT:** This signal selects which multiplexer data input to send to the output. The 2:1 multiplexing selects half of the inputs as row and the other half as column addresses.
–RDY	**READY:** This signal is an input to SPARClite signifying that data is available from or already received by the DRAM.
–RFSH	**REFRESH:** This signal, gated with –CAS, selects all 4 SIMM modules for refresh.

DISCUSSION

This design example illustrates the ease of interfacing a DRAM subsystem to the MB86930. Along with this ease in design effort, the part count and complexity are reduced. The user can also trade speed for less complexity and more flexibility by using the internal wait state generator.

At 40 MHz, the CPU can access page mode data in 75ns, achieving data throughput rate of over 53 MB/s. This, coupled with the outstanding instruction execution rate, should provide excellent processing power for high-end embedded applications.

Systems with slower clock rates can modify the MEMPAL to minimize the number of cycles needed for each DRAM task as long as the timing constraints of the DRAM and SPARClite are not violated. For example, page mode access in a 25 MHz system can be done in 2 CPU cycles rather then 3. If the internal wait state generator is used, a software revision is also needed to accommodate the change in wait state configuration.

The DRAM can be mapped to different parts of the CPU memory space simply by changing the corresponding address range register contents. Changing the page size can be accomplished as easily. This could imply minimal or no hardware changes when the system design is changed.

In summary, the SPARClite architecture provides many flexible options in I/O interfacing. This will enable design changes to meet the extreme time-to-market demands of today's competitive business climate.

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