LMH6672 Dual, High Output Current, High Speed Op Amp

Check for Samples: LMH6672

FEATURES

- **High Output Drive**
  - **19.2 V_{PP} Differential Output Voltage, R_L = 50Ω**
  - **9.6 V_{PP} Single-ended Output Voltage, R_L = 25Ω**
- **High Output Current**
  - **±200 mA @ V_O = 9 V_{PP}, V_S = 12V**
- **Low Distortion**
  - **105 dB SFDR @ 100 kHz, V_O = 8.4 V_{PP}, R_L = 25Ω**
  - **98 dB SFDR @ 1MHz, V_O = 2 V_{PP}, R_L = 100Ω**
- **High Speed**
  - **90 MHz 3 dB Bandwidth (G = 2)**
  - **135 V/µs Slew Rate**
- **Low Noise**
  - **3.1 nV/√Hz: Input Noise Voltage**
  - **1.8 pA/√Hz: input noise current**
- **Low Supply Current: 7.2mA/amp**
- **Single-supply Operation: 5V to 12V**
- **Available in 8-pin SOIC and SO PowerPAD (DDA)**

APPLICATIONS

- **ADSL PCI Modem Cards**
- **xDSL External Modems**
- **Line Drivers**

DESCRIPTION

The LMH6672 is a low cost, dual high speed op amp capable of driving signals to within 1V of the power supply rails. It features the high output drive with low distortion required for the demanding application of a single supply xDSL line driver.

When connected as a differential output driver, the LMH6672 can drive a 50Ω load to 16.8 V_{PP} swing with only −98 dBc distortion, fully supporting the peak upstream power levels for upstream full-rate ADSL. The LMH6672 is fully specified for operation with 5V and 12V supplies. Ideal for PCI modem cards and xDSL modems.

Connection Diagram and Typical Application

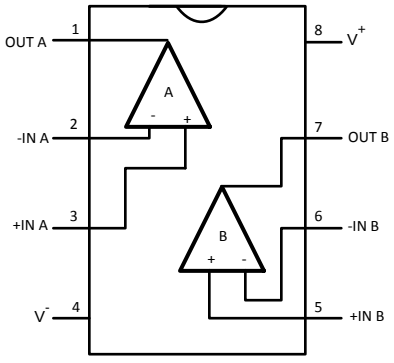

Figure 1. 8-Pin SOIC / SO PowerPAD (DDA) (Top View)

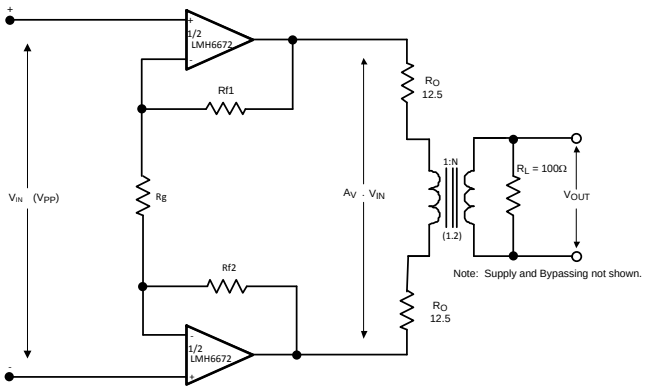

Figure 2. Typical Application

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)

ESD Tolerance(2)	Human Body Model	2kV
	Machine Model	200V
V_{IN} Differential		±1.2V
Output Short Circuit Duration		See(3)
Supply Voltage ($V^+ - V^-$)		13.2V
Voltage at Input/Output pins		V^+ +0.8V, V^- −0.8V
Storage Temperature Range		−65°C to +150°C
Junction Temperature		+150°C (4)
Soldering Information	Infrared or Convection (20 sec)	235°C
	Wave Soldering (10 sec)	260°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics.
(2) Human body model, 1.5kΩ in series with 100pF. Machine model, 200Ω in series with 100pF.
(3) Shorting the output to either supply or ground will exceed the absolute maximum T_J and can result in failure.
(4) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA} and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly onto a PC board.

Operating Ratings(1)

Supply Voltage ($V^+ - V^-$)	±2.5V to ±6.5V
Junction Temperature Range	−40°C to 150°C
Package Thermal Resistance (θ_{JA})	
8-pin SOIC	172°C/W
8-pin SO PowerPAD (DDA)	58.6°C/W

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics.

Electrical Characteristics

T_J = 25°C, G = +2, V_S = ±2.5 to ±6V, R_F = R_{IN} = 470Ω, R_L = 100Ω; Unless otherwise specified.

Symbol	Parameter	Conditions	Min(1)	Typ(2)	Max(1)	Units
Dynamic Performance						
	−3dB Bandwidth			90		MHz
	0.1dB Bandwidth	V_S = ±6V		12		MHz
	Slew Rate	V_S = ±6V, 4V Step, 10-90%		135		V/µs
	Rise and Fall Time	V_S = 6V, 4V Step, 10-90%		23.5		ns
Distortion and Noise Response						
	2nd Harmonic Distortion	V_O = 8.4 V_{PP}, f = 100 kHz, R_L = 25Ω		−105		dBc
		V_O = 8.4 V_{PP}, f = 1 MHz, R_L = 100Ω		−90		dBc
	3rd Harmonic Distortion	V_O = 8.4 V_{PP}, f = 100 kHz, R_L = 25Ω		−110		dBc
		V_O = 8.4 V_{PP}, f = 1 MHz, R_L = 100Ω		−87		dBc
	Input Noise Voltage	f = 100 kHz		3.1		nV/√Hz
	Input Noise Current	f = 100 kHz		1.8		pA/√Hz
Input Characteristics						
V_{OS}	Input Offset Voltage	T_J = −40°C to 125°C	−5.5	0.1	5.5	mV
			−4	−0.2	4	
I_B	Input Bias Current	T_J = −40°C to 125°C		8	16	µA
I_{OS}	Input Offset Current	T_J = −40°C to 125°C	−2.1	0	2.1	µA
CMVR	Common Voltage Range	V_S = ±6V	−6.0	−5.7 to 4.5	4.5	V
CMRR	Common-Mode Rejection Ratio	V_S = ±6V, T_J = −40°C to 125°C	150	7.5		µV/V
Transfer Characteristics						
A_{VOL}	Voltage Gain	R_L = 1k, T_J = −40°C to 125°C	1.0	5		V/mV
		R_L = 25Ω, T_J = −40°C to 125°C	0.67	3.4		V/mV
V_O	Output Swing	R_L = 25Ω, V_S = ±6V	−4.5	±4.8	4.5	V
		R_L = 25Ω, T_J = −40°C to 125°C, V_S = ±6V	−4.4	±4.8	4.4	
V_O	Output Swing	R_L = 1k, V_S = ±6V	−4.8	±4.8	4.8	V
		R_L = 1k, T_J = −40°C to 125°C, V_S = ±6V	−4.7	±4.8	4.7	
I_{SC}	Output Current(3)	V_O = 0, V_S = ±6V	350	525		mA
		V_O = 0, V_S = ±6V, T_J = −40°C to 125°C	260	600		mA
Power Supply						
I_S	Supply Current/Amp	V_S = ±6V			8	mA
		V_S = ±6V, T_J = −40°C to 125°C		7.2	9	
PSRR	Power Supply Rejection Ratio	V_S = ±2.5V to ±6V, T_J = −40°C to 125°C	72	88.5		dB

(1) All limits are specified by testing, characterization or statistical analysis.
(2) Typical values represent the most likely parametric norm.
(3) Shorting the output to either supply or ground will exceed the absolute maximum T_J and can result in failure.

±2.5V Electrical Characteristics

T_J = 25°C, G = +2, V_S = ±2.5 to ±6V, R_F = R_{IN} = 470Ω, R_L = 100Ω; Unless otherwise specified.

Symbol	Parameter	Conditions	Min(1)	Typ(2)	Max(1)	Units
Dynamic Performance						
	−3 dB Bandwidth			80		MHz
	0.1 dB Bandwidth			12		MHz
	Slew Rate	2V Step, 10-90%		15		V/µs
	Rise and Fall Time	2V Step, 10-90%		14		ns
Distortion and Noise Response						
	2nd Harmonic Distortion	V_O = 2 V_{PP}, f = 100 kHz, R_L = 25Ω		−96		dBc
		V_O = 2 V_{PP}, f = 1 MHz, R_L = 100Ω		−85		dBc
	3rd Harmonic Distortion	V_O = 2 V_{PP}, f = 100 kHz, R_L = 25Ω		−98		dBc
		V_O = 2 V_{PP}, f = 1 MHz, R_L = 100Ω		−87		dBc
Input Characteristics						
V_{OS}	Input Offset Voltage	T_J = −40°C to 125°C	−5.5		5.5	mV
			−4.0	0.02	4.0	
I_B	Input Bias Current	T_J = −40°C to 125°C		8.0	16	µA
CMVR	Common-Mode Voltage Range		−2.5		1.0	V
CMRR	Common-Mode Rejection Ratio	T_J = −40°C to 125°C	150	8		µV/V
Transfer Characteristics						
A_{VOL}	Voltage Gain	R_L = 25Ω, T_J = −40°C to 125°C	0.67	3		V/mV
		R_L = 1k, T_J = −40°C to 125°C	1.0	4		
Output Characteristics						
V_O	Output Voltage Swing	R_L = 25Ω	1.20	1.45		V
		R_L = 25Ω, T_J = −40°C to 125°C	1.10	1.35		
		R_L = 1k	1.30	1.60		
		R_L = 1k, T_J = −40°C to 125°C	1.25	1.50		
Power Supply						
I_S	Supply Current/Amp				8.0	mA
		T_J = −40°C to 125°C		6.7	9.0	

(1) All limits are specified by testing, characterization or statistical analysis.
(2) Typical values represent the most likely parametric norm.

Typical Performance Characteristics

Output Swing R_L = 25Ω, 1 kΩ @ −40°C, 25°C, 85°C

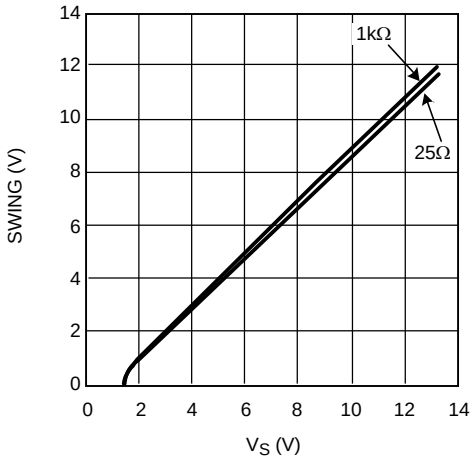

Figure 3.

Positive Output Swing into 1kΩ

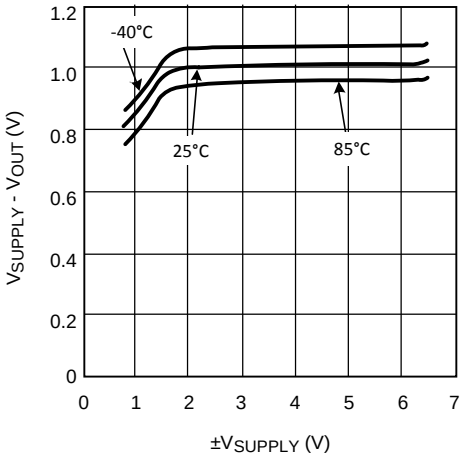

Figure 4.

Negative Output Swing into 1 kΩ

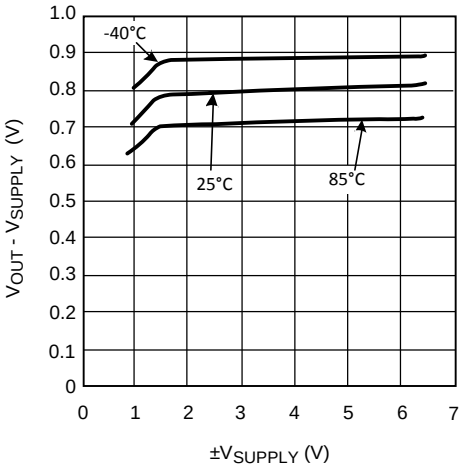

Figure 5.

Positive Output Swing into 25Ω

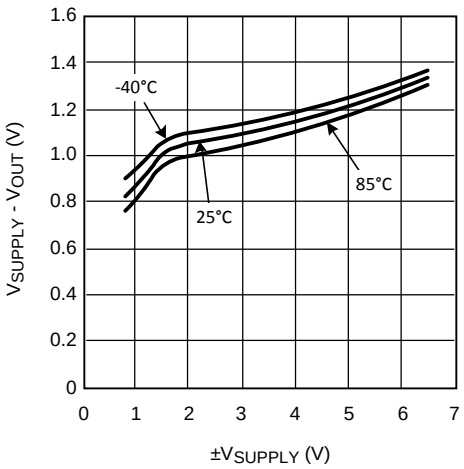

Figure 6.

Negative Output Swing into 25Ω

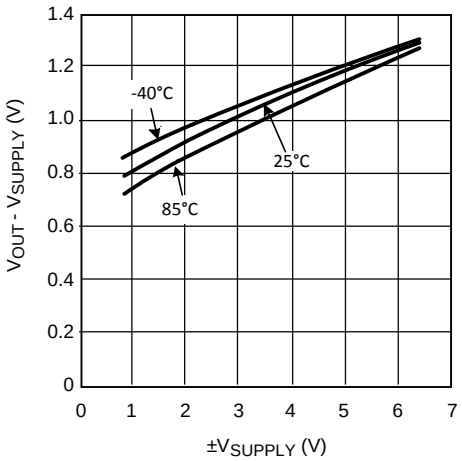

Figure 7.

$+V_{OUT}$ vs. I_{LOAD}

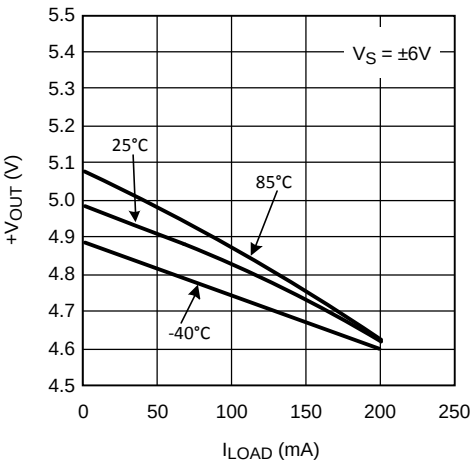

Figure 8.

Typical Performance Characteristics (continued)

$-V_{OUT}$ vs. I_{LOAD}

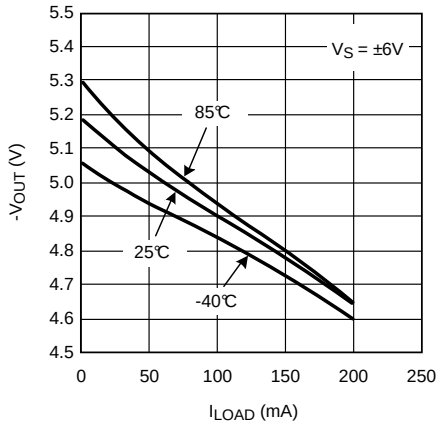

Figure 9.

$+V_{OUT}$ vs. I_{LOAD}

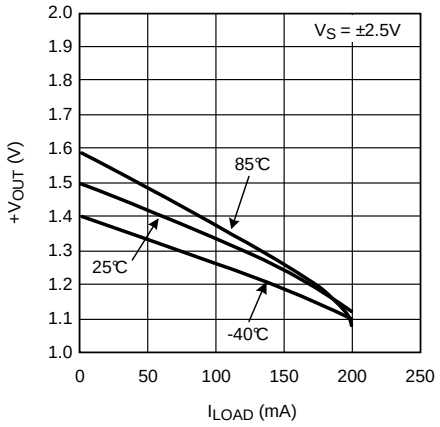

Figure 10.

$-V_{OUT}$ vs. I_{LOAD}

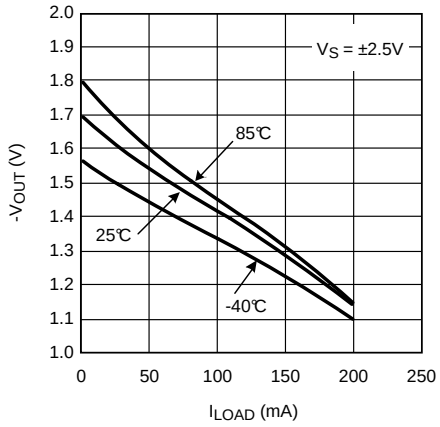

Figure 11.

Supply Current vs. Supply Voltage

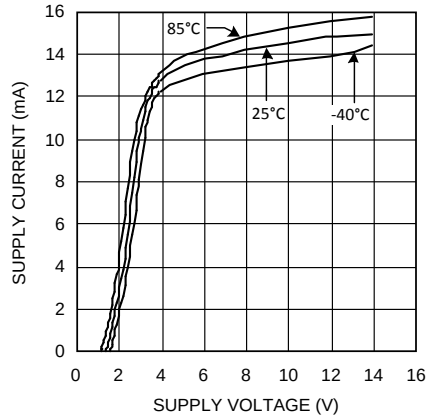

Figure 12.

Sourcing Current vs. Supply Voltage

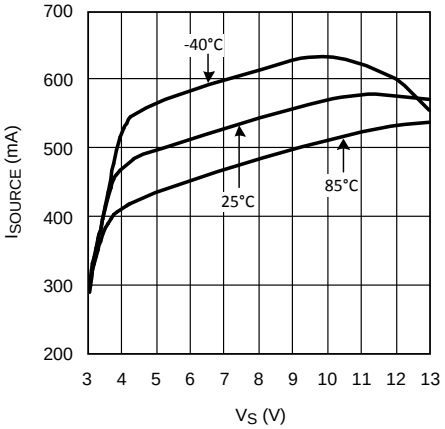

Figure 13.

Sinking Current vs. Supply Voltage

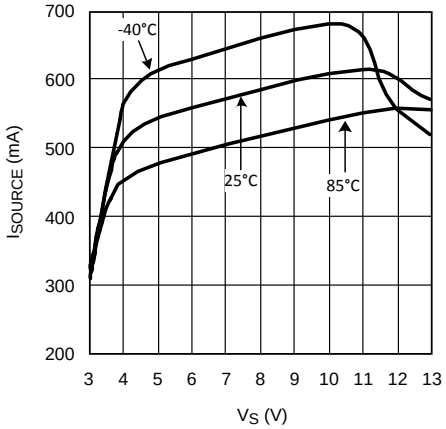

Figure 14.

Typical Performance Characteristics (continued)

V_{OS} vs. V_S

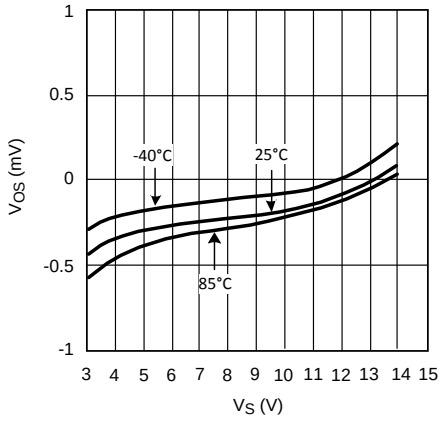

Figure 15.

V_{OS} vs. V_{CM}, V_S = 12V

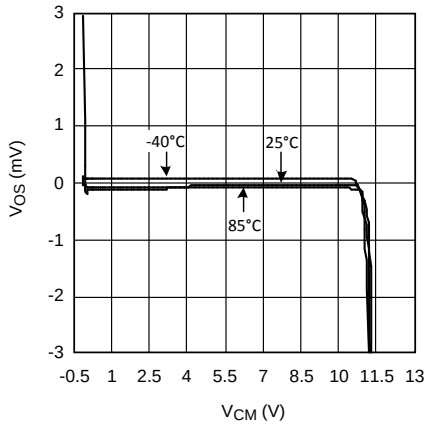

Figure 16.

V_{OS} vs. V_{CM}, V_S = 5V

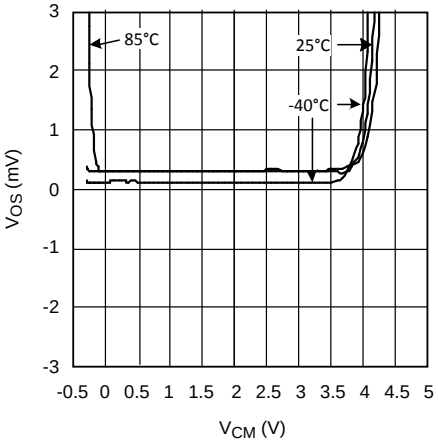

Figure 17.

Bias Current vs. V_{SUPPLY}

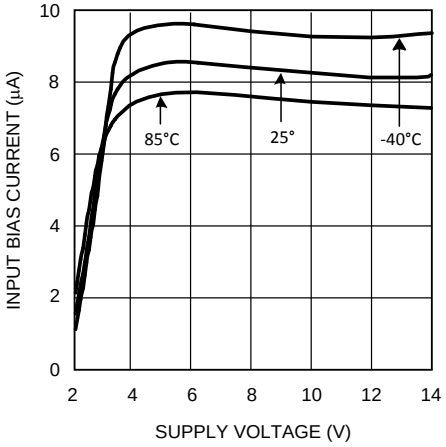

Figure 18.

Offset Current vs. V_{SUPPLY}

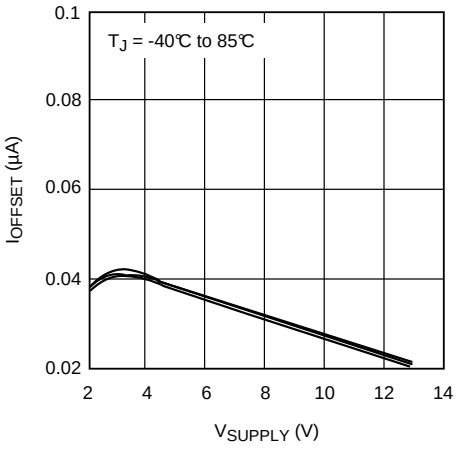

Figure 19.

V_{OUT} vs. V_{IN}

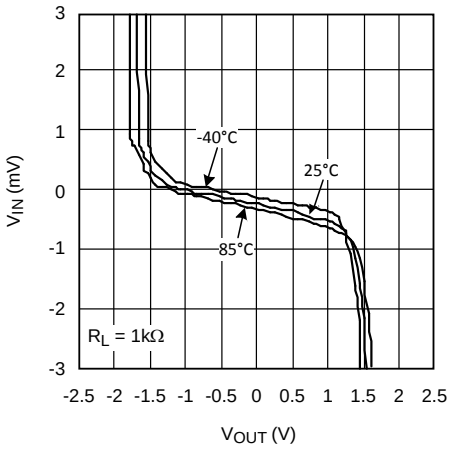

Figure 20.

Typical Performance Characteristics (continued)

V_{OUT} vs. V_{IN}

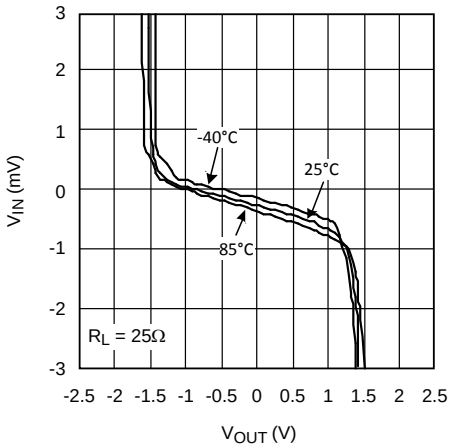

Figure 21.

Harmonic Distortion vs. Load

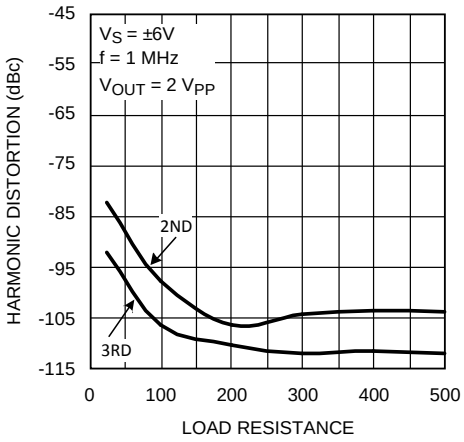

Figure 22.

Harmonic Distortion vs. Load

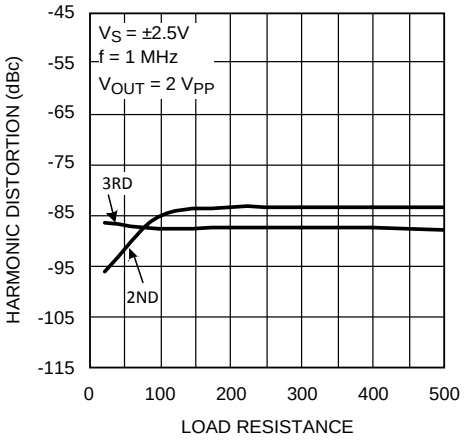

Figure .

Harmonic Distortion vs. Output Voltage

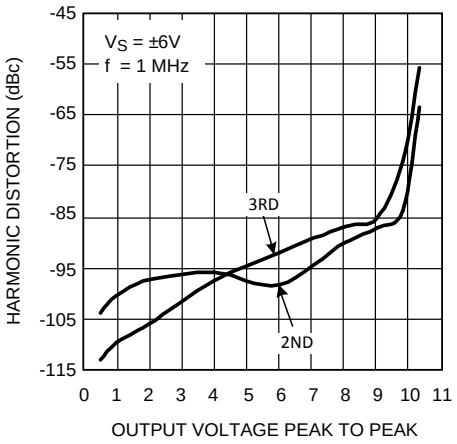

Figure 23.

Harmonic Distortion vs. Output Voltage

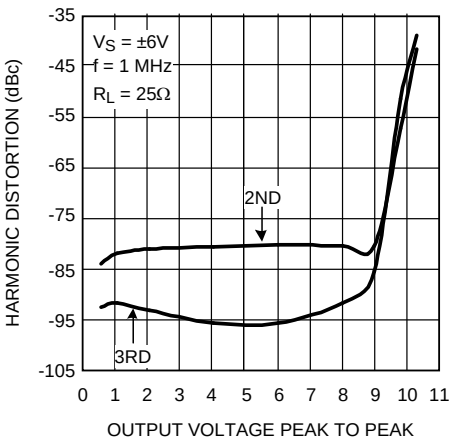

Figure 24.

Harmonic Distortion vs. Output Voltage

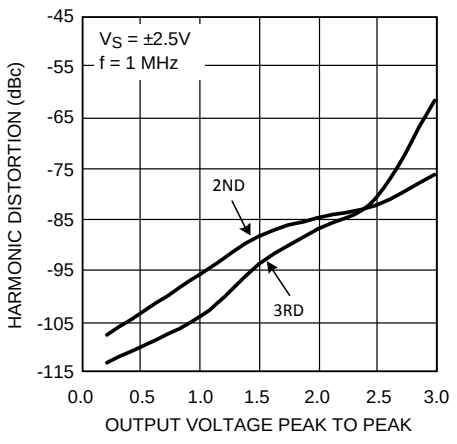

Figure 25.

Typical Performance Characteristics (continued)

Harmonic Distortion vs. Output Voltage

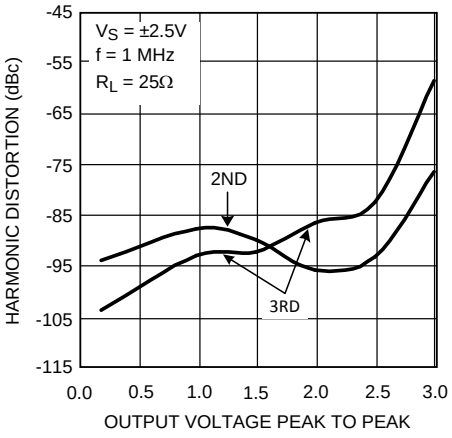

Figure 26.

Harmonic Distortion vs. Output Voltage

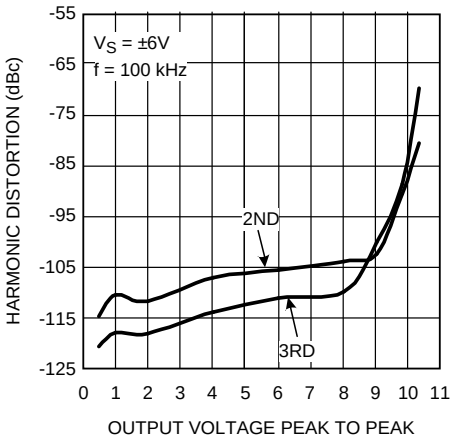

Figure 27.

Harmonic Distortion vs. Output Voltage

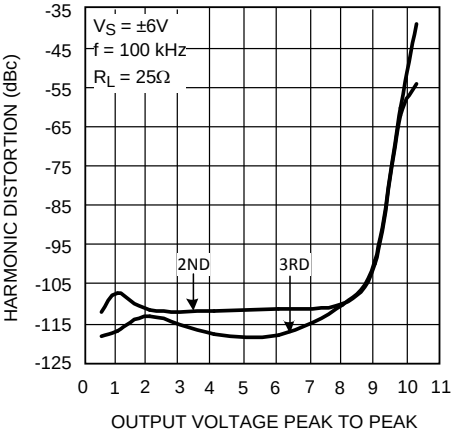

Figure 28.

Harmonic Distortion vs. Frequency

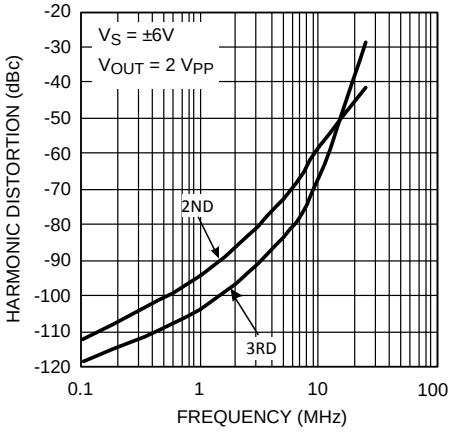

Figure 29.

Harmonic Distortion vs. Frequency

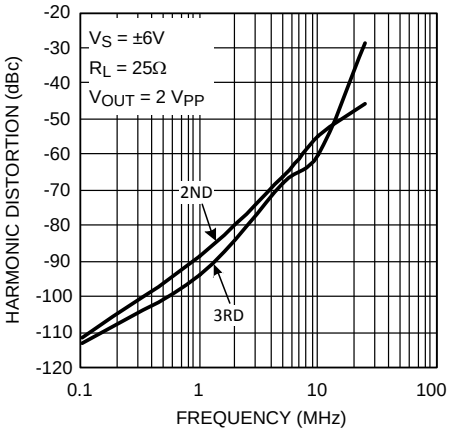

Figure 30.

Harmonic Distortion vs. Frequency

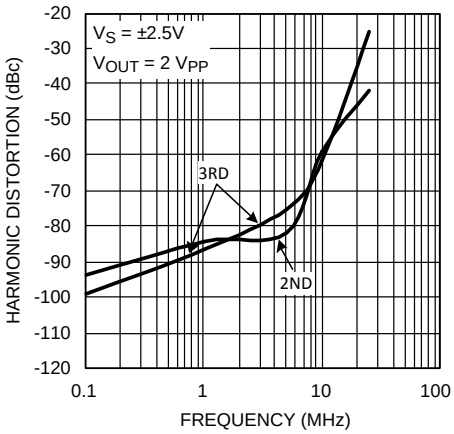

Figure 31.

Typical Performance Characteristics (continued)

Harmonic Distortion vs. Frequency

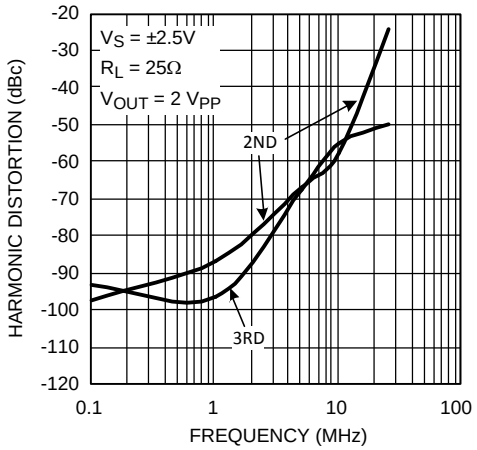

Figure 32.

Pulse Response, V_S= ±6V

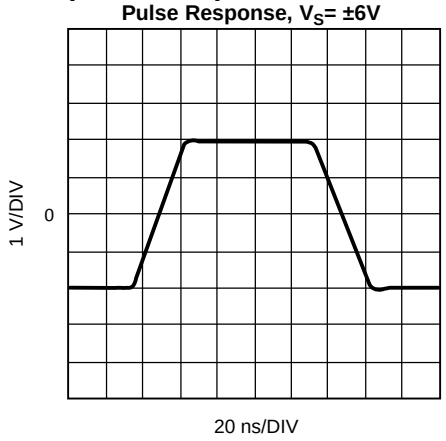

Figure 33.

Pulse Response, V_S= ±2.5V, ±6V

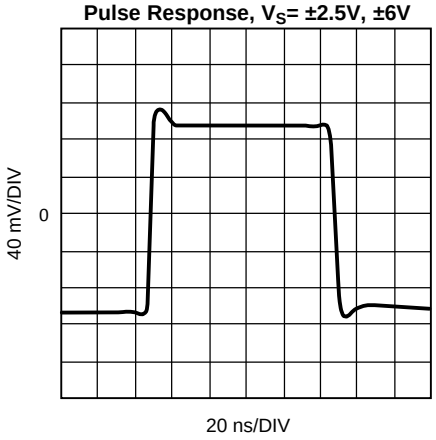

Figure 34.

Pulse Response, A_{VCL} = −1, V_S= ±6V

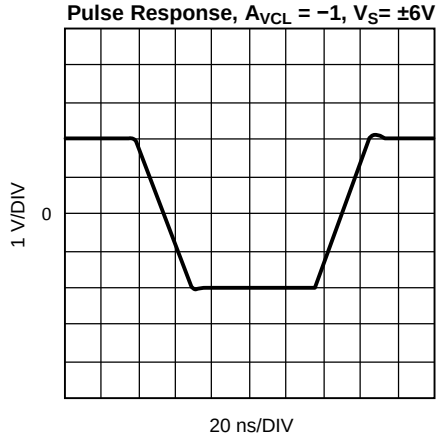

Figure 35.

Pulse Response, A_{VCL} = −1, V_S= ±2.5V, ±6V

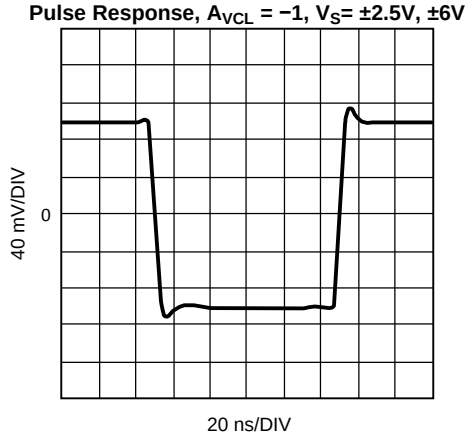

Figure 36.

Frequency Response

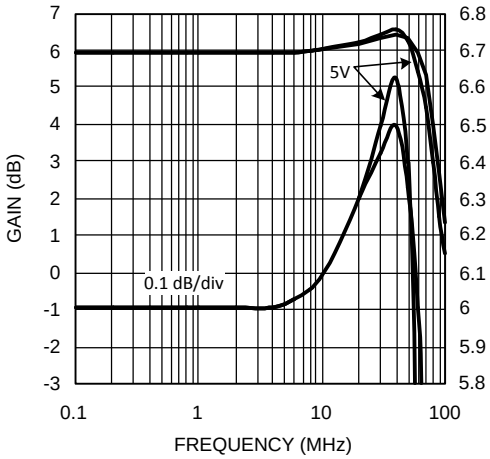

Figure 37.

Typical Performance Characteristics (continued)

Frequency Response, A_{VCL} = +5V

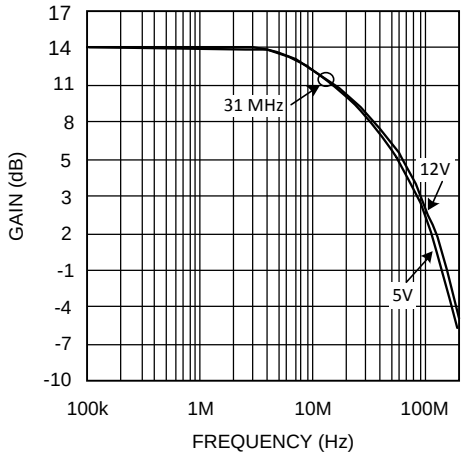

Figure 38.

Frequency Response, A_{VCL} = +10V

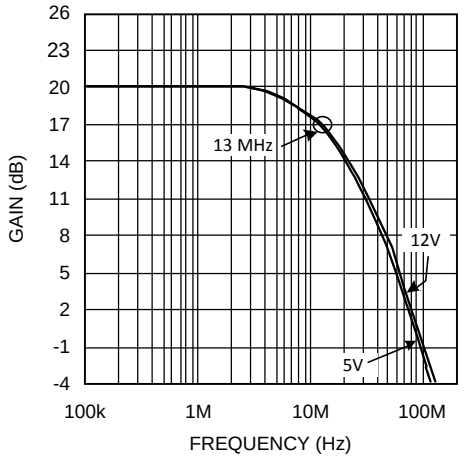

Figure 39.

CMRR vs. Frequency @ 12V

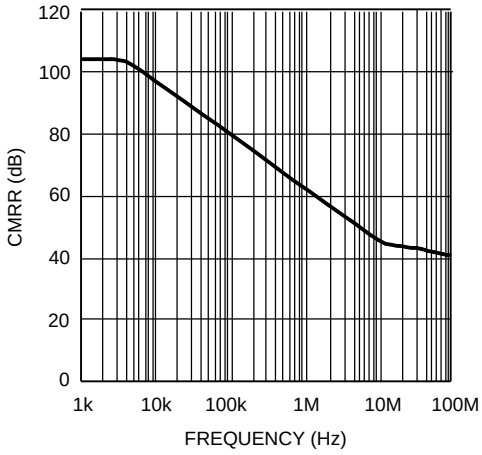

Figure 40.

CMRR vs. Frequency @ 5V

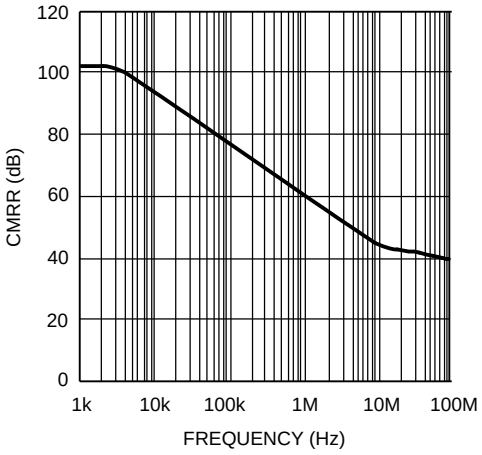

Figure 41.

PSRR+ vs. Frequency, V_S = 5V and 12V

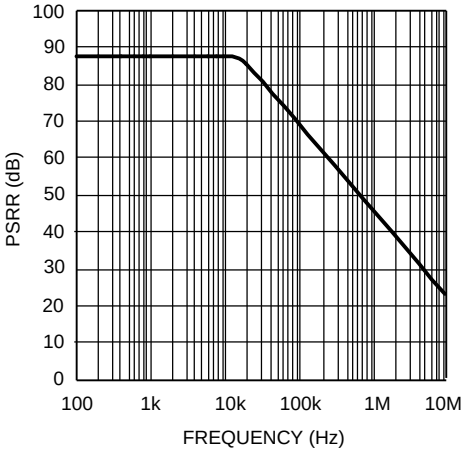

Figure 42.

PSRR− vs. Frequency V_S = 5V and 12V

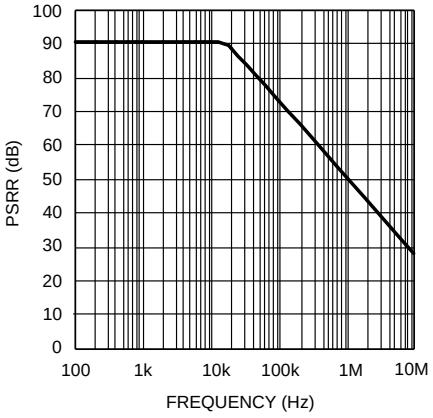

Figure 43.

Typical Performance Characteristics (continued)

e_n & i_n vs. Frequency, V_S = 5V and 12V

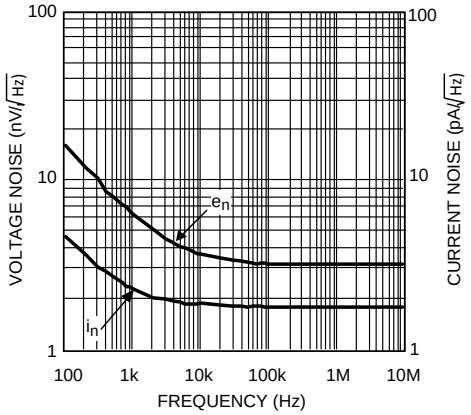

Figure 44.

Application Notes

THERMAL MANAGEMENT

The LMH6672 is a high-speed, high power, dual operational amplifier with a very high slew rate and very low distortion. For ease of use, it uses conventional voltage feedback. These characteristics make the LMH6672 ideal for applications where driving low impedances of 25-100Ω such as xDSL and active filters.

A class AB output stage allows the LMH6672 to deliver high currents to low impedance loads with low distortion while consuming low quiescent supply current. For most op-amps, class AB topology means that internal power dissipation is rarely an issue, even with the trend to smaller surface mount packages. However, the LMH6672 has been designed for applications where high levels of power dissipation may be encountered.

Several factors contribute to power dissipation and consequently higher junction temperatures. These factors need to be well understood if the LMH6672 is to perform to specifications in all applications. This section will examine the typical application shown in Figure 2, as an example. Because both amplifiers are in a single package, the calculations are for the total power dissipated by both amplifiers.

There are two separate contributors to the internal power dissipation:

1. The product of the supply voltage and the quiescent current when no signal is being delivered to the external load.
2. The additional power dissipated while delivering power to the external load.

The first of these components appears easy to calculate simply by inspecting the data sheet. The typical quiescent supply current for this part is 7.2 mA per amplifier, therefore, with a ±6 volt supply, the total power dissipation is:

$P_D = V_S \times 2 \times I_Q = 12 \times (14.4 \times 10^{-3}) = 173$ mW

($V_S = V_{CC} + V_{EE}$)

With a thermal resistance of 172°C/W for the SOIC package, this level of internal power dissipation will result in a junction temperature (T_J) of 30°C above ambient.

Using the worst-case maximum supply current of 18 mA and an ambient of 85°C, a similar calculation results in a power dissipation of 216 mW, or a T_J of 122°C.

This is approaching the maximum allowed T_J of 150°C before a signal is applied. Fortunately, in normal operation, this term is reduced, for reasons that will soon be explained.

The second contributor to high T_J is the power dissipated internally when power is delivered to the external load. This cause of temperature rise is more difficult to calculate, even when the actual operating conditions are known.

To maintain low distortion, in a Class AB output stage, an idle current, I_Q, is maintained through the output transistors when there is little or no output signal. In the LMH6672, about 4.8 mA of the total quiescent supply current of 14.4 mA flows through the output stages.

Under normal large signal conditions, as the output voltage swings positive, one transistor of the output pair will conduct the load current, while the other transistor shuts off, and dissipates no power. During the negative signal swing this situation is reversed, with the lower transistor sinking the load current while the upper transistor is cut off. The current in each transistor will approximate a half wave rectified version of the total load current.

Because the output stage idle current is now routed into the load, 4.8 mA can be subtracted from the quiescent supply current when calculating the quiescent power when the output is driving a load.

The power dissipation caused by driving a load in a DSL application, using a 1:2 turns ratio transformer driving 20 mW into the subscriber line and 20 mW into the back termination resistors, can be calculated as follows:

$P_{DRIVER} = P_{TOT} – (P_{TERM} + P_{LINE}$

Where

- P_{DRIVER} is the LMH6672 power dissipation
- P_{TOT} is the total power drawn from the power supply
- P_{TERM} is the power dissipated in the back termination resistors
- P_{LINE} is the power sent into the subscriber line
- At full specified power, $P_{TERM} = P_{LINE} = 20$ mW, $P_{TOT} = V_S \times I_S$ (1)

In this application, $V_S = 12V$.

$I_S = I_Q + A_{VG} |I_{OUT}|$.

I_Q = the LMH6672 quiescent current minus the output stage idle current.

$I_Q = 14.4 – 4.8 = 9.6$ mA

Average (A_{VG}) $|I_{OUT}|$ for a full-rate ADSL CPE application, using a 1:2 turns ratio transformer, is $\sqrt{(40\text{ mW}/50\Omega)}$ = 28.28 mA RMS.

For a Gaussian signal, which the DMT ADSL signal approximates, $A_{VG} |I_{OUT}| = \sqrt{2/\pi} \times I_{RMS}$ = 22.6 mA. Therefore, P_{TOT} = (22.6 mA + 9.6 mA) × 12V = 386 mW and P_{DRIVER} is 40 = 346 mW.

In the SOIC package, with a θ_{JA} of 172°C/W, this causes a temperature rise of 60°C. With an ambient temperature at the maximum recommended 85°C, the T_J is at 145°C, well below the specified 150°C maximum.

Even if we assume the absolute maximum I_S over temperature of 18 mA, when we scale up the I_Q proportionally to 7 mA, the P_{DRIVER} only goes up by 41 mW causing a 62°C rise to 147°C.

Although very few CPE applications will ever operate in an environment as hot as 85°C, if a lower T_J is desired or the LMH6672 is to be used in an application where the power dissipation is higher, the SO PowerPAD (DDA) package provides a much lower θ_{JA} of only 58.6°C/W. Using the same P_{DRIVER} as above, we find that the temperature rise is only 19° and 21°C, resulting in T_J's in an 85°C ambient of 104°C and 106°C respectively.

REVISION HISTORY

Changes from Revision F (March 2013) to Revision G	Page
• Changed layout of National Data Sheet to TI format	13

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMH6672MA/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMH6672MA	Samples
LMH6672MAX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMH6672MA	Samples
LMH6672MR/NOPB	ACTIVE	SO PowerPAD	DDA	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 85	LMH6672MR	Samples
LMH6672MRX/NOPB	ACTIVE	SO PowerPAD	DDA	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 85	LMH6672MR	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
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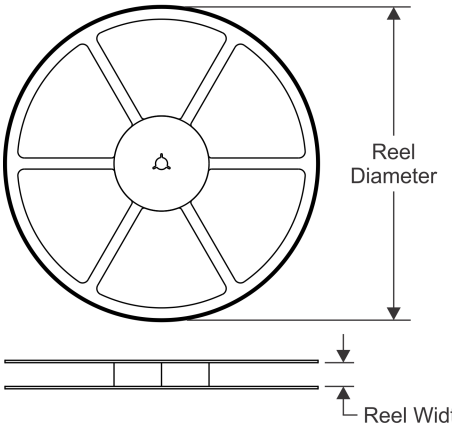
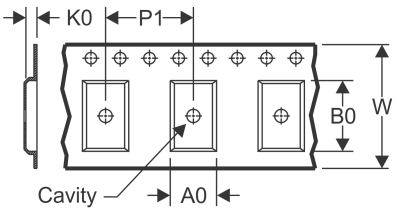
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

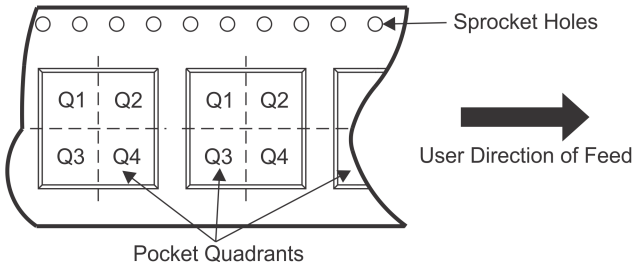


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

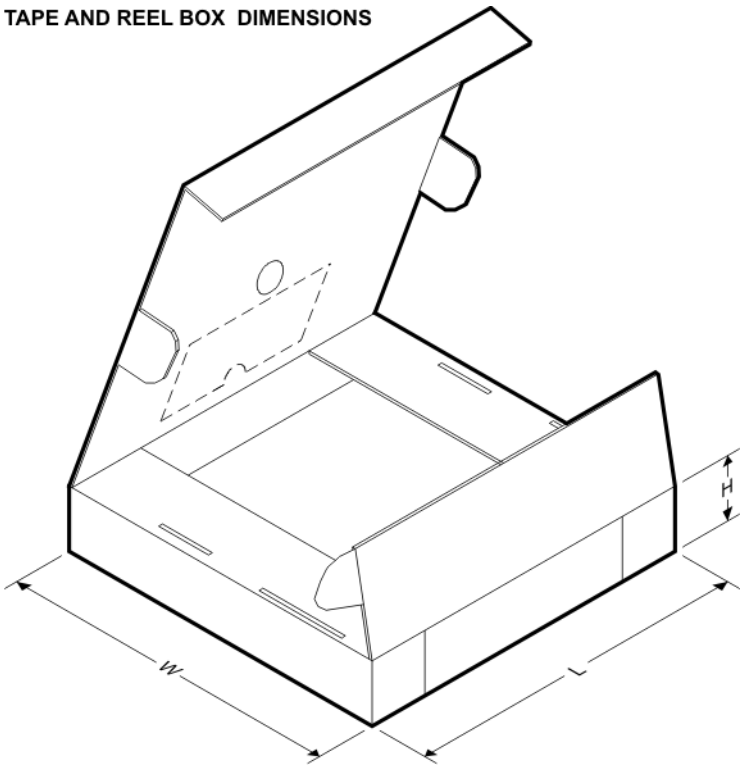
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMH6672MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMH6672MRX/NOPB	SO Power PAD	DDA	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMH6672MAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LMH6672MRX/NOPB	SO PowerPAD	DDA	8	2500	367.0	367.0	35.0

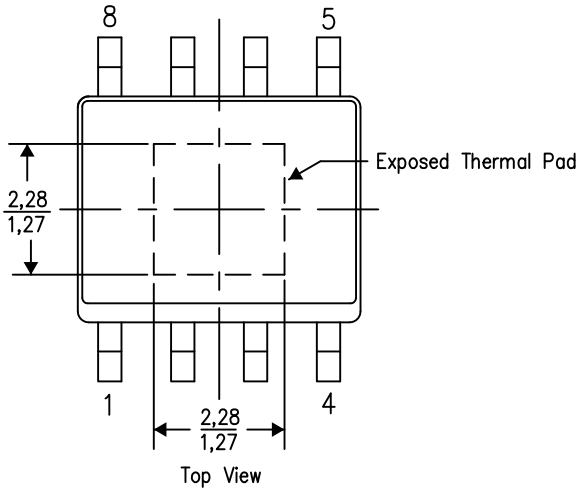
DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



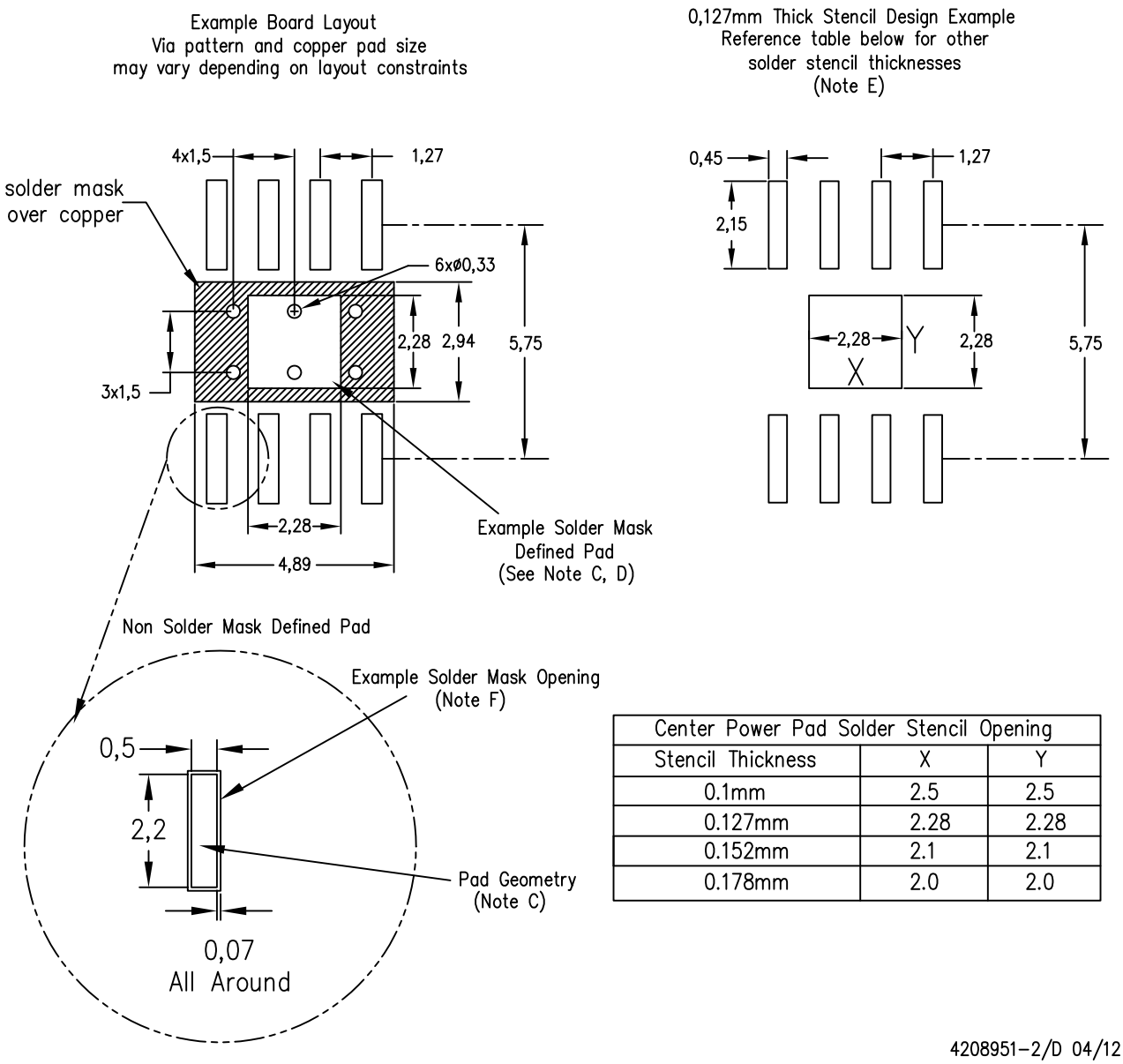
Exposed Thermal Pad Dimensions

4206322–2/L 05/12

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE

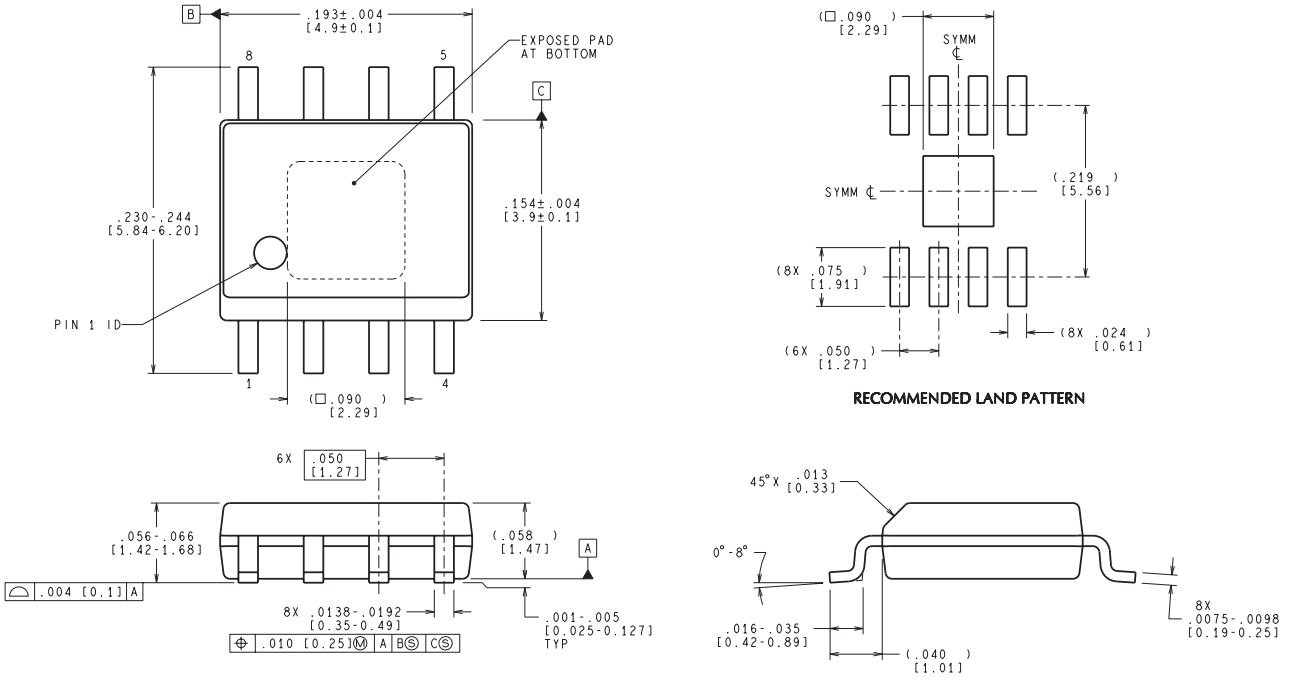


Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	2.5	2.5
0.127mm	2.28	2.28
0.152mm	2.1	2.1
0.178mm	2.0	2.0

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PowerPAD is a trademark of Texas Instruments.

DDA0008A



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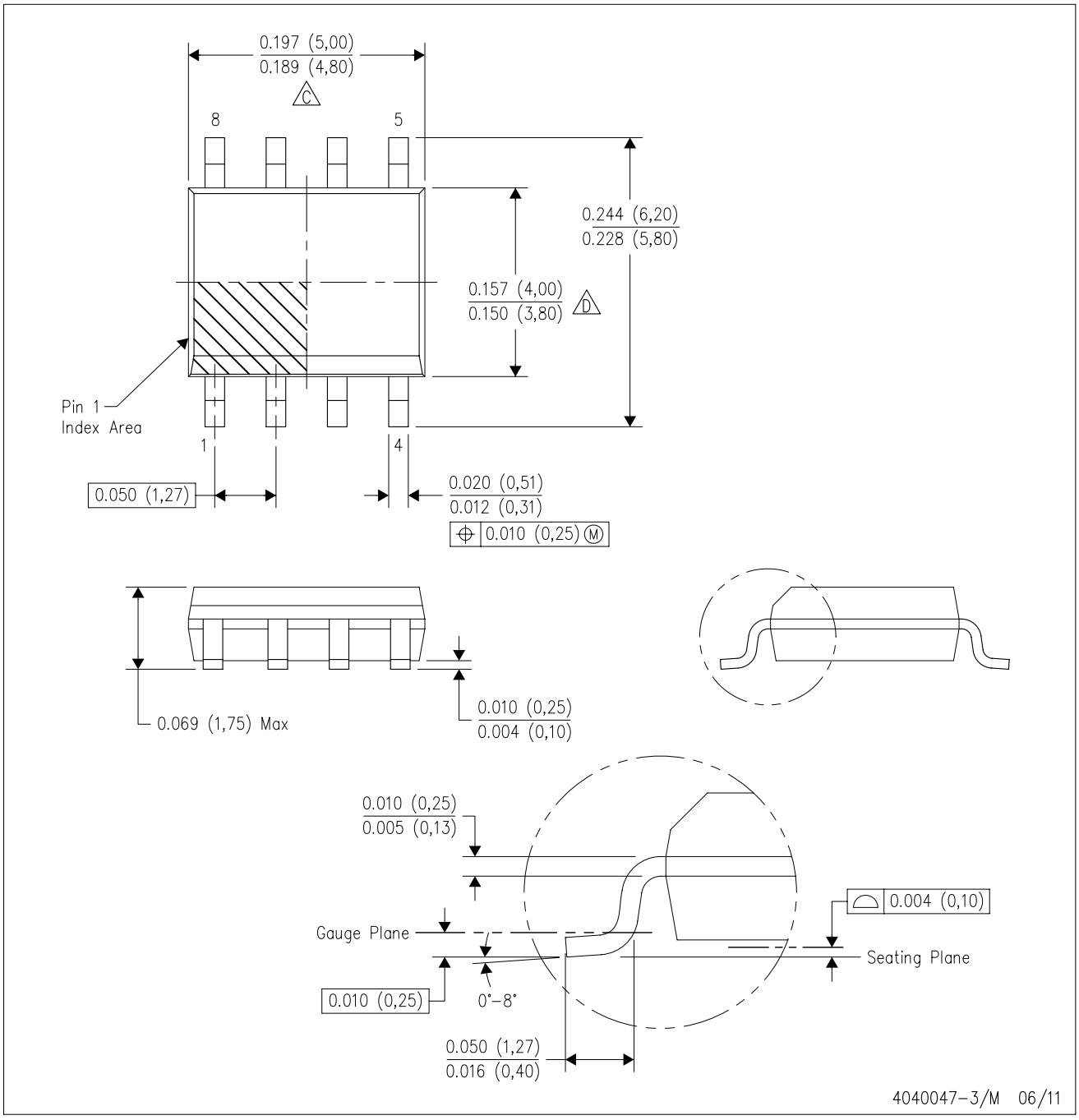
MRA08A (Rev D)

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

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