

DS89C386 Twelve Channel CMOS Differential Line Receiver

Check for Samples: [DS89C386](#)

FEATURES

- Low Power Design—240 mW Typical
- Meets TIA/EIA-422-B (RS-422)
- Receiver OPEN Input Failsafe Feature
- Ensured AC Parameters:
 - Maximum Receiver Skew –4 ns
 - Maximum Transition Time –9 ns
- High Output Drive Capability: ± 6 mA
- Available in SSOP Packaging:
 - Requires 30% less PCB Space than 3 DS34C86TMs

DESCRIPTION

The DS89C386 is a high speed twelve channel CMOS differential receiver that meets the requirements of TIA/EIA-422-B. The DS89C386 features low power dissipation of 240 mW typical.

Each TRI-STATE enable, EN, allows the receiver output to be active or in a Hi-impedance off state. Each enable is common to only two receivers for flexibility and multiplexing of receiver outputs.

The receiver output (RO) is ensured to be High when the inputs are left open and unterminated. The receiver can detect signals as low and including ± 200 mV over the common mode range of $\pm 7V$. The receiver outputs (RO) are compatible with both TTL and CMOS levels.

Connection Diagrams

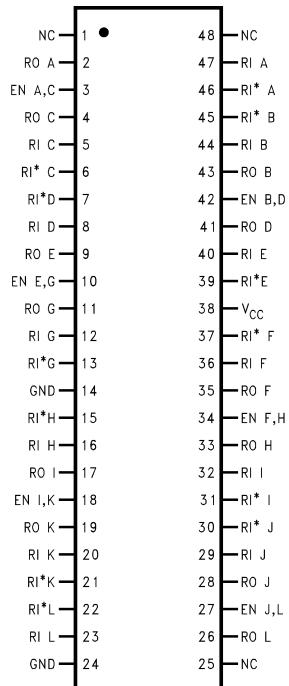


Figure 1. 48-Pin SSOP
See Package Number **DL0048A**

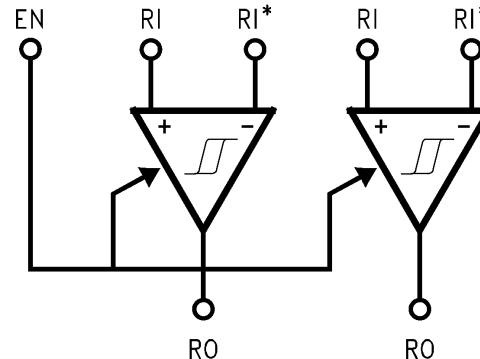


Figure 2. Function Diagram

Truth Table (1)

Enable	Inputs	Output
EN	RI-RI*	RO
L	X	Z
H	≥ 200 mV or OPEN ⁽¹⁾	H
H	≤ -200 mV	L
H	$+200$ mV > and > -200 mV	X

(1) Not terminated.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

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Absolute Maximum Ratings⁽¹⁾⁽²⁾⁽³⁾

Supply Voltage (V_{CC})	-0.5 to 7V
Input Common Mode Range (V_{CM})	$\pm 14V$
Differential Input Voltage (V_{DIFF})	$\pm 14V$
Enable Input Voltage (V_{IN})	7V
Storage Temperature Range (T_{STG})	-65°C to +150°C
Lead Temperature (Soldering 4 sec)	260°C
Maximum Power Dissipation at 25°C ⁽⁴⁾	
SSOP Package	1359 mW
Current Per Output	± 25 mA
This device does not meet 2000V ESD rating.⁽⁵⁾	

- (1) Unless otherwise specified, all voltages are referenced to ground.
- (2) Absolute Maximum Ratings are those values beyond which the safety of the device cannot be specified. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.
- (3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
- (4) Ratings apply to ambient temperature at 25°C. Above this temperature derate SSOP (MEA) Package 10.9 mW/°C.
- (5) ESD Rating: HEM (1.5 kΩ, 100 pF) Inputs $\geq 2000V$ Outputs $\geq 1000V$ EIAJ (0Ω, 200 pF) All Pins $\geq 350V$

Operating Conditions

		Min	Max	Unit
Supply Voltage (V_{CC})	4.50	5.50	V	
Operating Temperature Range (T_A)				
DS89C386T	-40	+85	°C	
Enable Input Rise or Fall Times		500	ns	

DC Electrical Characteristics⁽¹⁾

$V_{CC} = 5V \pm 10\%$ (unless otherwise specified)

Parameter	Test Conditions	Min	Typ	Max	Units
V_{TH}	Differential Input Voltage $V_{OUT} = V_{OH}$ or V_{OL} $-7V < V_{CM} < +7V$	-200	± 35	+200	mV
V_{HYST}	Input Hysteresis	$V_{CM} = 0V$		70	
R_{IN}	Input Resistance	$V_{IN} = -7V, +7V$ (Other Input = GND)	5.0	6.8	kΩ
I_{IN}	Input Current (Under Test)	$V_{IN} = +10V$, Other Input = GND $V_{IN} = -10V$, Other Input = GND		+1.1 -2.0	mA mA
V_{OH}	High Level Output Voltage	$V_{CC} = \text{Min.}$, $V_{(DIFF)} = +1V$ $I_{OUT} = -6.0$ mA	3.8	4.2	V
V_{OL}	Low Level Output Voltage	$V_{CC} = \text{Max.}$, $V_{(DIFF)} = -1V$ $I_{OUT} = 6.0$ mA		0.2	0.3
V_{IH}	Enable High Input Level Voltage		2.0		V_{CC}
V_{IL}	Enable Low Input Level Voltage		GND		V
I_{OZ}	TRI-STATE Output Leakage Current	$V_{OUT} = V_{CC}$ or GND, $EN = V_{IL}$		± 0.5	± 5.0 μA
I_I	Enable Input Current	$V_{IN} = V_{CC}$ or GND			± 1.0 μA
I_{CC}	Quiescent Power Supply Current	$V_{CC} = \text{Max.}$, $V_{(DIFF)} = +1V$		48	69

- (1) Unless otherwise specified, Min/Max limits apply across the operating temperature range. All typicals are given for $V_{CC} = 5V$ and $T_A = 25^\circ C$.

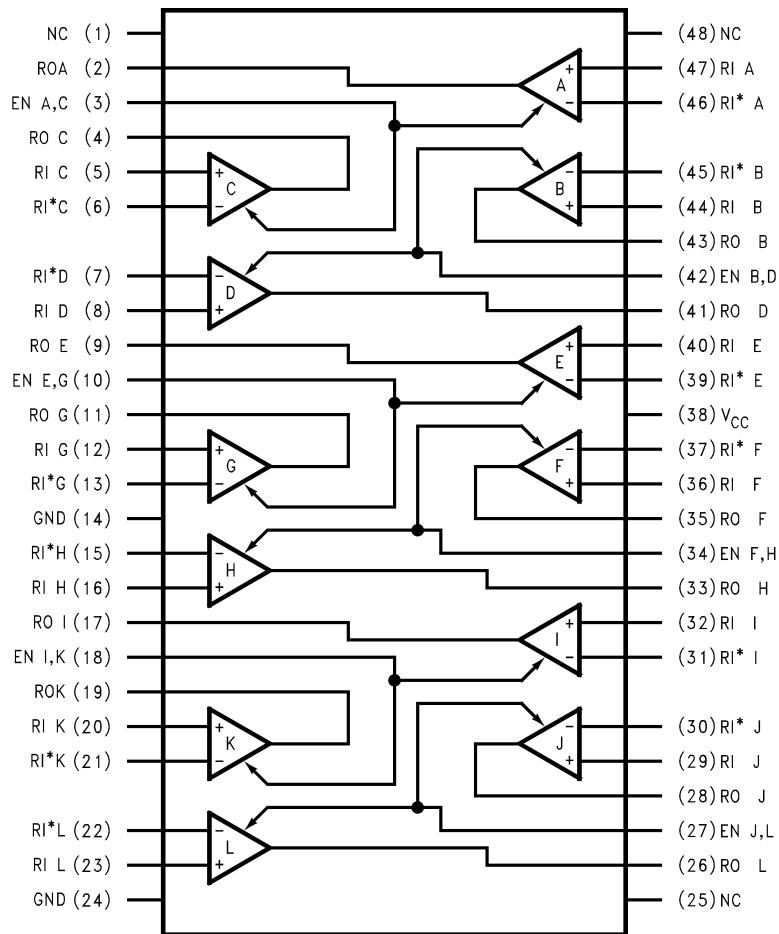
AC Electrical Characteristics⁽¹⁾

$V_{CC} = 5V \pm 10\%$ (Figure 3, Figure 4, and Figure 5)

Parameter		Test Conditions	Min	Typ	Max	Units
t_{PLH} , t_{PHL}	Propagation Delay Input to Output	$C_L = 50 \text{ pF}$ $V_{DIFF} = 2.5V$ $V_{CM} = 0V$	10	19	30	ns
t_{SK}	Skew	$C_L = 50 \text{ pF}$ $V_{DIFF} = 2.5V$ $V_{CM} = 0V$	0	2	4	ns
t_{RISE} , t_{FALL}	Output Rise and Fall Times	$C_L = 50 \text{ pF}$ $V_{DIFF} = 2.5V$ $V_{CM} = 0V$		4	9	ns
t_{PLZ} , t_{PHZ}	Propagation Delay ENABLE to Output	$C_L = 50 \text{ pF}$ $R_L = 1000\Omega$ $V_{DIFF} = 2.5V$		13	18	ns
t_{PZL} , t_{PZH}	Propagation Delay ENABLE to Output	$C_L = 50 \text{ pF}$ $R_L = 1000\Omega$ $V_{DIFF} = 2.5V$		13	21	ns

(1) Unless otherwise specified, Min/Max limits apply across the operating temperature range. All typicals are given for $V_{CC} = 5V$ and $T_A = 25^\circ\text{C}$.

Logic Diagram



Parameter Measurement Information

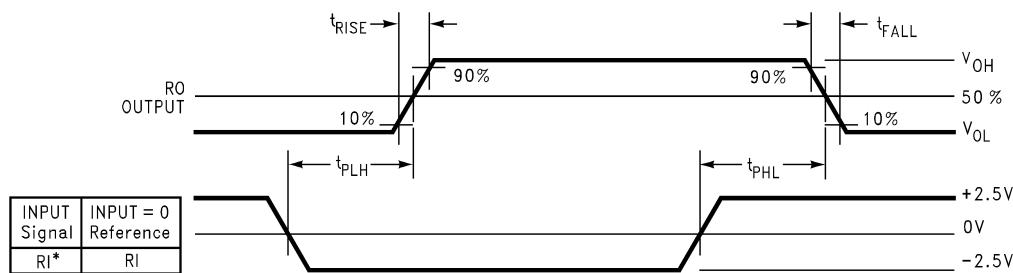
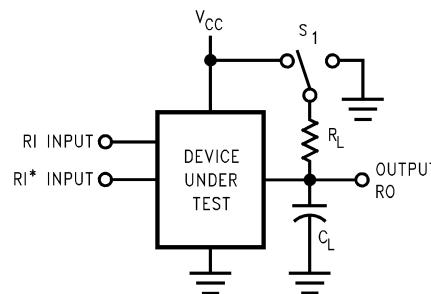


Figure 3. Propagation Delays



C_L Includes load and test jig capacitance.
 $S1 = V_{CC}$ for t_{PZL} , and t_{PLZ} measurements.
 $S1 = GND$ for t_{PZH} , and t_{PHZ} measurements.
 $S1 = Open$ for t_{PLH} , t_{PHL} , and t_{SK} .

Figure 4. Test Circuit for Switching Characteristics

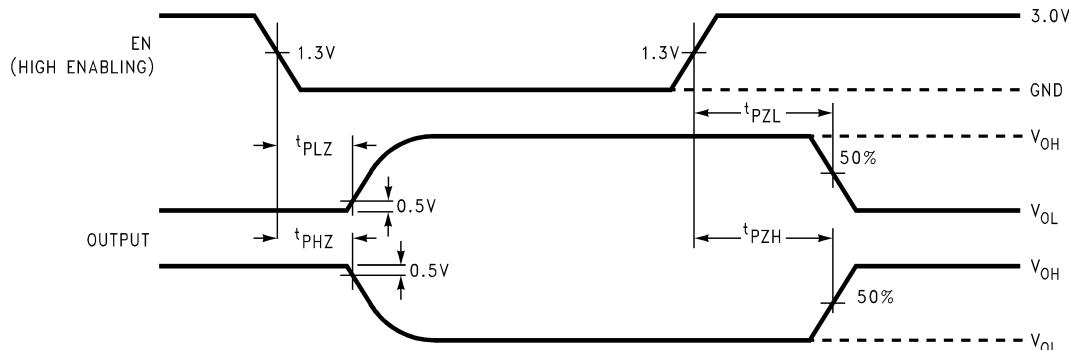
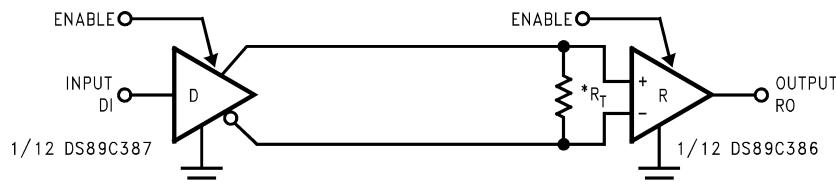


Figure 5. TRI-STATE Output Enable and Disable Waveforms

APPLICATION INFORMATION



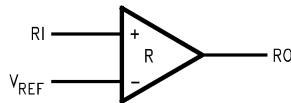
* R_T is optional although highly recommended to reduce reflections.

Figure 6. Two-Wire Balanced System, RS-422

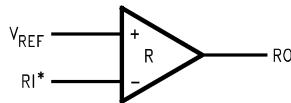
SKEW

Skew may be thought of in a lot of different ways, the next few paragraphs should clarify what is represented by t_{SK} in this datasheet and how it is determined. Skew, as used in this databook, is the absolute value of a mathematical difference between two propagation delays. This is commonly accepted throughout the semiconductor industry. However, there is no standardized method of measuring propagation delay, from which skew is calculated, of differential line receivers. Elucidating, the voltage level, at which propagation delays are measured, on both input and output waveforms are not always consistent. Therefore, skew calculated in this datasheet, may not be calculated the same as skew defined in another. This is important to remember whenever making a skew comparison.

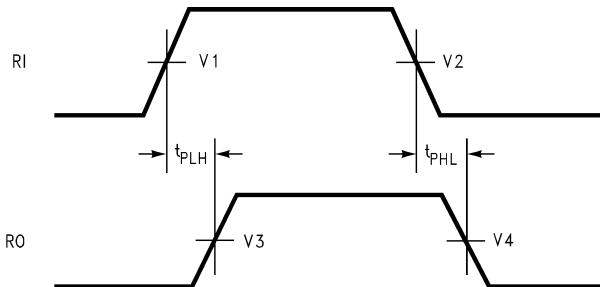
Skew may be calculated for the DS89C386, from many different propagation delay measurements. They may be classified into two categories, single-ended and differential. Single-ended skew is calculated from t_{PHL} and t_{PLH} propagation delay measurements (see [Figure 8](#) and [Figure 10](#)). Differential skew is calculated from t_{PHLD} and t_{PLHD} differential propagation delay measurements (see [Figure 11](#) and [Figure 12](#)).



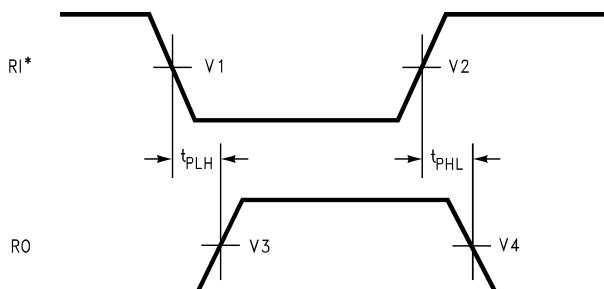
**Figure 7. (Circuit 1) – Circuits for Measuring Single-Ended Propagation Delays
(See [Figure 10](#))**



**Figure 8. (Circuit 2) – Circuits for Measuring Single-Ended Propagation Delays
(See [Figure 10](#))**



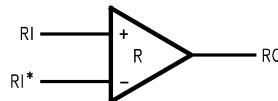
**Figure 9. Waveforms for Circuit 1 – Propagation Delay Waveforms for Circuit 1 and Circuit 2
(See [Figure 8](#))**



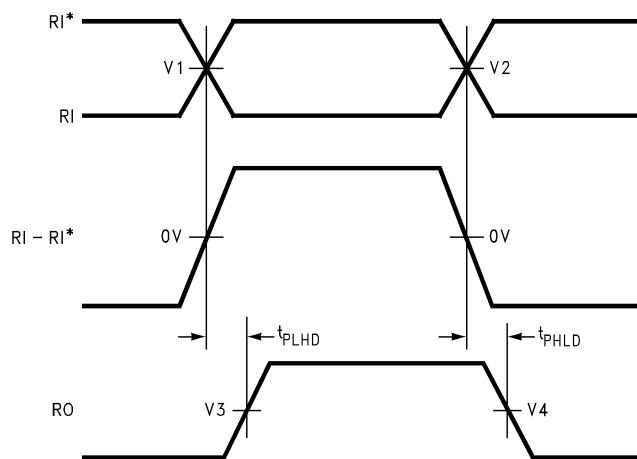
**Figure 10. Waveforms for Circuit 2 – Propagation Delay Waveforms for Circuit 1 and Circuit 2
(See [Figure 8](#))**

In [Figure 10](#), VX , where X is a number, is the waveform voltage level at which the propagation delay measurement either starts or stops. Furthermore, $V1$ and $V2$ are normally identical. The same is true for $V3$ and $V4$. However, as mentioned before, these levels are not standardized and may vary, even with similar devices from other companies. Also note, V_{REF} in [Figure 3](#) should equal $V1$ and $V2$ in [Figure 10](#).

The single-ended skew provides information about the pulse width distortion of the output waveform. The lower the skew, the less the output waveform will be distorted. For best case, skew would be zero, and the output duty cycle would be 50%, assuming the input has a 50% duty cycle.



**Figure 11. (Circuit 3) – Circuit for Measuring Differential Propagation Delays
(See [Figure 12](#))**



**Figure 12. Waveforms for Circuit 3 – Propagation Delay Waveforms
for Circuit 3
(see [Figure 11](#))**

For differential propagation delays, $V1$ may not equal $V2$. Furthermore, the crossing point of RI and RI^* corresponds to zero volts on the differential waveform. (See middle waveform in [Figure 12](#).) This is true whether $V1$ equals $V2$ or not. However, if $V1$ and $V2$ are specified voltages, then $V1$ and $V2$ are less likely to be equal to the crossing point voltage. Thus, the differential propagation delays will not be measured from zero volts on the differential waveform.

The differential skew also provides information about the pulse width distortion of the output waveform relative to the differential input waveform. The higher the skew, the greater the distortion of the output waveform. Assuming the differential input has a 50% duty cycle, the output will have a 50% duty cycle if skew equals zero and less than a 50% duty cycle if skew is greater than zero.

Only t_{SK} is specified in this datasheet for the DS89C386. t_{SK} is measured single-endedly but corresponds to differential skew. Because, for single-ended skew, when V_{REF} equals $V1$ and $V2$, t_{PHL} equals t_{PHLD} when t_{PHLD} is measured from the crossing point.

More information can be calculated from the propagation delays. The channel to channel and device to device skew may be calculated in addition to the types of skew mentioned previously. These parameters provide timing performance information beneficial when designing. The channel to channel skew is calculated from the variation in propagation delay from receiver to receiver within one package. The device to device skew is calculated from the variation in propagation delay from one DS89C386 to another DS89C386.

For the DS89C386, the maximum channel to channel skew is 20 ns (t_p max— t_p min) where t_p is the low to high or high to low propagation delay. The minimum channel to channel skew is 0 ns since it is possible for all 12 receivers to have identical propagation delays. Note, this is best and worst case calculations used whenever t_{SK} (channel) is not independently characterized and specified in the datasheet. The device to device skew may be calculated in the same way and the results are identical. Therefore, the device to device skew is 20 ns and 0 ns maximum and minimum respectively.

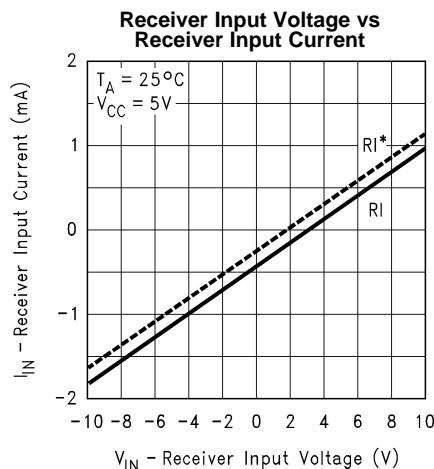
Table 1. DS89C386 Skew Table

Parameter	Min	Typ	Max	Units
t_{SK} (diff.)	0	2	4	ns
t_{SK} (channel)	0		20	ns
t_{SK} (device)	0		20	ns

Note t_{SK} (diff.) in [Table 1](#) is the same as t_{SK} in the datasheet. Also, t_{SK} (channel) and t_{SK} (device) are calculations, but are ensured by the propagation delay tests. Both t_{SK} (channel) and t_{SK} (device) would normally be tighter whenever specified from characterization data.

The information in this section of the datasheet is to help clarify how skew is defined in this datasheet. This should help when designing the DS89C386 into most applications.

Typical Performance Characteristics



The DS89C386 is V.11 compatible. I_{IN} (RI input) is not ≥ 0 when $V_{IN} = 3\text{V}$ due to internal failsafe bias resistors (see [Figure 10](#)). See ITU V.11 for complete conditions.

Failsafe (open inputs) is maintained over entire common mode range and operating range $\pm 10\text{V}$.
[Figure 13](#).

DS89C386 Equivalent Input/Output Circuits

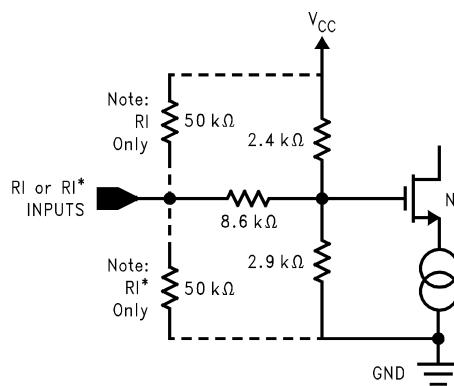


Figure 14. Receiver Input Equivalent Circuit

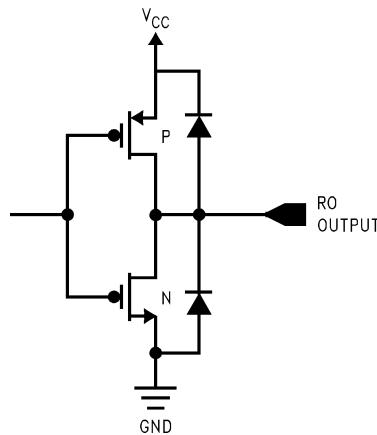


Figure 15. Receiver Output Equivalent Circuit

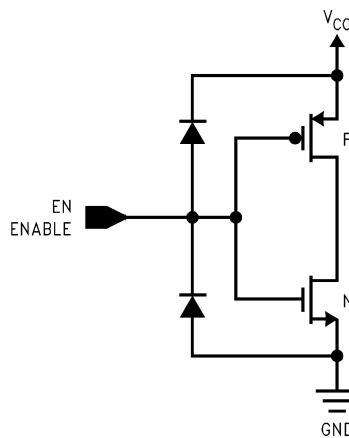


Figure 16. Receiver Enable Equivalent Circuit

Table 2. Pin Descriptions

Pin No.	Pin Name	Pin Description
2, 4, 9, 11, 17, 19, 26, 28, 33, 35, 41, 43	RO	TTL/CMOS Compatible Receiver Output Pin
5, 8, 12, 16, 20, 23, 29, 32, 36, 40, 44, 47	RI	Non-Inverting Signal Receiver Input Pin
6, 7, 13, 15, 21, 22, 30, 31, 37, 39, 45, 46	RI*	Inverting Signal Receiver Input Pin
3, 10, 18, 27, 34, 42	EN	Active High Dual Receiver Enabling Pin
38	V _{CC}	Positive Power Supply Pin +5 ±10%
14, 24	GND	Device Ground Pin
1, 25, 48	NC	Unused Pin (NOT CONNECTED)

REVISION HISTORY

Changes from Revision B (April 2013) to Revision C	Page
• Changed layout of National Data Sheet to TI format	8

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS89C386TMEA	NRND	SSOP	DL	48	29	TBD	Call TI	Call TI	-40 to 85	DS89C386T MEA	
DS89C386TMEA/NOPB	ACTIVE	SSOP	DL	48	29	Pb-Free (RoHS)	SN	Level-2A-260C-4 WEEK	-40 to 85	DS89C386T MEA	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

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Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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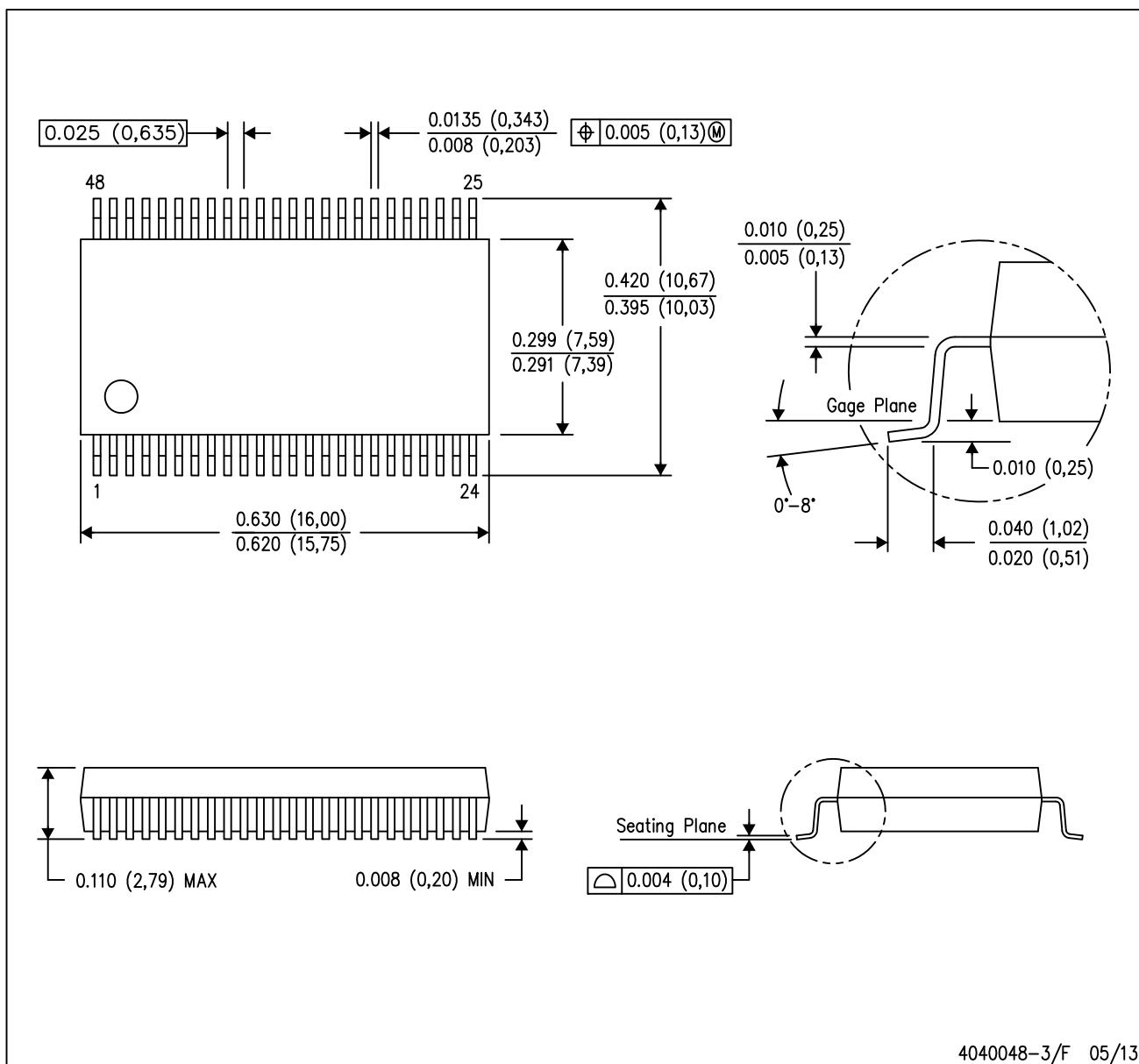
PACKAGE OPTION ADDENDUM

1-Nov-2013

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DL (R-PDSO-G48)

PLASTIC SMALL-OUTLINE PACKAGE



4040048-3/F 05/13

NOTES:

- All linear dimensions are in inches (millimeters).
- This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- Falls within JEDEC MO-118

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