

# FDS2570

## 150V N-Channel PowerTrench® MOSFET

### General Description

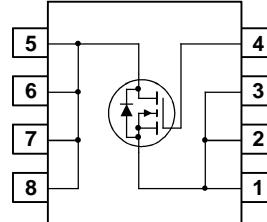
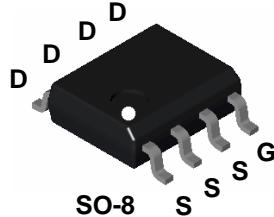
This N-Channel MOSFET has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers.

These MOSFETs feature faster switching and lower gate charge than other MOSFETs with comparable  $R_{DS(ON)}$  specifications.

The result is a MOSFET that is easy and safer to drive (even at very high frequencies), and DC/DC power supply designs with higher overall efficiency.

### Features

- 4A, 150 V.  $R_{DS(ON)} = 80 \text{ m}\Omega$  @  $V_{GS} = 10 \text{ V}$   
 $R_{DS(ON)} = 90 \text{ m}\Omega$  @  $V_{GS} = 6 \text{ V}$
- Low gate charge
- Fast switching speed
- High performance trench technology for extremely low  $R_{DS(ON)}$
- High power and current handling capability



### Absolute Maximum Ratings

$T_A = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Ratings	Units
$V_{DSS}$	Drain-Source Voltage	150	V
$V_{GSS}$	Gate-Source Voltage	$\pm 20$	V
$I_D$	Drain Current – Continuous (Note 1a)	4	A
	– Pulsed	30	
$P_D$	Power Dissipation for Single Operation (Note 1a)	2.5	W
		1.2	
		1.0	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	°C

### Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	50	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1c)	125	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	25	°C/W

### Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
FDS2570	FDS2570	13"	12mm	2500 units

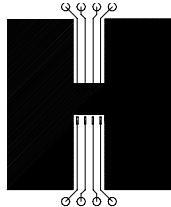
## Electrical Characteristics

$T_A = 25^\circ\text{C}$  unless otherwise noted

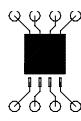
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
<b>Drain-Source Avalanche Ratings (Note 1)</b>						
$W_{DSS}$	Single Pulse Drain-Source Avalanche Energy	$V_{DD} = 75\text{ V}$ , $I_D = 4.4\text{ A}$			375	mJ
$I_{AR}$	Maximum Drain-Source Avalanche Current				4.4	A
<b>Off Characteristics</b>						
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}$ , $I_D = 250\text{ }\mu\text{A}$	150			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , Referenced to $25^\circ\text{C}$		150		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 120\text{ V}$ , $V_{GS} = 0\text{ V}$			1	$\mu\text{A}$
$I_{GSSF}$	Gate-Body Leakage, Forward	$V_{GS} = 20\text{ V}$ , $V_{DS} = 0\text{ V}$			100	NA
$I_{GSSR}$	Gate-Body Leakage, Reverse	$V_{GS} = -20\text{ V}$ $V_{DS} = 0\text{ V}$			-100	NA
<b>On Characteristics (Note 2)</b>						
$V_{GS(\text{th})}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$	2	2.6	4	V
$\frac{\Delta V_{GS(\text{th})}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , Referenced to $25^\circ\text{C}$		-7		mV/ $^\circ\text{C}$
$R_{DS(\text{on})}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}$ , $I_D = 4\text{ A}$ $V_{GS} = 6\text{ V}$ , $I_D = 3.8\text{ A}$ $V_{GS} = 10\text{ V}$ , $I_D = 4\text{ A}$ , $T_J = 125^\circ\text{C}$	60 63 120	80 90 158		$\text{m}\Omega$
$I_{D(\text{on})}$	On-State Drain Current	$V_{GS} = 10\text{ V}$ , $V_{DS} = 10\text{ V}$	30			A
$g_{FS}$	Forward Transconductance	$V_{DS} = 10\text{ V}$ , $I_D = 4\text{ A}$		20		S
<b>Dynamic Characteristics</b>						
$C_{iss}$	Input Capacitance	$V_{DS} = 75\text{ V}$ , $V_{GS} = 0\text{ V}$ , $f = 1.0\text{ MHz}$		1907		PF
$C_{oss}$	Output Capacitance			117		PF
$C_{rss}$	Reverse Transfer Capacitance			33		PF
<b>Switching Characteristics (Note 2)</b>						
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 75\text{ V}$ , $I_D = 1\text{ A}$ , $V_{GS} = 10\text{ V}$ , $R_{\text{GEN}} = 6\text{ }\Omega$		12	19	Ns
$t_r$	Turn-On Rise Time			7	14	Ns
$t_{d(off)}$	Turn-Off Delay Time			41	65	Ns
$t_f$	Turn-Off Fall Time			21	34	Ns
$Q_g$	Total Gate Charge	$V_{DS} = 75\text{ V}$ , $I_D = 4\text{ A}$ , $V_{GS} = 10\text{ V}$		39	62	NC
$Q_{gs}$	Gate-Source Charge			7		NC
$Q_{gd}$	Gate-Drain Charge			9		NC
<b>Drain-Source Diode Characteristics and Maximum Ratings</b>						
$I_S$	Maximum Continuous Drain-Source Diode Forward Current				2.1	A
$V_{SD}$	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}$ , $I_S = 2.1\text{ A}$ (Note 2)		0.7	1.2	V

**Notes:**

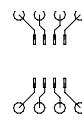
1.  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a) 50°C/W when mounted on a 1in<sup>2</sup> pad of 2 oz copper



b) 105°C/W when mounted on a .04 in<sup>2</sup> pad of 2 oz copper



c) 125°C/W when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width < 300μs, Duty Cycle < 2.0%

## Typical Characteristics

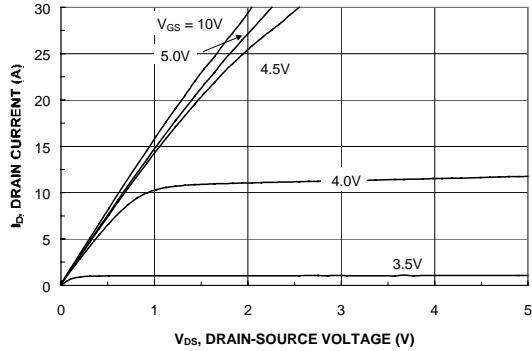


Figure 1. On-Region Characteristics.

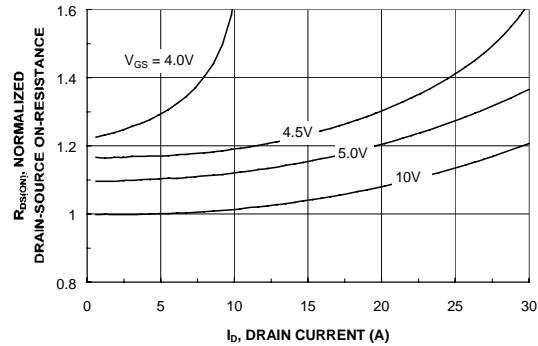


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

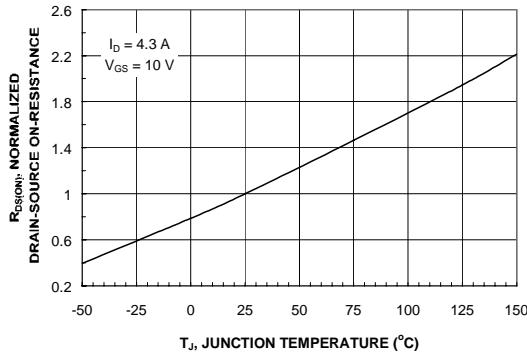


Figure 3. On-Resistance Variation with Temperature.

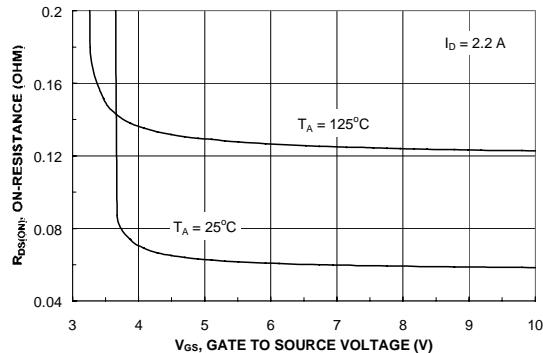


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

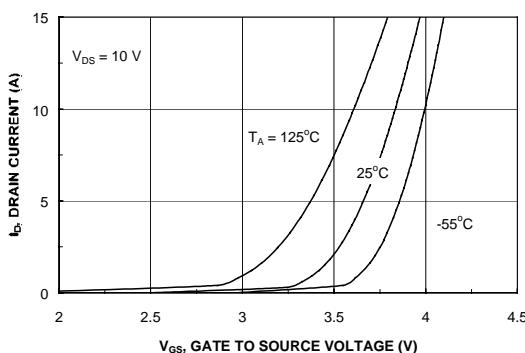


Figure 5. Transfer Characteristics.

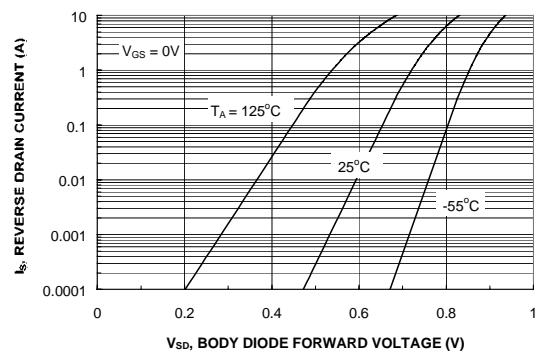


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

## Typical Characteristics

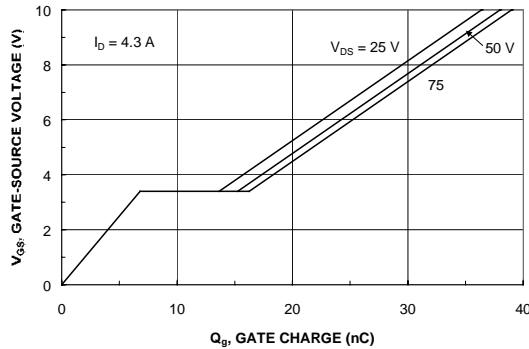


Figure 7. Gate Charge Characteristics.

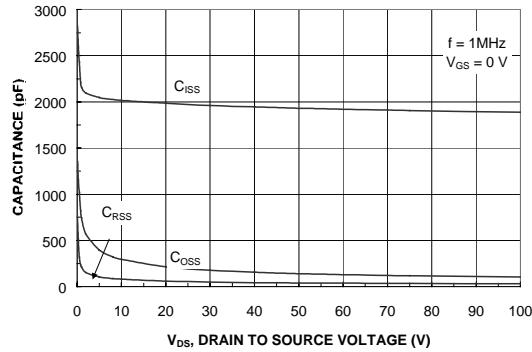


Figure 8. Capacitance Characteristics.

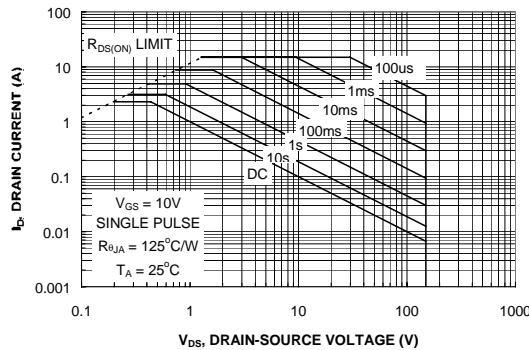


Figure 9. Maximum Safe Operating Area.

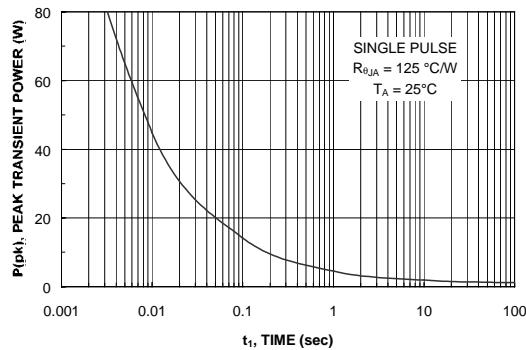


Figure 10. Single Pulse Maximum Power Dissipation.

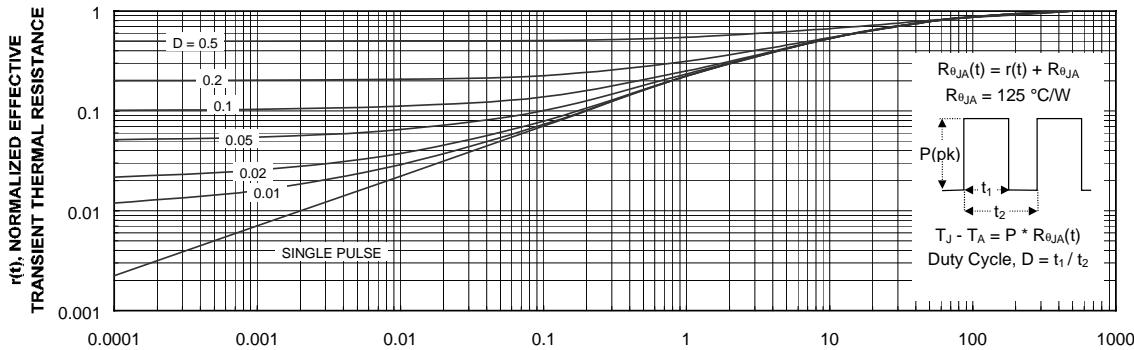


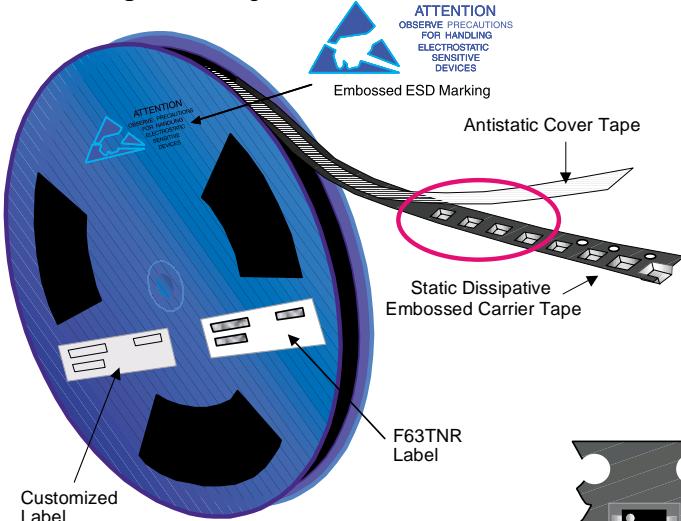
Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1c.  
Transient thermal response will change depending on the circuit board design.

## SOIC-8 Tape and Reel Data

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### SOIC(8lds) Packaging Configuration: Figure 1.0

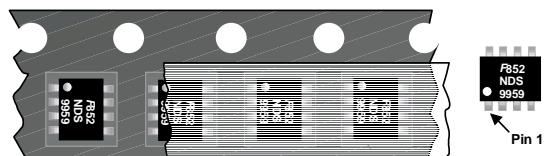


SOIC (8lds) Packaging Information				
Packaging Option	Standard (no flow code)	L86Z	F011	D84Z
Packaging type	TNR	Rail/Tube	TNR	TNR
Qty per Reel/Tube/Bag	2,500	95	4,000	500
Reel Size	13" Dia	-	13" Dia	7" Dia
Box Dimension (mm)	355x333x40	530x130x83	355x333x40	193x183x80
Max qty per Box	5,000	30,000	8,000	2,000
Weight per unit (gm)	0.0774	0.0774	0.0774	0.0774
Weight per Reel (kg)	0.6060	-	0.9696	0.1182
Note/Comments				

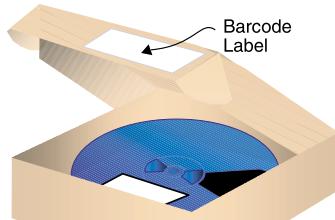
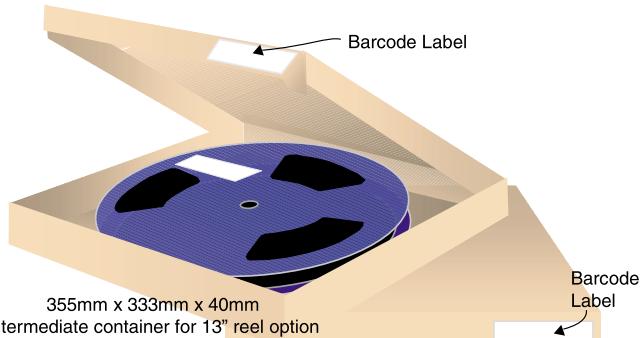
### Packaging Description:

SOIC-8 parts are shipped in tape. The carrier tape is made from a dissipative (carbon filled) polycarbonate resin. The cover tape is a multilayer film (Heat Activated Adhesive in nature) primarily composed of polyester film, adhesive layer, sealant, and anti-static sprayed agent. These reeled parts in standard option are shipped with 2,500 units per 13" or 330cm diameter reel. The reels are dark blue in color and is made of polystyrene plastic (anti-static coated). Other option comes in 500 units per 7" or 177cm diameter reel. This and some other options are further described in the Packaging Information table.

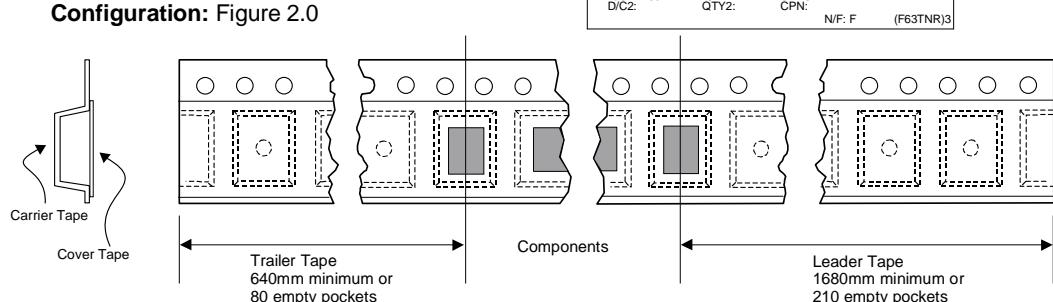
These full reels are individually barcode labeled and placed inside a standard intermediate box (illustrated in figure 1.0) made of recyclable corrugated brown paper. One box contains two reels maximum. And these boxes are placed inside a barcode labeled shipping box which comes in different sizes depending on the number of parts shipped.



### SOIC-8 Unit Orientation



### SOIC(8lds) Tape Leader and Trailer Configuration: Figure 2.0



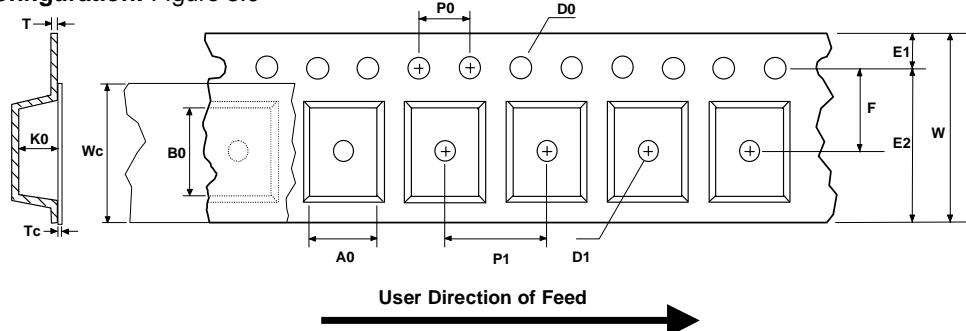
### F63TNR Label sample

LOT: CBVK741B019	QTY: 2500
FSID: FDS9953A	SPEC:
D/C1: Z9842AB	QTY1: 2500
D/C2:	QTY2: 0
	SPEC REV: CPN: (F63TNR)3
	N/F: F

## SOIC-8 Tape and Reel Data, continued

### SOIC(8lds) Embossed Carrier Tape

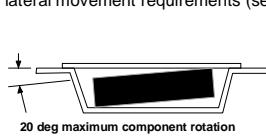
Configuration: Figure 3.0



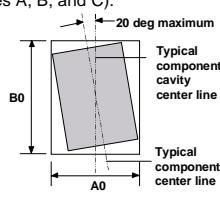
Dimensions are in millimeter

Pkg type	A0	B0	W	D0	D1	E1	E2	F	P1	P0	K0	T	Wc	Tc
SOIC(8lds) (12mm)	5.30 +/-0.10	6.50 +/-0.10	12.0 +/-0.3	1.55 +/-0.05	1.60 +/-0.10	1.75 +/-0.10	10.25 min	5.50 +/-0.05	8.0 +/-0.1	4.0 +/-0.1	2.1 +/-0.10	0.450 +/-0.150	9.2 +/-0.3	0.06 +/-0.02

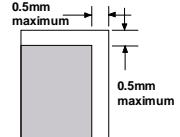
Notes: A0, B0, and K0 dimensions are determined with respect to the EIA/Jedec RS-481 rotational and lateral movement requirements (see sketches A, B, and C).



Sketch A (Side or Front Sectional View)  
Component Rotation

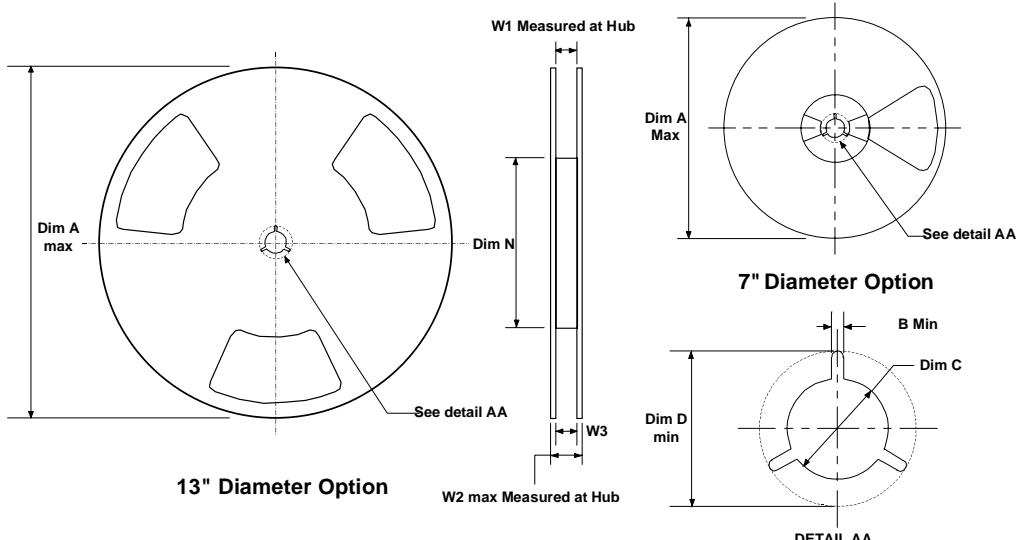


Sketch B (Top View)  
Component Rotation



Sketch C (Top View)  
Component lateral movement

### SOIC(8lds) Reel Configuration: Figure 4.0



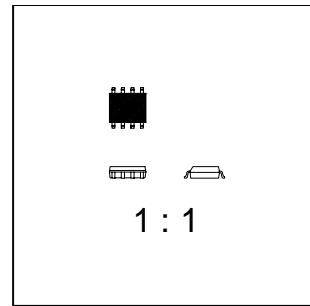
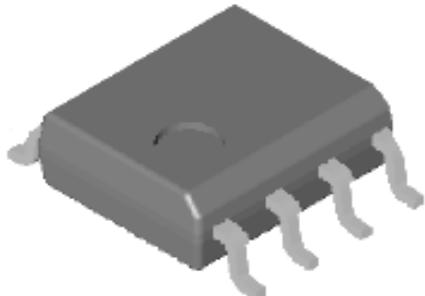
Dimensions are in inches and millimeters

Tape Size	Reel Option	Dim A	Dim B	Dim C	Dim D	Dim N	Dim W1	Dim W2	Dim W3 (LSL-USL)
12mm	7" Dia	7.00 177.8	0.059 1.5	512 +0.020/-0.008 13 +0.5/-0.2	0.795 20.2	2.165 55	0.488 +0.078/-0.000 12.4 +2/0	0.724 18.4	0.469 - 0.606 11.9 - 15.4
12mm	13" Dia	13.00 330	0.059 1.5	512 +0.020/-0.008 13 +0.5/-0.2	0.795 20.2	7.00 178	0.488 +0.078/-0.000 12.4 +2/0	0.724 18.4	0.469 - 0.606 11.9 - 15.4

## SOIC-8 Package Dimensions

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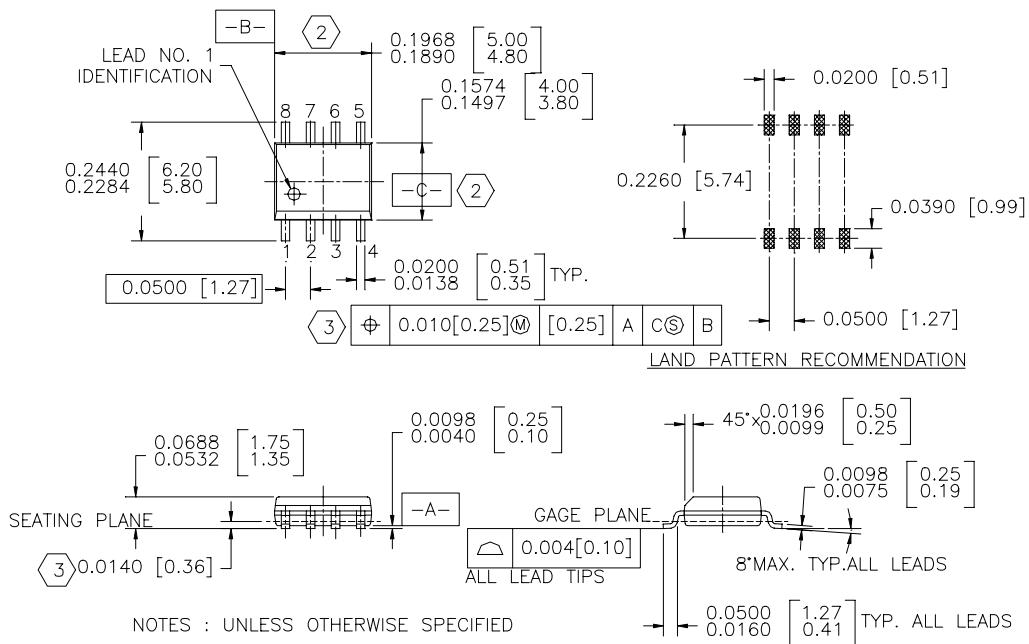
### SOIC-8 (FS PKG Code S1)



Scale 1:1 on letter size paper

Dimensions shown below are in:  
inches [millimeters]

Part Weight per unit (gram): 0.0774



1. STANDARD LEAD FINISH:  
200 MICROINCHES / 5.08 MICRONS MINIMUM  
LEAD / TIN (SOLDER) ON COPPER. SO 0.150 WIDE 8 LEADS

(2.) THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH  
(3.) MAXIMUM LEAD 0.024 [0.609]

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DOME <sup>TM</sup>	ISOPLANAR <sup>TM</sup>	Quiet Series <sup>TM</sup>	
E <sup>2</sup> CMOS <sup>TM</sup>	MICROWIRE <sup>TM</sup>	SILENT SWITCHER <sup>®</sup>	
EnSigna <sup>TM</sup>	OPTOLOGIC <sup>TM</sup>	SMART START <sup>TM</sup>	
FACT <sup>TM</sup>	OPTOPLANAR <sup>TM</sup>	SuperSOT <sup>TM</sup> -3	
FACT Quiet Series <sup>TM</sup>	PACMAN <sup>TM</sup>	SuperSOT <sup>TM</sup> -6	
FAST <sup>®</sup>	POP <sup>TM</sup>	SuperSOT <sup>TM</sup> -8	

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## PRODUCT STATUS DEFINITIONS

### Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
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