

TENTATIVE

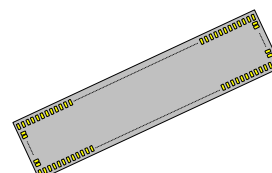
160COMMON x 128RGB LCD DRIVER FOR 65,536-COLOR STN DISPLAY

■ GENERAL DESCRIPTION

The **NJU6855** is a 160COMMONx128RGB LCD driver for 65,536-color STN display. It contains common drivers, RGB drivers, a serial and a parallel MPU interface circuit, an internal LCD power supply, grayscale palettes and 327,680-bit display data RAM. The segment drivers for RGB (Red, Green, Blue) independently produce optimum 64 or 32 grayscales from a built-in grayscale palette, and the LSI achieves 65,536 colors (64x32x32).

In addition, the **NJU6855** operates with a low voltage of 1.7V and a low operating current, therefore it is ideally suited for battery-powered handheld applications.

■ PACKAGE

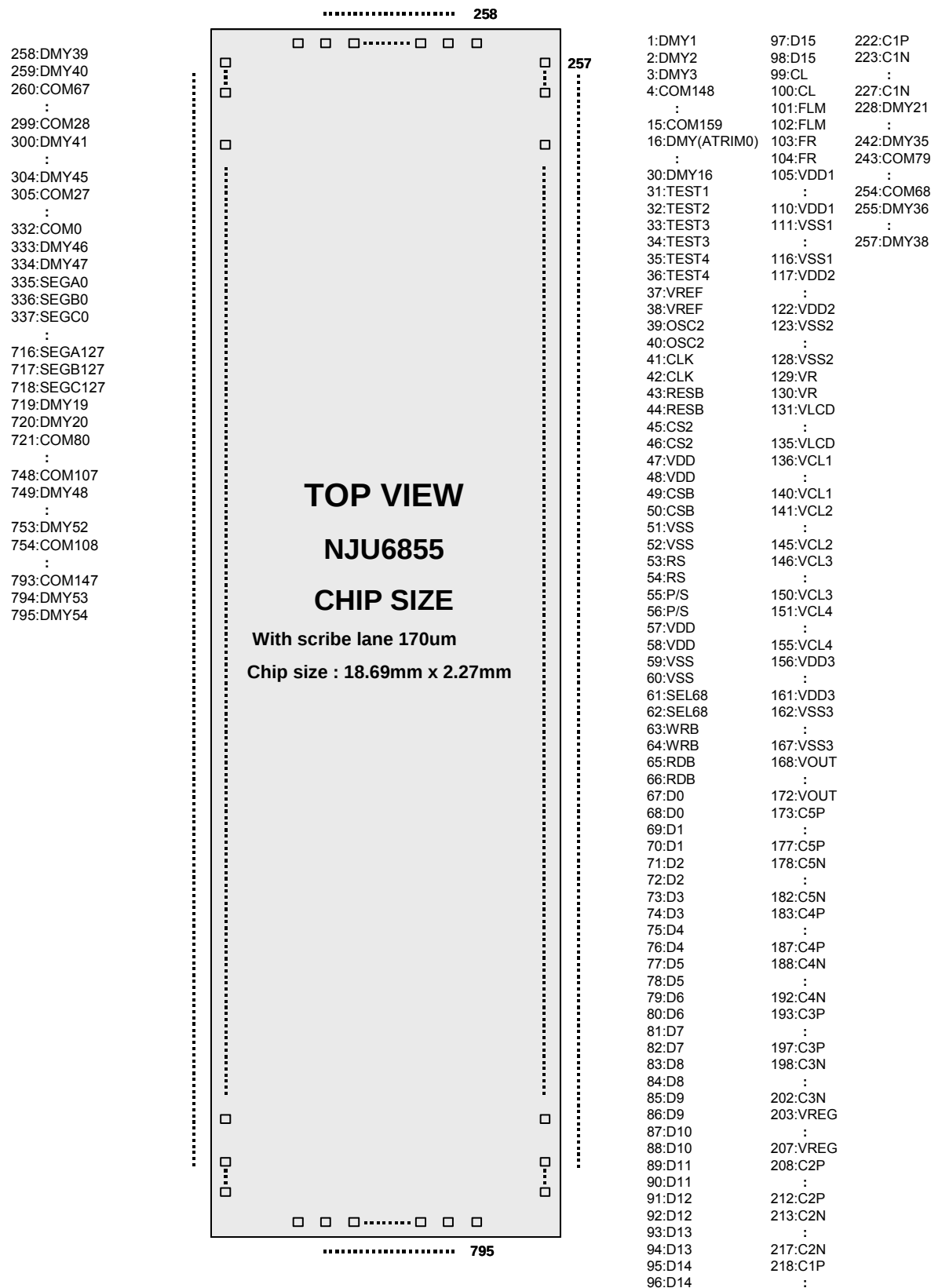


BUMP CHIP

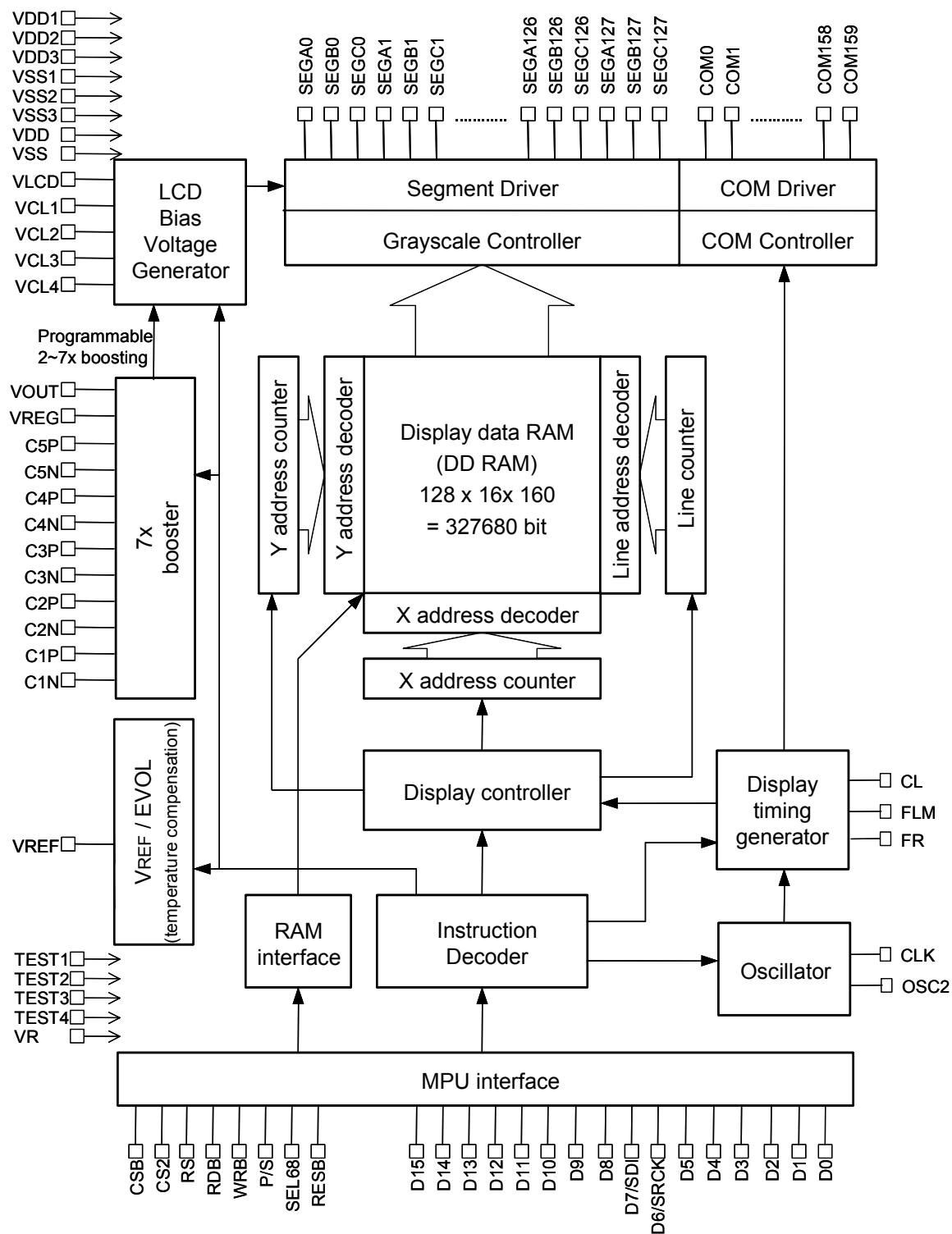
■ FEATURES

- 65,536-color STN LCD driver
- Built-in LCD Drivers : 160-common x 128RGB (384-segment drivers)
- Built-in Display Data RAM (DDRAM) : 327,680 bits for Graphic Display
- Programmable Display Mode
 - 64 grayscales(Green)
 - 32 grayscales(Red, Blue)
- 2 Areas Partial Display
- 8-/16-bit Parallel Interface Selectable
- 8-/16-bit Bus Length for Display Data Selectable
- 3-/4-line Serial Interface Selectable
- Programmable Duty Ratio and Bias Ratio
- Programmable Internal Voltage Booster : Maximum 7 times
- Programmable Contrast Control : 256-step Electronic Volume Register (EVR)
- Various Useful Instructions
- Low Operating Current
- Low Logic Voltage : 1.7V to 3.3V
- Wide LCD Voltage Range : 5.0V to 18.0V
- C-MOS Technology
- Slim Chip for COG
- Package : Bump Chip

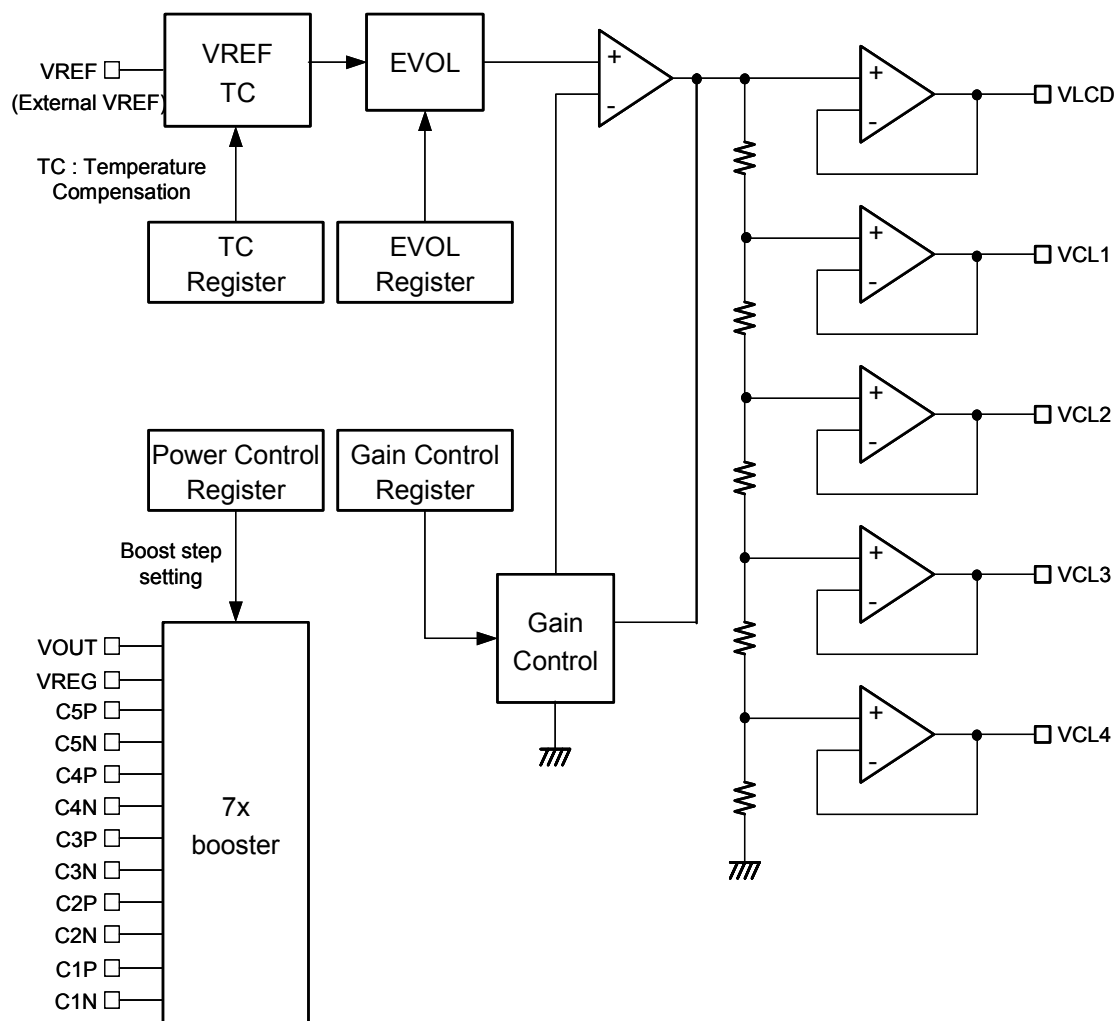
■ PAD LOCATION



■ BLOCK DIAGRAM



■ LCD POWER SUPPLY BLOCK DIAGRAM



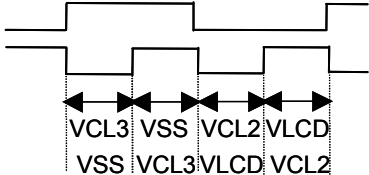
■ TERMINAL DESCRIPTION
Power Supply

No.	Terminal	I/O	Description
105-110	V _{DD1}	Power	Power Supply for Logic Circuit
117-122	V _{DD2}	Power	Power Supply for Analog Circuit
156-161	V _{DD3}	Power	Power Supply for Voltage Booster
47-48 57-58	V _{DD}	Power	Power Supply for Logic Circuit(Internally connected to VDD1) External power supply is not allowed
51-52 59-60	V _{SS}	Power	GND for Logic Circuit (internally connected to VSS1) External power supply is not allowed.
111-116	V _{SS1}	Power	GND for Logic Circuit
123-128	V _{SS2}	Power	GND for Analog Circuit
162-167	V _{SS3}	Power	GND for Voltage Booster(or high voltage)
131-135 136-140 141-145 146-150 151-155	VLCD VCL1 ~VCL4	Power/O	LCD Bias Voltage When the internal LCD power supply is used, LCD bias voltages (VLCD and VCL1~VCL4) are generated by the built-in Voltage Booster, and capacitors must be connected between these pins and GND for stabilizing. When the external LCD power supply is used, LCD bias voltages must maintain the following shown relationship: VSS < VCL4 < VCL3 < VCL2 < VCL1 < VLCD
218-222 223-227	C1P, C1N	O	Capacitor Connection for Voltage Booster
208-212 213-217	C2P, C2N	O	Capacitor Connection for Voltage Booster
193-197 198-202	C3P, C3N	O	Capacitor Connection for Voltage Booster
183-187 188-192	C4P, C4N	O	Capacitor Connection for Voltage Booster
173-177 178-182	C5P, C5N	O	Capacitor Connection for Voltage Booster
168-172	VOUT	Power/O	High Voltage Power Supply(from external power) Internal Voltage Booster output (2x~7x boosting)
203-207	V _{REG}	Power/O	High Voltage Power Supply(from external power) Internal Voltage Booster output(2x boosting)
37-38	V _{REF}	I	External Reference Voltage Input Pin When TSEL<2:0> is "101" or "110" or "111", external reference voltage is used. Set to "L" or "H" when not used.

MPU Interface

Pin I/O Interface																							
No.	Terminal	I/O	Description																				
79-80	D6/SRCK	I/O	Parallel Interface D ₇ to D ₀ : 8-bit Bi-directional Bus(P/S="H") Serial Interface SDI: Serial Data Input SRCK: Shift Clock																				
81-82	D7/SDI	I/O																					
67-78	D0-D5	I/O																					
83-98	D8-D15	I/O	8-bit Bidirectional Bus In the 16-bit data bus mode, D15~D8 assigned to upper 8-bit data. In the serial interface mode or 8-bit parallel interface mode, D15-D8 should be fixed to "H" or "L".																				
49-50 45-46	CSB, CS2	I	Chip Select Active "L"																				
53-54	RS	I	Register Select Interprets transferred data as display data or instruction <table><tr><td>RS</td><td>H</td><td>L</td></tr><tr><td>Data</td><td>Instruction</td><td>Display Data</td></tr></table>			RS	H	L	Data	Instruction	Display Data												
RS	H	L																					
Data	Instruction	Display Data																					
65-66	RDB(E)	I	80-series MPU Interface (P/S="H", SEL68="L") Data Read (RDb) Signal: Active "L" 68-series MPU Interface (P/S="H", SEL68="H") Enable Signal: Active "H"																				
63-64	WRB(R/WB)	I	80-series MPU Interface (P/S="H", SEL68="L") Data Write (WRb) Signal: Active "L" 68-series MPU Interface (P/S="H", SEL68="H") Data Read or Write (R/W) Signal <table><tr><td>R/W</td><td>H</td><td>L</td></tr><tr><td>Status</td><td>Read</td><td>Write</td></tr></table>			R/W	H	L	Status	Read	Write												
R/W	H	L																					
Status	Read	Write																					
61-62	SEL68	I	MPU Mode Select <table><tr><td>SEL86</td><td>H</td><td>L</td></tr><tr><td>MPU</td><td>68-series</td><td>80-series</td></tr></table>			SEL86	H	L	MPU	68-series	80-series												
SEL86	H	L																					
MPU	68-series	80-series																					
55-56	P/S	I	Parallel/Serial Interface Mode Select <table><tr><td>P/S</td><td>Chip Select</td><td>Display / Instruction</td><td>Data</td><td>Read /Write</td><td>Serial Clock</td></tr><tr><td>H</td><td>CSB</td><td>RS</td><td>D₀ ~ D₇</td><td>RDB, WRB</td><td>-</td></tr><tr><td>L</td><td>CSB</td><td>RS</td><td>SDI (D₇)</td><td>Write Only</td><td>SRCK (D₆)</td></tr></table> In the serial interface mode (P/S="L"), RDB, WRB, D ₀ -D ₅ and D ₈ -D ₁₅ should be fixed to "H" or "L",..			P/S	Chip Select	Display / Instruction	Data	Read /Write	Serial Clock	H	CSB	RS	D ₀ ~ D ₇	RDB, WRB	-	L	CSB	RS	SDI (D ₇)	Write Only	SRCK (D ₆)
P/S	Chip Select	Display / Instruction	Data	Read /Write	Serial Clock																		
H	CSB	RS	D ₀ ~ D ₇	RDB, WRB	-																		
L	CSB	RS	SDI (D ₇)	Write Only	SRCK (D ₆)																		
43-44	RESB	I	Reset																				
31	TEST1	I	Test(Only for maker use) Keep open																				
32	TEST2	O	Test(Only for maker use) Keep open																				
33-34	TEST3	I	Test(Only for maker use) Keep open																				
35-36	TEST4	O	Test(Only for maker use) Keep open																				
129-130	VR	I	Test(Only for maker use) Keep open																				

LCD Output

No.	Terminal	I/O	Description															
335-718	SEGA ₀ ~ SEGA ₁₂₇ , SEGB ₀ ~ SEGB ₁₂₇ , SEGC ₀ ~ SEGC ₁₂₇	O	Segment Drivers Output															
			<table><tr><th>REV Mode</th><th>Turn-off</th><th>Turn-on</th></tr><tr><td>Normal</td><td>0</td><td>1</td></tr><tr><td>Reverse</td><td>1</td><td>0</td></tr></table>	REV Mode	Turn-off	Turn-on	Normal	0	1	Reverse	1	0						
			REV Mode	Turn-off	Turn-on													
			Normal	0	1													
Reverse	1	0																
FRAME signal																		
Display RAM data	Normal mode Reverse mode																	
99-100	CL	O	Normally open.															
101-102	FLM	O	Normally open.															
103-104	FR	O	Normally open.															
4-15 243-254 260-299 305-332 721-748 754-793	COM ₀ ~ COM ₁₅₉	O	Common Divers Output															
			<table><tr><th>Data</th><th>FR</th><th>Output level</th></tr><tr><td>H</td><td>H</td><td>VLCD</td></tr><tr><td>L</td><td>H</td><td>VCL4</td></tr><tr><td>H</td><td>L</td><td>VSS</td></tr><tr><td>L</td><td>L</td><td>VCL1</td></tr></table>	Data	FR	Output level	H	H	VLCD	L	H	VCL4	H	L	VSS	L	L	VCL1
Data	FR	Output level																
H	H	VLCD																
L	H	VCL4																
H	L	VSS																
L	L	VCL1																
41-42	CLK	I	External Reference Clock Input Fix to “L” or “H” when not used															
39-40	OSC2	O	Display Timing Clock Output Internal oscillator wave will be output when MCKSEL is “H”.															

■ ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	CONDITION	TERMINAL	RATING	UNIT
Supply Voltage (1)	V_{DD1}	$V_{SS1} = V_{SS2} =$ $V_{SS3} = 0V$ $T_a = +25^{\circ}C$	V_{DD1}	-0.3 to +4.0	V
Supply Voltage (2)	V_{DD2}		V_{DD2}	-0.3 to +4.0	V
Supply Voltage (3)	V_{DD3}		V_{DD3}	-0.3 to +4.0	V
Supply Voltage (4)	V_{OUT}		V_{OUT}	-0.3 to +20.0	V
Supply Voltage (5)	V_{LCD}		V_{LCD}	-0.3 to +20.0	V
Supply Voltage (6)	$V_{CL1} \sim V_{CL4}$		$V_{CL1} \sim V_{CL4}$	-0.3 to $V_{LCD} + 0.3$	V
Input Voltage	V_I		*1	-0.3 to $V_{DD1} + 0.3$	V
Storage Temperature	T_{stg}			-45 to +125	$^{\circ}C$

*1 D0 ~ D15, CSB, CS2, RS, WRB, RDB, CLK, RESB, TEST1~4 terminals

*2 To stabilize the LSI operation, place decoupling capacitors between V_{DD1} and V_{SS1} , V_{DD2} and V_{SS2} , V_{DD3} and V_{SS3} .

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TERMINAL	MIN	TYP	MAX	UNIT	NOTE
Supply Voltage	V_{DD1}	V_{DD1}	1.7		3.3	V	
	V_{DD2}	V_{DD2}	2.4		3.3	V	
	V_{DD3}	V_{DD3}	2.4		3.3	V	*1
Operating Voltage	V_{OUT}	V_{OUT}	5		18.0	V	*2
	V_{LCD}	V_{LCD}	5		18.0	V	
	V_{REG}	V_{REG}	4.8		6.6	V	
	V_{REF}	V_{REF}	1.0	1.2	1.3	V	*3
Operating Temperature	T_{opr}		-30		85	$^{\circ}C$	

*1. When the Voltage booster is used, V_{DD3} should be used within the limit range, and V_{DD2} can be connected to V_{DD3} .

*2. Please keep the relationship as following shown, $V_{OUT} \geq V_{LCD} > V_{CL1} > V_{CL2} > V_{CL3} > V_{CL4} > V_{SS}$, $V_{OUT} \geq V_{REG} \geq V_{CL2}$, when the internal boosting circuit is not used.

*3. When the internal reference voltage circuit is used, reference voltage V_{REF} should be used within the limit range.

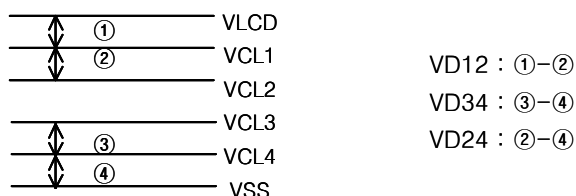
■ DC CHARACTERISTICS

 $V_{SS} = 0V$, $V_{DD1}=+1.7$ to $+3.3V$, $V_{DD2}=+2.4$ to $+3.3V$, $T_a=-30$ to $+85^{\circ}C$

PARAMETER	SYM BOL	CONDITION	MIN	TYP	MAX	UNIT	NOTE
High level input voltage	V_{IH}		$0.8 V_{DD1}$		V_{DD1}	V	*1
Low level input voltage	V_{IL}		0		$0.2V_{DD1}$	V	*1
High level output voltage	V_{OH1}	$I_{OH} = -0.4mA$	$V_{DD1} - 0.4$			V	*2
Low level output voltage	V_{OL1}	$I_{OL} = 0.4mA$			0.4	V	*2
High level output voltage	V_{OH2}	$I_{OH} = -0.1mA$	$V_{DD1} - 0.4$			V	*3
Low level output voltage	V_{OL2}	$I_{OL} = 0.1mA$			0.4	V	*3
Input leakage current	I_{LI}	$V_I = V_{SS1}$ or V_{DD1}		TBD		μA	*4
Output leakage current	I_{LO}	$V_I = V_{SS1}$ or V_{DD1}		TBD		μA	*5
Driver ON-resistance	R_{ON1}	$ \Delta V_{ON} = 0.5V$	$V_{LCD} = 10V$	1	2	k Ω	*6
			$V_{LCD} = 6V$	2	4		
Stand-by current	I_{STB}	$CSB=V_{DD1}$, $T_a=25^{\circ}C$	$V_{DD1} = 3V$	TBD		μA	*7
Internal oscillation Frequency	f_{OSC1}	$V_{DD2} = 3V$ $T_a = 25^{\circ}C$	1572	1850	2127	kHz	*8
	f_{OSC2}		1045	1230	1414		*9
	f_{OSC3}		850	1000	1150		*10
	f_{OSC4}		671.5	790	908.5		*11
Voltage converter output voltage	V_{OUT}	N-time booster (N=2 to 7)	$(N \times V_{DD3}) \times 0.95$			V	*12
Supply current (1)	I_{DD1}	$V_{DD3} = 2.5V$, 7-time booster All ON pattern		TBD		μA	*13
Supply current (2)	I_{DD2}	$V_{DD3} = 2.5V$, 7-time booster Checker pattern		TBD			
Supply current (3)	I_{DD3}	$V_{DD3} = 3V$, 6-time booster All ON pattern		TBD			
Supply current (4)	I_{DD4}	$V_{DD3} = 3V$, 6-time booster Checker pattern		TBD			
Supply current (5)	I_{DD5}	$V_{DD3} = 3V$, 5-time booster All ON pattern		TBD			
Supply current (6)	I_{DD6}	$V_{DD3} = 3V$, 5-time booster Checker pattern		TBD			
Supply current (7)	I_{DD7}	$V_{DD3} = 3V$, 4-time booster All ON pattern		TBD			
Supply current (8)	I_{DD8}	$V_{DD3} = 3V$, 4-time booster Checker pattern		TBD			
Output Voltage	V_{CL2}		-100	0	+100	mV	*14
	V_{CL3}		-100	0	+100		
	V_{D12}		-100	0	+30		
	V_{D34}		-30	0	+30		
	V_{D24}		-30	0	+30		

Applied Terminals (* remark solves)

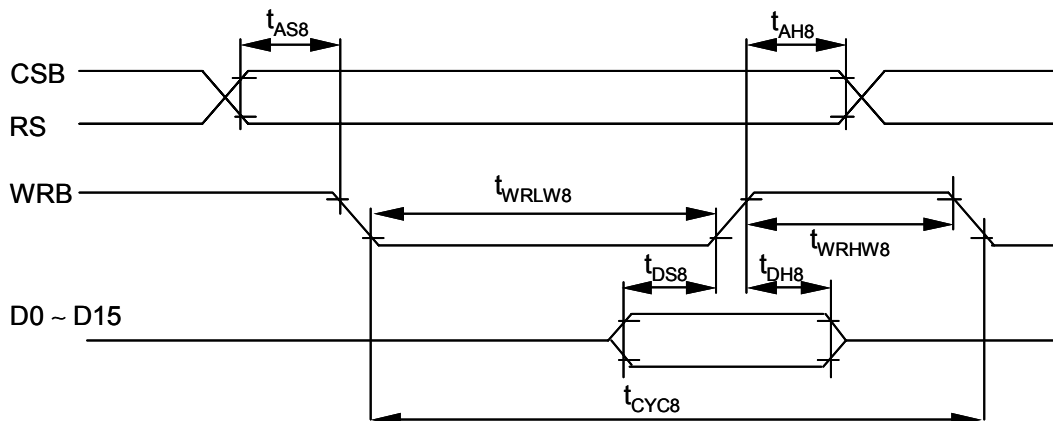
- *1. D0~D15, CSB, RS, RDB, WRB, P/S, SEL68, RESB terminals
- *2. D0~D15 terminals
- *3. OSC2 terminals
- *4. CSB, RS, SEL68, RDB, WRB, P/S, RES, CLK terminals
- *5. Applicable at D0~D15 = high impedance state
- *6. SEGA0~SEGA127, SEGB0~SEGB127, SEGC0~SEGC127, COM0~COM159 terminals
Resistance when being supplied 0.5V between each output terminals and power terminal (VLCD, VCL1, VCL2, VCL3, and VCL4).
Applicable under bias ratio = 1/9
- *7. VDD1 terminal
VDD1 current when source clock is stopped, chip selection (CSB=VDD1) is non- selection state and no load.
- *8. Oscillator frequency when internal oscillator circuit is used.
Applicable under MCLK register of oscillator circuit, {MCLK<7:0>} = "00000000".
- *9. Oscillator frequency when internal oscillator circuit is used.
Applicable under MCLK register of oscillator circuit, {MCLK<7:0>} = "01000000".
- *10. Oscillator frequency when internal oscillator circuit is used.
Applicable under MCLK register of oscillator circuit, {MCLK<7:0>} = "10000000".
- *11. Oscillator frequency when internal oscillator circuit is used.
Applicable under MCLK register of oscillator circuit, {MCLK<7:0>} = "11000000".
- *12. VOUT terminal
N x boosting (N=2~7), applicable under internal oscillator circuit and internal power circuit are ON state.
VDD3 = 2.4~3.3V, electric volume is MAX("11111111").
bias = 1/5~1/12, no load at LCD driver terminal.
CA₁= CA₂=1.0μF, DCON="1", AMPON="1"
- *13. Applicable under internal oscillator circuit and internal power circuit are ON state and no access from CPU.
Electric volume is "11111111".
Display data is all ON or cross check pattern, and no load at LCD driver terminal.
Test condition: VDD2=VDD3, CA₁=CA₂=1.0μF, DCON="1", AMPON="1", T_a=25°C.
- *14. VLCD, VCL1, VCL2, VCL3 and VCL4 terminals.
VDD3 = 3.0V, VOUT=15.0V, bias = 1/5~1/12, electric volume is "11111111"
Display OFF and no load at LCD drive terminal.
Boosting coefficient N is 5 times.
Test condition: CA₁=CA₂=1.0μF, DCON="1", AMPON="1".



■ AC CHARACTERISTICS

(1) Write operation (80-type MPU)

Write Timing-1



(V_{DD}=2.5 to 3.3V, Ta=-30 to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time	t _{AH8}		0		ns	CSB
Address setup time	t _{AS8}		0		ns	RS
System cycle time	t _{CYC8}		90		ns	
Enable "L" level pulse width	t _{WRLW8}		35		ns	WRB
Enable "H" level pulse width	t _{WRHW8}		35		ns	
Data setup time	t _{DS8}		30		ns	D ₀ to D ₁₅
Data hold time	t _{DH8}		5		ns	

(V_{DD}=2.2 to 2.5V, Ta=-30 to +85°C)

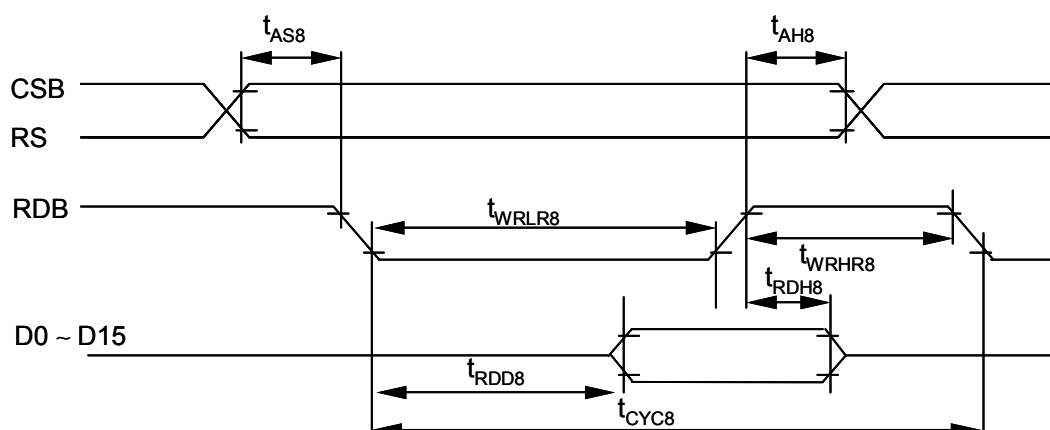
PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time	t _{AH8}		0		ns	CSB
Address setup time	t _{AS8}		0		ns	RS
System cycle time	t _{CYC8}		160		ns	
Enable "L" level pulse width	t _{WRLW8}		70		ns	WRB
Enable "H" level pulse width	t _{WRHW8}		70		ns	
Data setup time	t _{DS8}		40		ns	D ₀ to D ₁₅
Data hold time	t _{DH8}		5		ns	

(V_{DD}=1.7 to 2.2V, Ta=-30 to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time	t _{AH8}		0		ns	CSB
Address setup time	t _{AS8}		0		ns	RS
System cycle time	t _{CYC8}		180		ns	
Enable "L" level pulse width	t _{WRLW8}		80		ns	WRB
Enable "H" level pulse width	t _{WRHW8}		80		ns	
Data setup time	t _{DS8}		70		ns	D ₀ to D ₁₅
Data hold time	t _{DH8}		10		ns	

Note) Each timing is specified based on 20% and 80% of V_{DD1}.

(2) Read operation (80-type MPU)



($V_{DD}=2.5$ to $3.3V$, $T_a=-30$ to $+85^{\circ}C$)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time	t_{AH8}		0		ns	CSB
Address setup time	t_{AS8}		0		ns	RS
System cycle time	t_{CYC8}		180		ns	
Enable "L" level pulse width	t_{WRLR8}		80		ns	RDB
Enable "H" level pulse width	t_{WRHR8}		80		ns	
Read Data delay time	T_{RDD8}	CL=15pF		60	ns	D ₀ to D ₁₅
Read Data hold time	T_{RDH8}		10		ns	

($V_{DD}=2.2$ to $2.5V$, $T_a=-30$ to $+85^{\circ}C$)

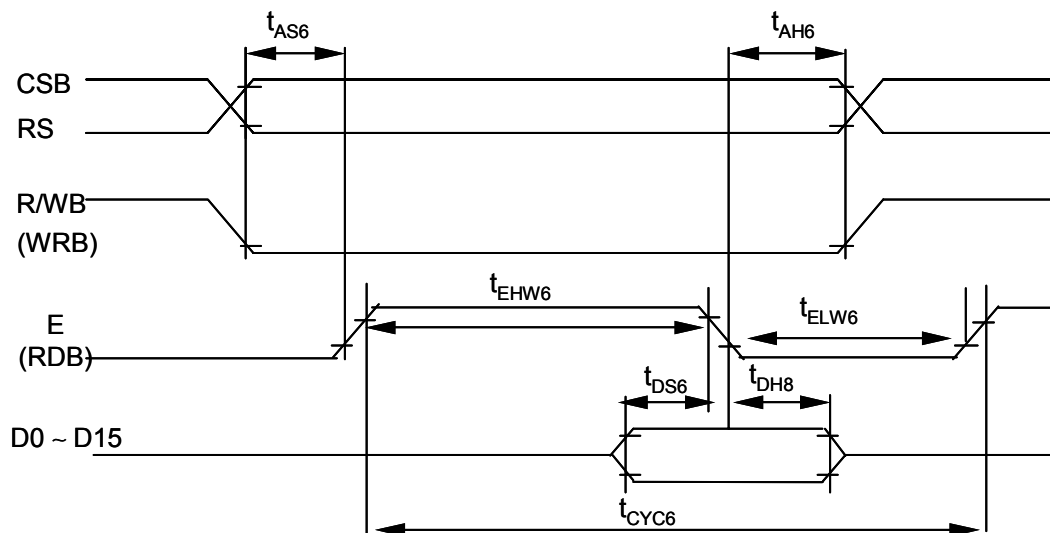
PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time	t_{AH8}		0		ns	CSB
Address setup time	t_{AS8}		0		ns	RS
System cycle time	t_{CYC8}		180		ns	
Enable "L" level pulse width	t_{WRLR8}		80		ns	RDB
Enable "H" level pulse width	t_{WRHR8}		80		ns	
Read Data delay time	t_{RDD8}	CL=15pF		60	ns	D ₀ to D ₁₅
Read Data hold time	t_{RDH8}		10		ns	

($V_{DD}=1.7$ to $2.2V$, $T_a=-30$ to $+85^{\circ}C$)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time	t_{AH8}		0		ns	CSB
Address setup time	t_{AS8}		0		ns	RS
System cycle time	t_{CYC8}		250		ns	
Enable "L" level pulse width	t_{WRLR8}		120		ns	RDB
Enable "H" level pulse width	t_{WRHR8}		120		ns	
Read Data delay time	t_{RDD8}	CL=15pF		110	ns	D ₀ to D ₁₅
Read Data hold time	t_{RDH8}		10		ns	

Note) Each timing is specified based on 20% and 80% of V_{DD1} .

(3) Write operation (68-type MPU)

(V_{DD}=2.5 to 3.3V, Ta=-30 to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time	t_{AH6}		0		ns	CSB
Address setup time	t_{AS6}		0		ns	RS
System cycle time	t_{CYC6}		90		ns	E
Enable "L" level pulse width	t_{ELW6}		35		ns	
Enable "H" level pulse width	t_{EHW6}		35		ns	
Data setup time	t_{DS6}		40		ns	D ₀ to D ₁₅
Data hold time	t_{DH6}		5		ns	

(V_{DD1}=2.2 to 2.5V, Ta=-30 to +85°C)

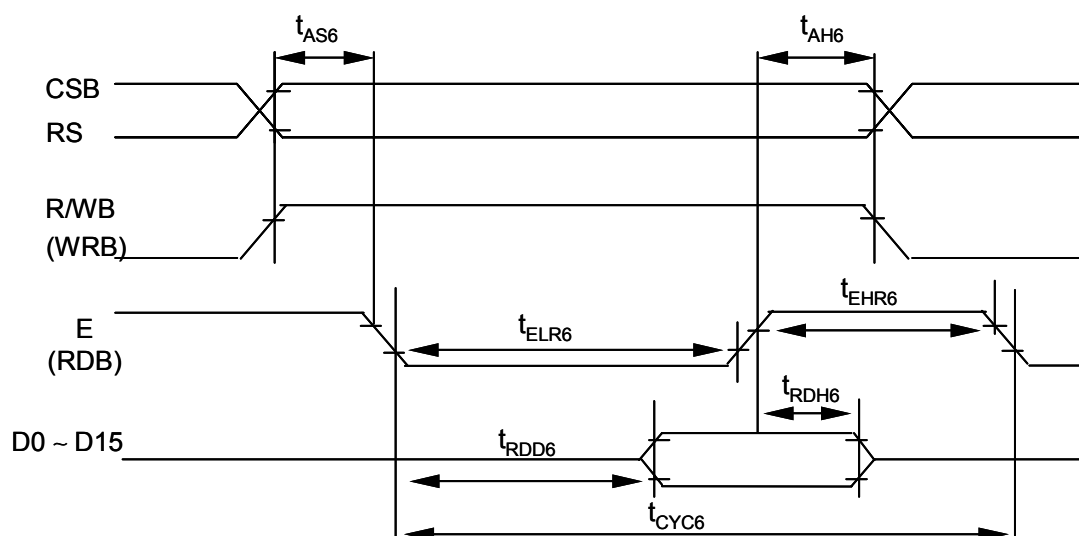
PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time	t_{AH6}		0		ns	CSB
Address setup time	t_{AS6}		0		ns	RS
System cycle time	t_{CYC6}		160		ns	E
Enable "L" level pulse width	t_{ELW6}		70		ns	
Enable "H" level pulse width	t_{EHW6}		70		ns	
Data setup time	t_{DS6}		50		ns	D ₀ to D ₁₅
Data hold time	t_{DH6}		10		ns	

(V_{DD1}=1.7 to 2.2V, Ta=-30 to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time	t_{AH6}		0		ns	CSB
Address setup time	t_{AS6}		0		ns	RS
System cycle time	t_{CYC6}		180		ns	E
Enable "L" level pulse width	t_{ELW6}		80		ns	
Enable "H" level pulse width	t_{EHW6}		80		ns	
Data setup time	t_{DS6}		70		ns	D ₀ to D ₁₅
Data hold time	t_{DH6}		10		ns	

Note) Each timing is specified based on 20% and 80% of V_{DD1}.

(4) Read operation (68-type MPU)



($V_{DD1}=2.5$ to $3.3V$, $T_a=-30$ to $+85^{\circ}C$)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time	t_{AH6}		0		ns	CSB
Address setup time	t_{AS6}		0		ns	RS
System cycle time	t_{CYC6}		180		ns	
Enable "L" level pulse width	t_{ELR6}		80		ns	E
Enable "H" level pulse width	t_{EHR6}		80		ns	
Read Data delay time	t_{RDD6}	CL=15pF	0	70	ns	D ₀ to D ₁₅
Read Data hold time	t_{RDH6}		0		ns	

($V_{DD1}=2.2$ to $2.5V$, $T_a=-30$ to $+85^{\circ}C$)

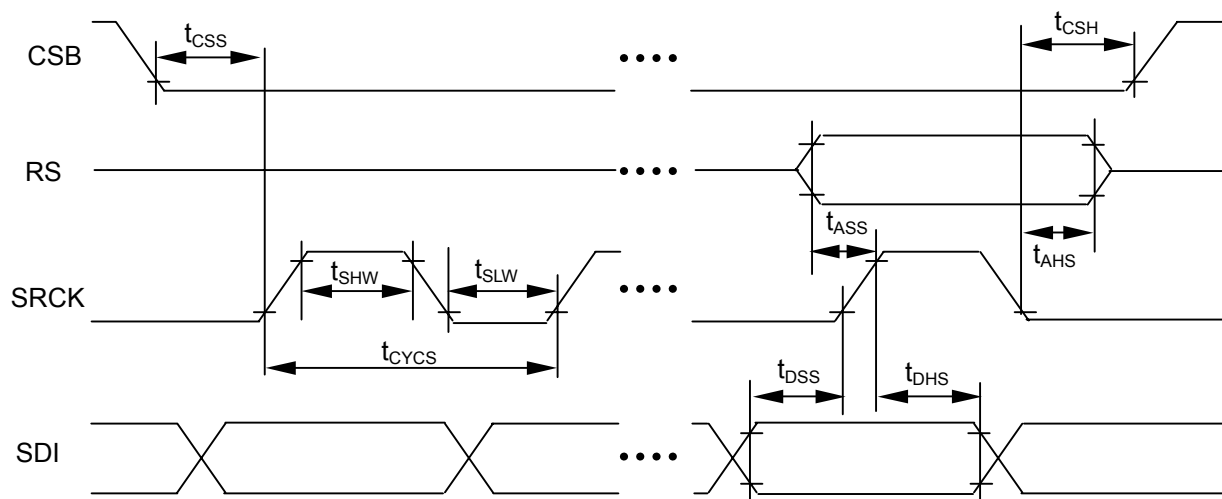
PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time	t_{AH6}		0		ns	CSB
Address setup time	t_{AS6}		0		ns	RS
System cycle time	t_{CYC6}		180		ns	
Enable "L" level pulse width	t_{ELR6}		80		ns	E
Enable "H" level pulse width	t_{EHR6}		80		ns	
Read Data delay time	t_{RDD6}	CL=15pF	0	70	ns	D ₀ to D ₁₅
Read Data hold time	t_{RDH6}		0		ns	

($V_{DD1}=1.7$ to $2.2V$, $T_a=-30$ to $+85^{\circ}C$)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time	t_{AH6}		0		ns	CSB
Address setup time	t_{AS6}		0		ns	RS
System cycle time	t_{CYC6}		250		ns	
Enable "L" level pulse width	t_{ELR6}		120		ns	E
Enable "H" level pulse width	t_{EHR6}		120		ns	
Read Data delay time	t_{RDD6}	CL=15pF	10	110	ns	D ₀ to D ₁₅
Read Data hold time	t_{RDH6}		10		ns	

Note) Each timing is specified based on 20% and 80% of V_{DD1} .

(5) Serial interface

(V_{DD1}=2.5 to 3.3V, Ta=-30 to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Serial clock cycle	t _{CYCS}		50		ns	
SRCK "H" level pulse width	t _{SHW}		20		ns	SRCK
SRCK "L" level pulse width	t _{SLW}		20		ns	
Address setup time	t _{ASS}		20		ns	RS
Address hold time	t _{AHS}		20		ns	
Data setup time	t _{DSS}		20		ns	SDI
Data hold time	t _{DHS}		20		ns	
CSB – SRCK time	t _{CSS}		20		ns	CSB
CSB hold time	t _{CSH}		20		ns	

(V_{DD1}=2.2 to 2.5V, Ta=-30 to +85°C)

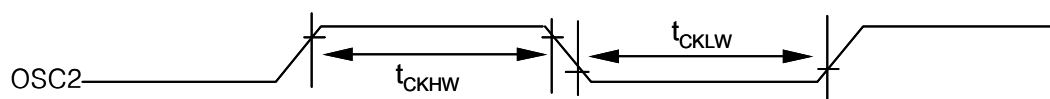
PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Serial clock cycle	t _{CYCS}		50		ns	
SRCK "H" level pulse width	t _{SHW}		20		ns	SRCK
SRCK "L" level pulse width	t _{SLW}		20		ns	
Address setup time	t _{ASS}		20		ns	RS
Address hold time	t _{AHS}		20		ns	
Data setup time	t _{DSS}		20		ns	SDI
Data hold time	t _{DHS}		20		ns	
CSB – SRCK time	t _{CSS}		20		ns	CSB
CSB hold time	t _{CSH}		20		ns	

(V_{DD1}=1.7 to 2.2V, Ta=-30 to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Serial clock cycle	t _{CYCS}		80		ns	
SRCK "H" level pulse width	t _{SHW}		35		ns	SRCK
SRCK "L" level pulse width	t _{SLW}		35		ns	
Address setup time	t _{ASS}		35		ns	RS
Address hold time	t _{AHS}		35		ns	
Data setup time	t _{DSS}		5		ns	SDI
Data hold time	t _{DHS}		35		ns	
CSB – SRCK time	t _{CSS}		35		ns	CSB
CSB hold time	t _{CSH}		35		ns	

Note) Each timing is specified based on 20% and 80% of V_{DD1}.

(6) Source Clock timing

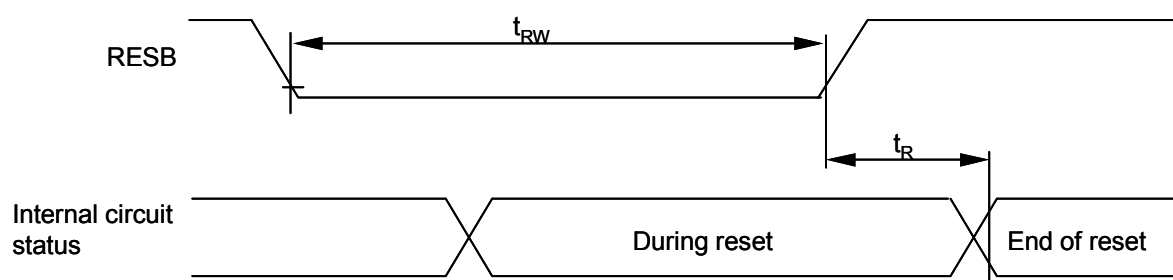


($V_{DD2}=2.4$ to $3.3V$, $T_a=-30$ to $+85^{\circ}C$)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
OSC2 "H" level pulse width (1)	t_{CKHW}	MCLK<7:0>="00000000"	0.235	0.318	μs	OSC2
OSC2 "L" level pulse width (1)	t_{CKLW}		0.235	0.318	μs	
OSC2 "H" level pulse width (2)	t_{CKHW}	MCLK<7:0>="01000000"	0.353	0.478	μs	OSC2
OSC2 "L" level pulse width (2)	t_{CKLW}		0.353	0.478	μs	
OSC2 "H" level pulse width (3)	t_{CKHW}	MCLK<7:0>="10000000"	0.434	0.588	μs	OSC2
OSC2 "L" level pulse width (3)	t_{CKLW}		0.434	0.588	μs	
OSC2 "H" level pulse width (4)	t_{CKHW}	MCLK<7:0>="11000000"	0.55	0.744	μs	OSC2
OSC2 "L" level pulse width (4)	t_{CKLW}		0.55	0.744	μs	

Note) Each timing is specified based on 20% and 80% of V_{DD1} .

(7) Reset input timing



($V_{DD1}=2.4$ to $3.3V$, $T_a=-30$ to $+85^{\circ}C$)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	Terminal
Reset time	t_R			1.0	μs	
RESB "L" level pulse width	t_{RW}		10.0		μs	RESB

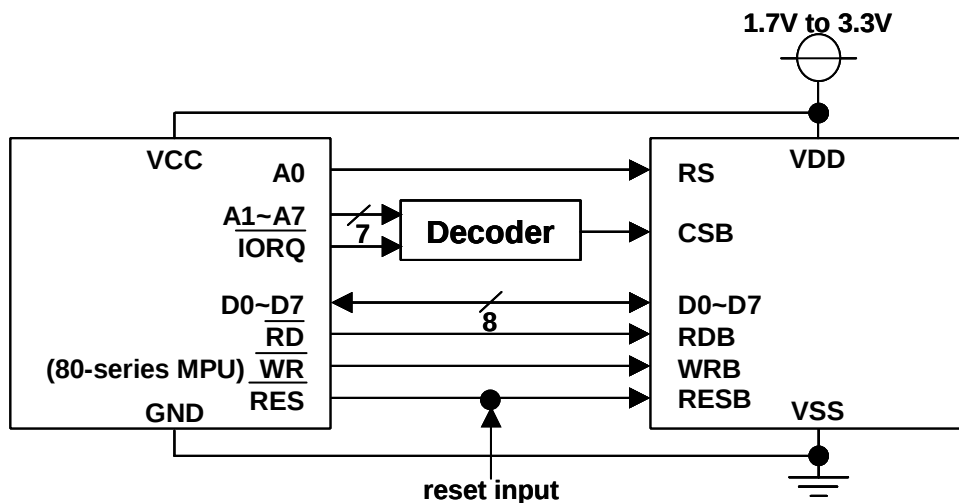
($V_{DD1}=1.7$ to $2.4V$, $T_a=-30$ to $+85^{\circ}C$)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	Terminal
Reset time	t_R			1.5	μs	
RESB "L" level pulse width	t_{RW}		10.0		μs	RESB

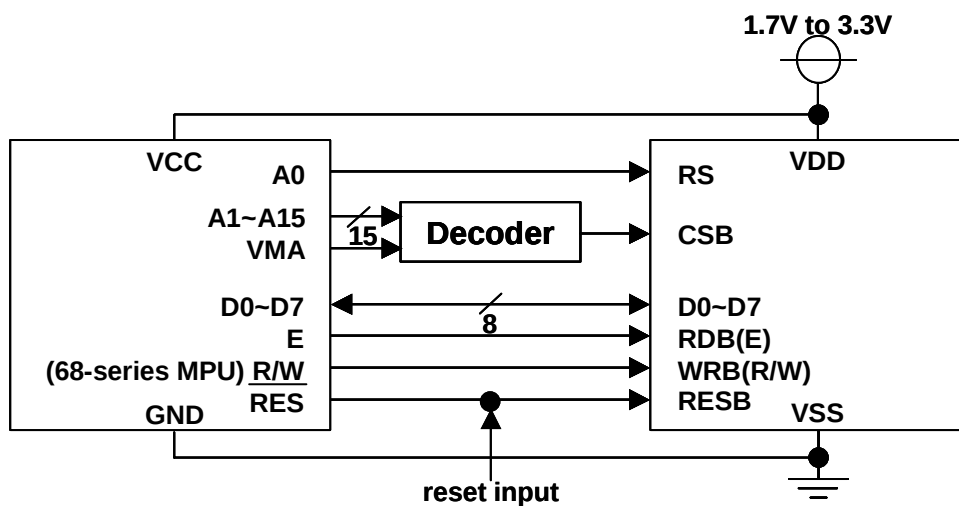
Note) Each timing is specified based on 20% and 80% of V_{DD1} .

■ MPU Connections

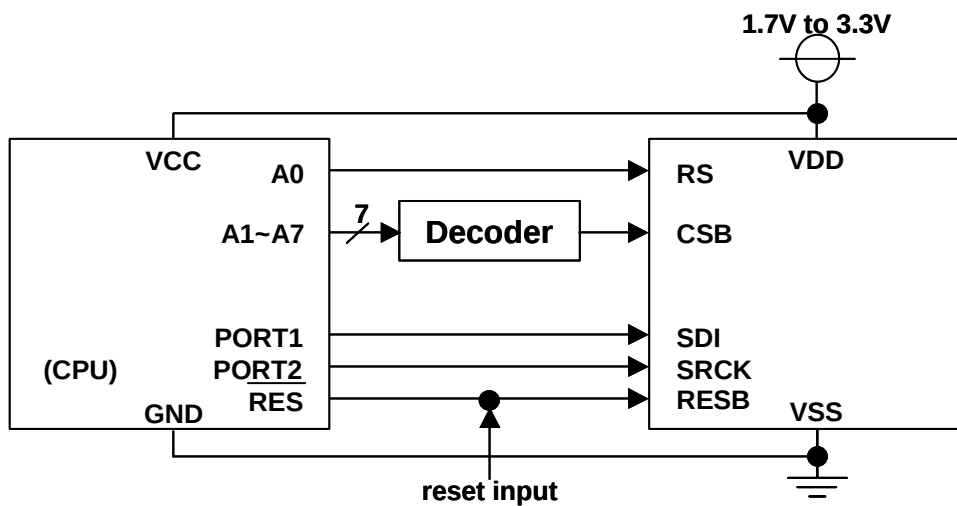
80-type MPU interface



68-type MPU interface



Serial interface



[CAUTION]

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