



TRIPLE D FLIP-FLOP

SY100S331

FEATURES

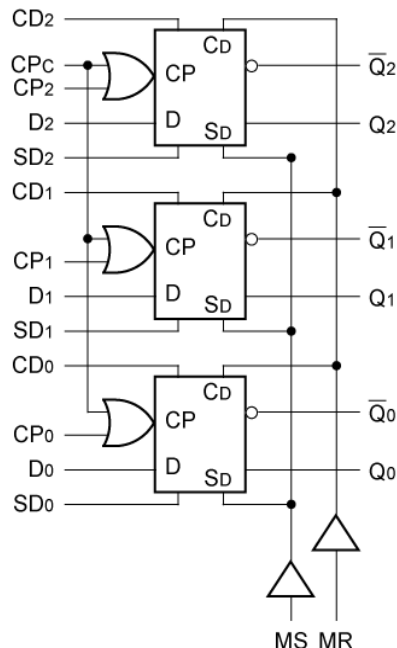
- Max. toggle frequency of 800MHz
- Differential outputs
- IEE min. of -80mA
- Industry standard 100K ECL levels
- Extended supply voltage option:
VEE = -4.2V to -5.5V
- Voltage and temperature compensation for improved noise immunity
- Internal 75kΩ input pull-down resistors
- 150% faster than Fairchild
- 40% lower power than Fairchild
- Function and pinout compatible with Fairchild F100K
- Available in 28-pin PLCC package

DESCRIPTION

The SY100S331 offers three D-type, edge-triggered master/slave flip-flops with true and complement outputs, designed for use in high-performance ECL systems. Each flip-flop is controlled by a common clock (CP_c), as well as its own clock pulse (CP_n). The resultant clock signal controlling the flip-flop is the logical OR operation of these two clock signals. Data enters the master when both CP_c and CP_n are LOW and enters the slave on the rising edge of either CP_c or CP_n (or both).

Additional control signals include Master Set (MS) and Master Reset (MR) inputs. Each flip-flop also has its own Direct Set (SD_n) and Direct Clear (CD_n) signals. The MR, MS, SD_n and DC_n signals override the clock signals. The inputs on this device have 75kΩ pull-down resistors.

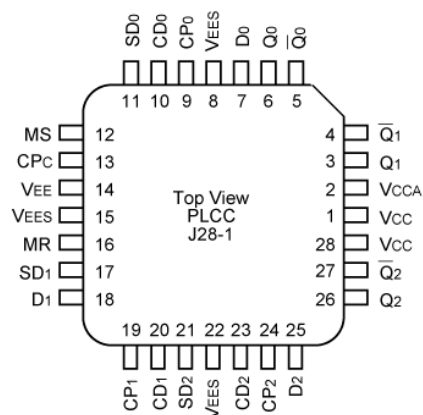
BLOCK DIAGRAM



PIN NAMES

Pin	Function
CP ₀ – CP ₂	Individual Clock Inputs
CP _c	Common Clock Input
D ₀ – D ₂	Data Inputs
CD ₀ – CD ₂	Individual Direct Clear Inputs
SD _n	Individual Direct Set Inputs
MR	Master Reset Input
MS	Master Set Input
Q ₀ – Q ₂	Data Outputs
\bar{Q}_0 – \bar{Q}_2	Complementary Data Outputs
VEES	VEE Substrate
VCCA	VCCO for ECL Outputs

PACKAGE/ORDERING INFORMATION



28-Pin PLCC (J28-1)

Ordering Information

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY100S331JC	J28-1	Commercial	SY100S331JC	Sn-Pb
SY100S331JCTR ⁽¹⁾	J28-1	Commercial	SY100S331JC	Sn-Pb
SY100S331JZ ⁽²⁾	J28-1	Commercial	SY100S331JZ with Pb-Free bar-line indicator	Matte-Sn
SY100S331JZTR ^(1, 2)	J28-1	Commercial	SY100S331JZ with Pb-Free bar-line indicator	Matte-Sn
SY100S331JY ⁽²⁾	J28-1	Industrial	SY100S331JY with Pb-Free bar-line indicator	Matte-Sn
SY100S331JYTR ^(1, 2)	J28-1	Industrial	SY100S331JY with Pb-Free bar-line indicator	Matte-Sn

Notes:

1. Tape and Reel.
2. Pb-Free package is recommended for new designs.

TRUTH TABLES

Asynchronous Operation ⁽¹⁾					
Inputs					Outputs
D _n	CP _n	CP _c	MS SD _n	MR DC _n	Q _n (t+1)
X	X	X	H	L	H
X	X	X	L	H	L
X	X	X	H	H	U

NOTE:

1. H = High Voltage Level, L = Low Voltage Level, X = Don't Care, U = Undefined, t = Time before CP Positive Transition, t+1 = Time after CP Positive Transition, u = Low-to-High Transition

Synchronous Operation ⁽¹⁾					
Inputs					Outputs
D _n	CP _n	CP _c	MS SD _n	MR DC _n	Q _n
L	u	L	L	L	L
H	u	L	L	L	H
L	L	u	L	L	L
H	L	u	L	L	H
X	L	L	L	L	Q _n (t)
X	H	X	L	L	Q _n (t)
X	X	H	L	L	Q _n (t)

NOTE:

1. H = High Voltage Level, L = Low Voltage Level, X = Don't Care, U = Undefined, t = Time before CP Positive Transition, t+1 = Time after CP Positive Transition, u = Low-to-High Transition

DC ELECTRICAL CHARACTERISTICS

$V_{EE} = -4.2V$ to $-5.5V$ unless otherwise specified, $V_{CC} = V_{CCA} = GND$

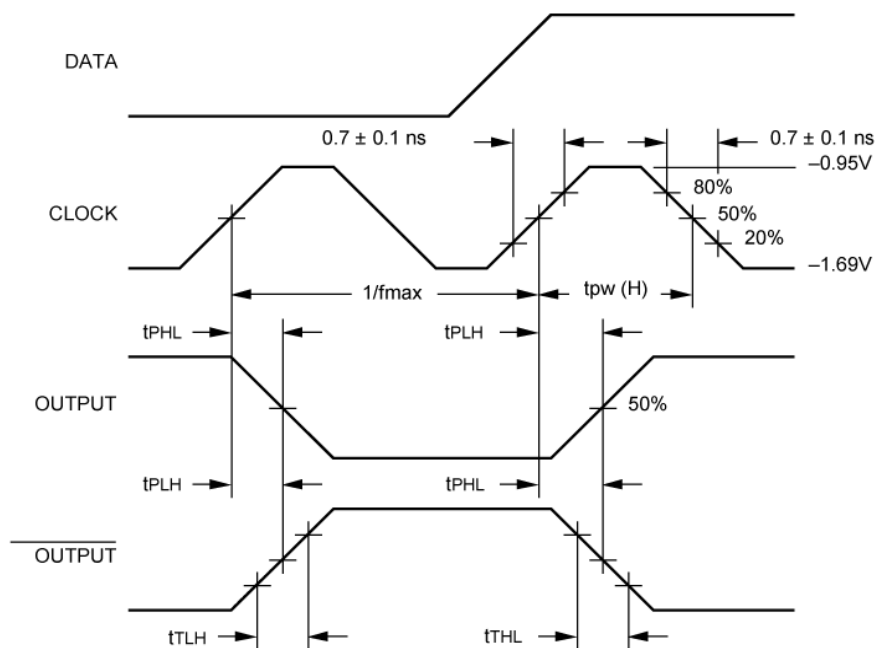
Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
I_{IH}	Input HIGH Current, All Inputs	—	—	200	μA	$V_{IN} = V_{IH} (Max.)$
I_{EE}	Power Supply Current	-80	-65	-35	mA	Inputs Open

AC ELECTRICAL CHARACTERISTICS

$V_{EE} = -4.2V$ to $-5.5V$ unless otherwise specified, $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_A = -40^{\circ}C$		$T_A = 0^{\circ}C$		$T_A = +25^{\circ}C$		$T_A = +85^{\circ}C$		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
f_{max}	Toggle Frequency	800	—	800	—	800	—	800	—	MHz	
t_{PLH} t_{PHL}	Propagation Delay CP _c to Output	300	700	300	700	300	700	300	700	ps	
t_{PLH} t_{PHL}	Propagation Delay CP _n to Output	300	700	300	700	300	700	300	700	ps	
t_{PLH} t_{PHL}	Propagation Delay CD _n , SD _n to Output	300	800	300	800	300	800	300	800	ps	
t_{PLH} t_{PHL}	Propagation Delay MS, MR to Output	300	900	300	900	300	900	300	900	ps	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	300	900	ps	
t_s	Set-up Time D _n CD _n , SD _n (Release Time) MS, MR (Release Time)	400 500 800	— — —	400 500 800	— — —	400 500 800	— — —	400 500 800	— — —	ps	
t_H	Hold Time D _n	300	—	300	—	300	—	300	—	ps	
$t_{pw} (H)$	Pulse Width HIGH CP _n , CP _c , DC _n SD _n , MR, MS	800	—	800	—	800	—	800	—	ps	

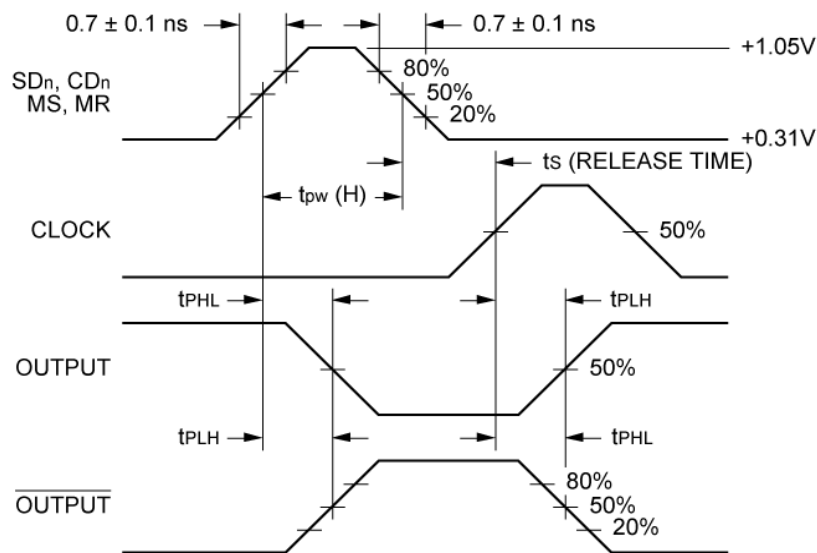
TIMING DIAGRAMS



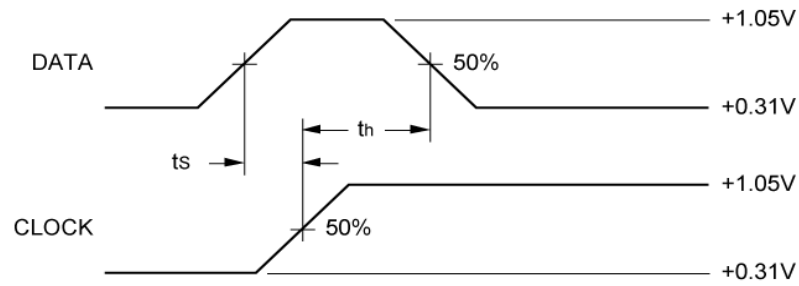
Propagation Delay (Clock) and Transition Times

Note:

$V_{EE} = -4.2V$ to $-5.5V$ unless otherwise specified, $V_{CC} = V_{CCA} = GND$



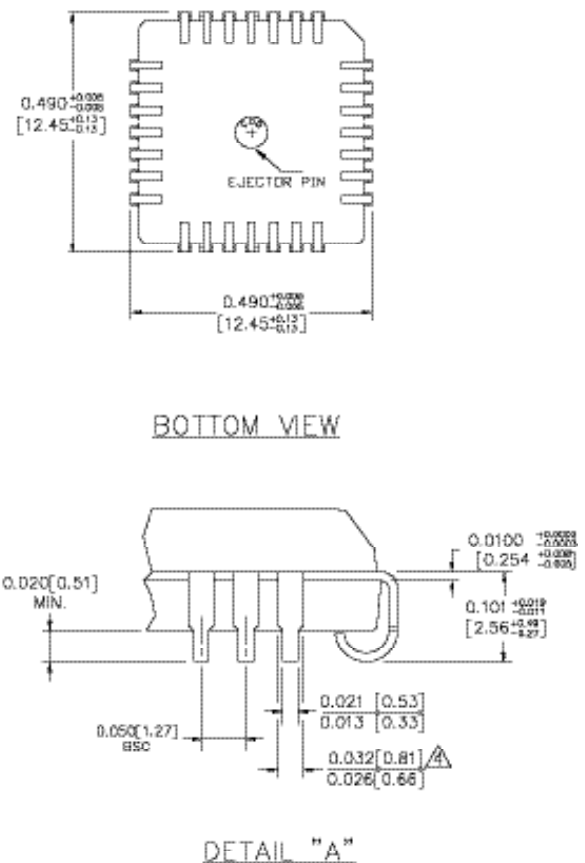
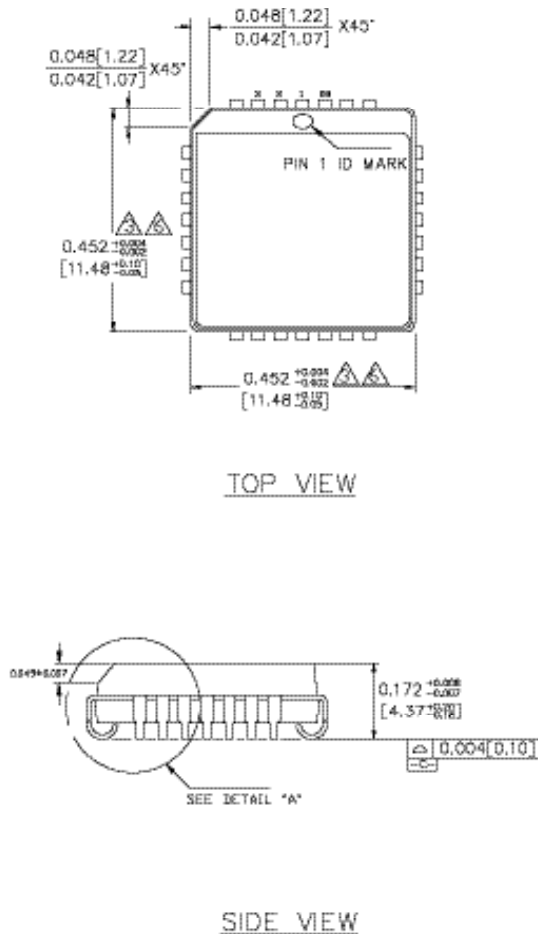
Propagation Delay (Sets and Resets)

TIMING DIAGRAMS**Data Setup and Hold Time****Notes:**

t_s is the minimum time before the transition of the clock that information must be present at the data input.

t_h is the minimum time after the transition of the clock that information must remain unchanged at the data input.

28-PIN PLCC (J28-1)



NOTES:

1. DIMENSIONS ARE IN INCHES [MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.008 [0.203].
4. LEAD DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION.
5. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX/MIN
6. PACKAGE TOP DIMENSION MAY BE SLIGHTLY SMALLER THAN BOTTOM DIMENSION.

Rev. A

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