

DDR SDRAM SODIMM

MT9VDDT1672H – 128MB¹

MT9VDDT3272H – 256MB

MT9VDDT6472H – 512MB

For component data sheets, refer to Micron's Web site: www.micron.com

Features

- 200-pin, small-outline dual in-line memory module (SODIMM)
- Fast data transfer rates: PC2100, PC2700, or PC3200
- 128MB (16 Meg x 72), 256MB (32 Meg x 72), and 512MB (64 Meg x 72)
- Supports ECC error detection and correction
- $V_{DD} = V_{DDQ} = 2.5V$ (-40B: $V_{DD} = V_{DDQ} = 2.6V$)
- $V_{DDSPD} = 2.3\text{--}3.6V$
- 2.5V I/O (SSTL_2-compatible)
- Internal, pipelined double data rate (DDR) architecture; two data accesses per clock cycle
- Bidirectional data strobe (DQS) transmitted/received with data—that is, source-synchronous data capture
- Differential clock inputs (CK and CK#)
- Multiple internal device banks for concurrent operation
- Selectable burst lengths (BL) 2, 4, or 8
- Auto precharge option
- Auto refresh and self refresh modes: 15.625 μ s (128MB) and 7.8125 μ s (256MB, 512MB) maximum average periodic refresh interval
- Serial presence-detect (SPD) with EEPROM
- Selectable CAS latency (CL) for maximum compatibility
- Single rank
- Gold edge contacts

200-Pin SODIMM (MO-224) Figures

Figure 1: Low-Profile Layout

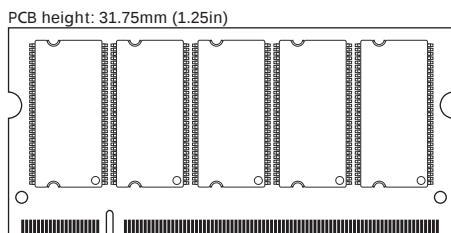
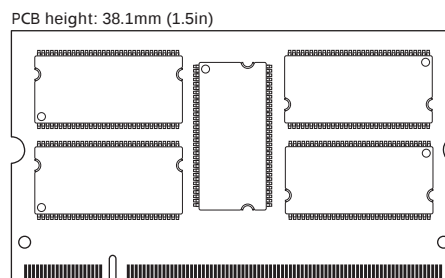


Figure 2: Standard Layout



Options

- Operating temperature²
 - Commercial ($0^{\circ}C \leq T_A \leq +70^{\circ}C$)
 - Industrial ($-40^{\circ}C \leq T_A \leq +85^{\circ}C$)
- Package
 - 200-pin DIMM (standard)
 - 200-pin DIMM (Pb-free)
- Memory clock, speed, CAS latency
 - 5.0ns (200 MHz), 400 MT/s, CL = 3.0
 - 6.0ns (167 MHz), 333 MT/s, CL = 2.5
 - 7.5ns (133 MHz), 266 MT/s, CL = 2.0³
 - 7.5ns (133 MHz), 266 MT/s, CL = 2.0³
 - 7.5ns (133 MHz), 266 MT/s, CL = 2.5³

Marking

None
I
G
Y

Notes: 1. End of life.

2. Contact Micron for industrial temperature module offerings.

3. Not recommended for new designs.



128MB, 256MB, 512MB (x72, ECC, SR) 200-Pin DDR SODIMM Features

Table 1: Key Timing Parameters

Speed Grade	Industry Nomenclature	Data Rate (MT/s)			t_{RCD} (ns)	t_{RP} (ns)	t_{RC} (ns)	Notes
		CL = 3	CL = 2.5	CL = 2				
-40B	PC3200	400	333	266	15	15	55	
-335	PC2700	–	333	266	18	18	60	1
-262	PC2100	–	266	266	15	15	60	
-26A	PC2100	–	266	266	20	20	65	
-265	PC2100	–	266	200	20	20	65	

Notes: 1. The values of t_{RCD} and t_{RP} for -335 modules show 18ns to align with industry specifications; actual DDR SDRAM device specifications are 15ns.

Table 2: Addressing

Parameter	128MB	256MB	512MB
Refresh count	4K	8K	8K
Row address	8K (A[11:0])	8K (A[12:0])	8K (A[12:0])
Device bank address	4 (BA[1:0])	4 (BA[1:0])	4 (BA[1:0])
Device configuration	128Mb (16 Meg x 8)	256Mb (32 Meg x 8)	512Mb (64 Meg x 8)
Column address	1K (A[9:0])	1K (A[9:0])	2K (A[11, 9:0])
Module rank address	1 (S0#)	1 (S0#)	1 (S0#)

Table 3: Part Numbers and Timing Parameters – 128MB Modules

Base device: MT46V16M8,¹ 128Mb DDR SDRAM

Part Number ²	Module Density	Configuration	Module Bandwidth	Memory Clock/Data Rate	Clock Cycles (CL- t_{RCD} - t_{RP})
MT9VDDT1672HG-335__	128MB	16 Meg x 72	2.7 GB/s	6.0ns/333 MT/s	2.5-3-3
MT9VDDT1672HY-335__	128MB	16 Meg x 72	2.7 GB/s	6.0ns/333 MT/s	2.5-3-3
MT9VDDT1672HY-262__	128MB	16 Meg x 72	2.1 GB/s	7.5ns/266 MT/s	2-2-2
MT9VDDT1672HG-26A__	128MB	16 Meg x 72	2.1 GB/s	7.5ns/266 MT/s	2-3-3
MT9VDDT1672HG-265__	128MB	16 Meg x 72	2.1 GB/s	7.5ns/266 MT/s	2.5-3-3

Table 4: Part Numbers and Timing Parameters – 256MB Modules

Base device: MT46V32M8,¹ 256Mb DDR SDRAM

Part Number ²	Module Density	Configuration	Module Bandwidth	Memory Clock/Data Rate	Clock Cycles (CL- t_{RCD} - t_{RP})
MT9VDDT3272HG-40B__	256MB	32 Meg x 72	3.2 GB/s	5.0ns/400 MT/s	3-3-3
MT9VDDT3272HY-40B__	256MB	32 Meg x 72	3.2 GB/s	5.0ns/400 MT/s	3-3-3
MT9VDDT3272HG-335__	256MB	32 Meg x 72	2.7 GB/s	6.0ns/333 MT/s	2.5-3-3
MT9VDDT3272H(I)Y-335__	256MB	32 Meg x 72	2.7 GB/s	6.0ns/333 MT/s	2.5-3-3
MT9VDDT3272HG-262__	256MB	32 Meg x 72	2.1 GB/s	7.5ns/266 MT/s	2-2-2
MT9VDDT3272HG-265__	256MB	32 Meg x 72	2.1 GB/s	7.5ns/266 MT/s	2.5-3-3
MT9VDDT3272HY-265__	256MB	32 Meg x 72	2.1 GB/s	7.5ns/266 MT/s	2.5-3-3



128MB, 256MB, 512MB (x72, ECC, SR) 200-Pin DDR SODIMM Features

Table 5: Part Numbers and Timing Parameters – 512MB Modules

Base device: MT46V64M8,¹ 512Mb DDR SDRAM

Part Number ²	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Clock Cycles (CL- ^t RCD- ^t RP)
MT9VDDT6472HG-40B__	512MB	64 Meg x 72	3.2 GB/s	5.0ns/400 MT/s	3-3-3
MT9VDDT6472HY-40B__	512MB	64 Meg x 72	3.2 GB/s	5.0ns/400 MT/s	3-3-3
MT9VDDT6472HG-335__	512MB	64 Meg x 72	2.7 GB/s	6.0ns/333 MT/s	2.5-3-3
MT9VDDT6472H(I)Y-335__	512MB	64 Meg x 72	2.7 GB/s	6.0ns/333 MT/s	2.5-3-3
MT9VDDT6472HG-26A__	512MB	64 Meg x 72	2.1 GB/s	7.5ns/266 MT/s	2-3-3
MT9VDDT6472HG-265__	512MB	64 Meg x 72	2.1 GB/s	7.5ns/266 MT/s	2.5-3-3

- Notes:
1. Data sheets for the base devices can be found on Micron's Web site.
 2. All part numbers end with a two-place code (not shown) that designates component and PCB revisions. Consult factory for current revision codes. Example: MT9VDDT6472HY-335J1.



128MB, 256MB, 512MB (x72, ECC, SR) 200-Pin DDR SODIMM Pin Assignments and Descriptions

Pin Assignments and Descriptions

Table 6: Pin Assignments

200-Pin SODIMM Front								200-Pin SODIMM Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	V _{REF}	51	V _{SS}	101	A9	151	DQ42	2	V _{REF}	52	V _{SS}	102	A8	152	DQ46
3	V _{SS}	53	DQ19	103	V _{SS}	153	DQ43	4	V _{SS}	54	DQ23	104	V _{SS}	154	DQ47
5	DQ0	55	DQ24	105	A7	155	V _{DD}	6	DQ4	56	DQ28	106	A6	156	V _{DD}
7	DQ1	57	V _{DD}	107	A5	157	V _{DD}	8	DQ5	58	V _{DD}	108	A4	158	CK1#
9	V _{DD}	59	DQ25	109	A3	159	V _{SS}	10	V _{DD}	60	DQ29	110	A2	160	CK1
11	DQS0	61	DQS3	111	A1	161	V _{SS}	12	DM0	62	DM3	112	A0	162	V _{SS}
13	DQ2	63	V _{SS}	113	V _{DD}	163	DQ48	14	DQ6	64	V _{SS}	114	V _{DD}	164	DQ52
15	V _{SS}	65	DQ26	115	A10	165	DQ49	16	V _{SS}	66	DQ30	116	BA1	166	DQ53
17	DQ3	67	DQ27	117	BA0	167	V _{DD}	18	DQ7	68	DQ31	118	RAS#	168	V _{DD}
19	DQ8	69	V _{DD}	119	WE#	169	DQS6	20	DQ12	70	V _{DD}	120	CAS#	170	DM6
21	V _{DD}	71	CB0	121	S0#	171	DQ50	22	V _{DD}	72	CB4	122	NC	172	DQ54
23	DQ9	73	CB1	123	NC	173	V _{SS}	24	DQ13	74	CB5	124	NC	174	V _{SS}
25	DQS1	75	V _{SS}	125	V _{SS}	175	DQ51	26	DM1	76	V _{SS}	126	V _{SS}	176	DQ55
27	V _{SS}	77	DQS8	127	DQ32	177	DQ56	28	V _{SS}	78	DM8	128	DQ36	178	DQ60
29	DQ10	79	CB2	129	DQ33	179	V _{DD}	30	DQ14	80	CB6	130	DQ37	180	V _{DD}
31	DQ11	81	V _{DD}	131	V _{DD}	181	DQ57	32	DQ15	82	V _{DD}	132	V _{DD}	182	DQ61
33	V _{DD}	83	CB3	133	DQS4	183	DQS7	34	V _{DD}	84	CB7	134	DM4	184	DM7
35	CK0	85	NC	135	DQ34	185	V _{SS}	36	V _{DD}	86	NC	136	DQ38	186	V _{SS}
37	CK0#	87	V _{SS}	137	V _{SS}	187	DQ58	38	V _{SS}	88	V _{SS}	138	V _{SS}	188	DQ62
39	V _{SS}	89	CK2	139	DQ35	189	DQ59	40	V _{SS}	90	V _{SS}	140	DQ39	190	DQ63
41	DQ16	91	CK2#	141	DQ40	191	V _{DD}	42	DQ20	92	V _{DD}	142	DQ44	192	V _{DD}
43	DQ17	93	V _{DD}	143	V _{DD}	193	SDA	44	DQ21	94	V _{DD}	144	V _{DD}	194	SA0
45	V _{DD}	95	NC	145	DQ41	195	SCL	46	V _{DD}	96	CKE0	146	DQ45	196	SA1
47	DQS2	97	NC	147	DQS5	197	V _{DDSPD}	48	DM2	98	NC	148	DM5	198	SA2
49	DQ18	99 ¹	NC/A12	149	V _{SS}	199	NC	50	DQ22	100	A11	150	V _{SS}	200	NC

Notes: 1. Pin 99 is NC for 128MB and A12 for 256MB and 512MB.

Table 7: Pin Descriptions

Symbol	Type	Description
A[12:0]	Input	Address inputs: Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective device bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one device bank (A10 LOW, device bank selected by BA[1:0]) or all device banks (A10 HIGH). The address inputs also provide the op-code during a MODE REGISTER SET command. BA[1:0] define which mode register (or extended mode register) is loaded during the LOAD MODE REGISTER command. A[11:0] (128MB) and A[12:0] (256MB, 512MB).
BA[1:0]	Input	Bank address: BA[1:0] define the device bank to which an ACTIVE, READ, WRITE, or PRECHARGE command is being applied.
CK[2:0], CK#[2:0]	Input	Clock: CK and CK# are differential clock inputs. All control, command, and address input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#. Output data (DQ and DQS) is referenced to the crossings of CK and CK#.
CKE0	Input	Clock enable: CKE enables (registered HIGH) and disables (registered LOW) the internal clock, input buffers, and output drivers.
DM[8:0]	Input	Input data mask: DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH, along with that input data, during a write access. DM is sampled on both edges of DQS. Although DM pins are input-only, the DM loading is designed to match that of the DQ and DQS pins.
RAS#, CAS#, WE#	Input	Command inputs: RAS#, CAS#, and WE# (along with S#) define the command being entered.
S0#	Input	Chip selects: S# enables (registered LOW) and disables (registered HIGH) the command decoder.
SA[2:0]	Input	Presence-detect address inputs: These pins are used to configure the presence-detect device.
SCL	Input	Serial clock for presence-detect: SCL is used to synchronize the presence-detect data transfer to and from the module.
CB[7:0]	I/O	Check bits.
DQ[63:0]	I/O	Data input/output: Data bus.
DQS[8:0]	I/O	Data strobe: Output with read data. Edge-aligned with read data. Input with write data. Center-aligned with write data. Used to capture data.
SDA	I/O	Serial presence-detect data: SDA is a bidirectional pin used to transfer addresses and data into and out of the presence-detect portion of the module.
V _{DD}	Supply	Power supply: 2.5V ±0.2V (-40B: 2.6V ±0.1V).
V _{DDSPD}	Supply	Serial EEPROM positive power supply: 2.3–3.6V.
V _{REF}	Supply	SSTL_2 reference voltage (V _{DD} /2).
V _{SS}	Supply	Ground.
NC	–	No connect: These pins are not connected on the module.

Functional Block Diagrams

Figure 3: Functional Block Diagram – Low-Profile Layout

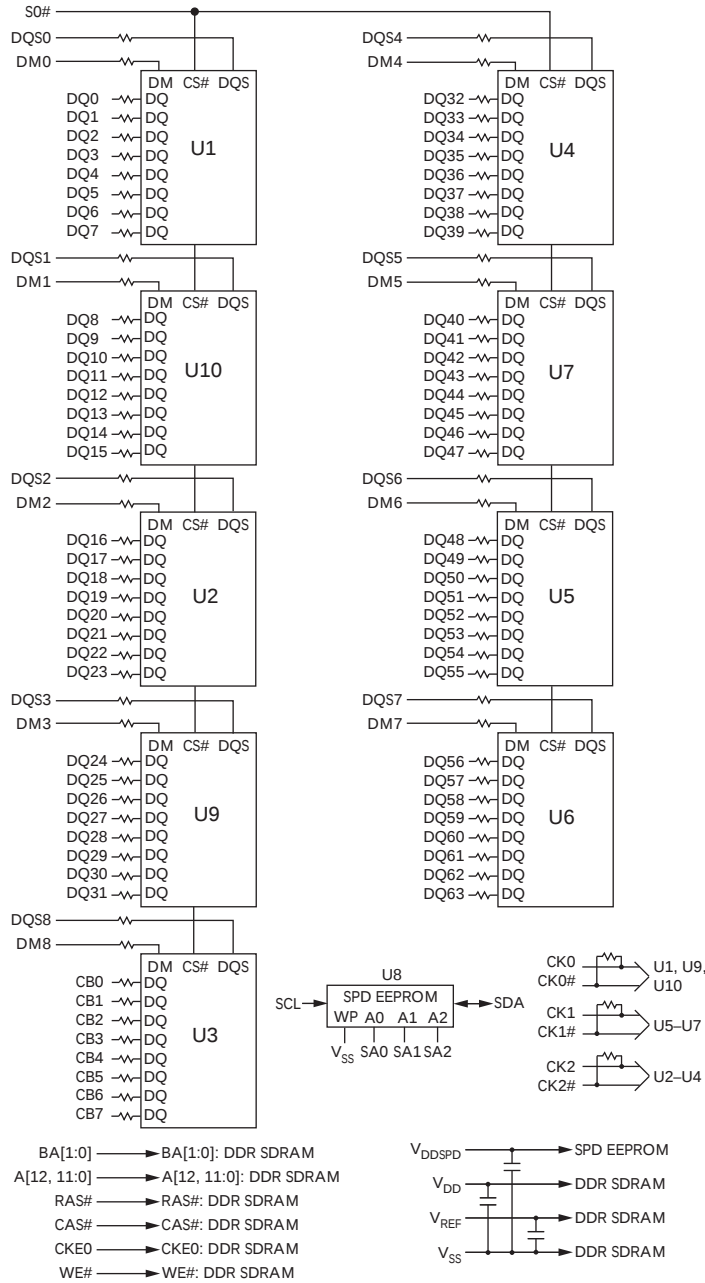
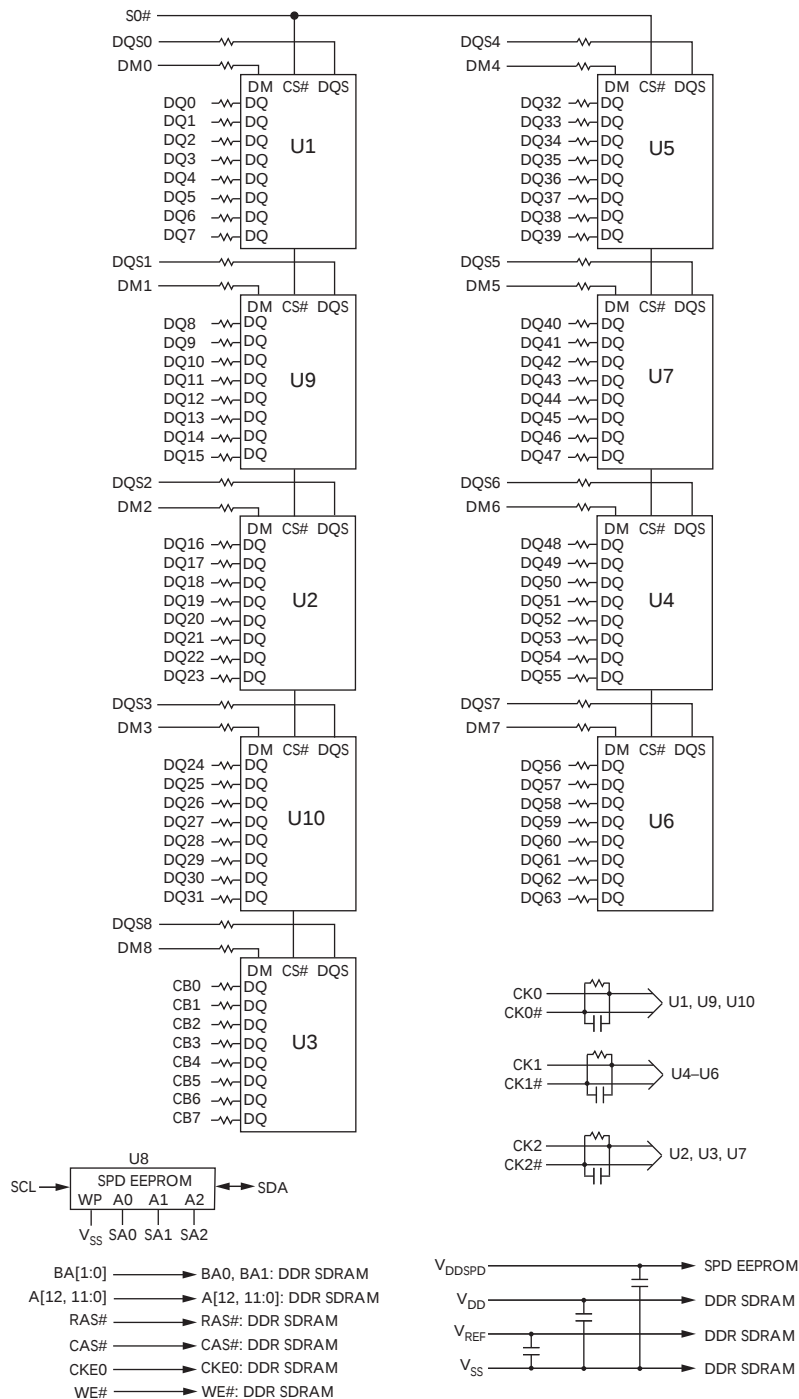


Figure 4: Functional Block Diagram – Standard Layout



General Description

The MT9VDDT1672H, MT9VDDT3272H, and MT9VDDT6472H are high-speed, CMOS dynamic random access, 128MB, 256MB, and 512MB memory modules organized in a x72 configuration. These modules use DDR SDRAM devices with four internal banks.

DDR SDRAM modules use a double data rate architecture to achieve high-speed operation. The double data rate architecture is essentially a $2n$ -prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for DDR SDRAM modules effectively consists of a single $2n$ -bit-wide, one-clock-cycle data transfer at the internal DRAM core and two corresponding n -bit-wide, one-half-clock-cycle data transfers at the I/O pins.

A bidirectional data strobe (DQS) is transmitted externally, along with data, for use in data capture at the receiver. DQS is a strobe transmitted by the DDR SDRAM during READs and by the memory controller during WRITEs. DQS is edge-aligned with data for READs and center-aligned with data for WRITEs.

DDR SDRAM modules operate from differential clock inputs (CK and CK#); the crossing of CK going HIGH and CK# going LOW will be referred to as the positive edge of CK. Control, command, and address signals are registered at every positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CK.

Serial Presence-Detect Operation

DDR SDRAM modules incorporate serial presence-detect. The SPD function is implemented using a 2048-bit EEPROM. This nonvolatile storage device contains 256 bytes. The first 128 bytes are programmed by Micron to identify the module type and various SDRAM organizations and timing parameters. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device (DIMM) occur via a standard I²C bus using the DIMM's SCL (clock) and SDA (data) signals, together with SA[2:0], which provide eight unique DIMM/EEPROM addresses. Write protect (WP) is tied to V_{SS} on the module, permanently disabling hardware write protect.

Electrical Specifications

Stresses greater than those listed in Table 8 may cause permanent damage to the module. This is a stress rating only, and functional operation of the module at these or any other conditions outside those indicated on the device data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may adversely affect reliability.

Table 8: Absolute Maximum Ratings

Symbol	Parameter		Min	Max	Units
V _{DD}	V _{DD} supply voltage relative to V _{SS}		−1.0	3.6	V
V _{IN} , V _{OUT}	Voltage on any pin relative to V _{SS}		−0.5	3.2	V
I _I	Input leakage current; Any input 0V ≤ V _{IN} ≤ V _{DD} ; V _{REF} input 0V ≤ V _{IN} ≤ 1.35V (All other pins not under test = 0V)	Address inputs, RAS#, CAS#, WE#, BA, S#, CKE	−18	18	μA
		CK, CK#	−6	6	
		DM	−2	2	
I _{OZ}	Output leakage current; 0V ≤ V _{OUT} ≤ V _{DDQ} ; DQ are disabled	DQ, DQS	−5	5	μA
T _A	DRAM ambient operating temperature ¹	Commercial	0	+70	°C
		Industrial	−40	+85	°C

Notes: 1. For further information, refer to technical note TN-00-08: "Thermal Applications," available on Micron's Web site.

Input Capacitance

Micron encourages designers to simulate the performance of the module to achieve optimum values. Simulations are significantly more accurate and realistic than a gross estimation of module capacitance when inductance and delay parameters associated with trace lengths are used in simulations. JEDEC modules are currently designed using simulations to close timing budgets.

Component AC Timing and Operating Conditions

Recommended AC operating conditions are given in the DDR component data sheets. Component specifications are available on Micron's Web site. Module speed grades correlate with component speed grades, as shown in Table 9.

Table 9: Module and Component Speed Grades

DDR components meet or exceed the listed module speed grades

Module Speed Grade	Component Speed Grade
-40B	-5
-335	-6
-262	-75E
-26A	-75Z
-265	-75

I_{DD} Specifications

Table 10: I_{DD} Specifications and Conditions – 128MB (Die Revision D)

Values are shown for the MT46V16M8 DDR SDRAM only and are computed from values specified in the 128Mb (16 Meg x 8) component data sheet

Parameter/Condition	Symbol	-335	-262	-26A/ -265	Units
Operating one bank active-precharge current: $t_{RC} = t_{RC} \text{ (MIN)}$; $t_{CK} = t_{CK} \text{ (MIN)}$; DQ, DM, and DQS inputs changing once per clock cycle; Address and control inputs changing once every two clock cycles	I_{DD0}	1125	990	945	mA
Operating one bank active-read-precharge current: BL = 4; $t_{RC} = t_{RC} \text{ (MIN)}$; $t_{CK} = t_{CK} \text{ (MIN)}$; $I_{OUT} = 0\text{mA}$; Address and control inputs changing once per clock cycle	I_{DD1}	1215	1080	1080	mA
Precharge power-down standby current: All device banks idle; Power-down mode; $t_{CK} = t_{CK} \text{ (MIN)}$; CKE = LOW	I_{DD2P}	27	27	27	mA
Idle standby current: CS# = HIGH; All device banks idle; $t_{CK} = t_{CK} \text{ (MIN)}$; CKE = HIGH; Address and other control inputs changing once per clock cycle; $V_{IN} = V_{REF}$ for DQ, DM, and DQS	I_{DD2F}	405	405	360	mA
Active power-down standby current: One device bank active; Power-down mode; $t_{CK} = t_{CK} \text{ (MIN)}$; CKE = LOW	I_{DD3P}	225	225	180	mA
Active standby current: CS# = HIGH; CKE = HIGH; One device bank active; $t_{RC} = t_{RAS} \text{ (MAX)}$; $t_{CK} = t_{CK} \text{ (MIN)}$; DQ, DM, and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle	I_{DD3N}	450	450	405	mA
Operating burst read current: BL = 2; Continuous burst reads; One device bank active; Address and control inputs changing once per clock cycle; $t_{CK} = t_{CK} \text{ (MIN)}$; $I_{OUT} = 0\text{mA}$	I_{DD4R}	1260	1170	1125	mA
Operating burst write current: BL = 2; Continuous burst writes; One device bank active; Address and control inputs changing once per clock cycle; $t_{CK} = t_{CK} \text{ (MIN)}$; DQ, DM, and DQS inputs changing twice per clock cycle	I_{DD4W}	1260	1125	1080	mA
Auto refresh current	$t_{REFC} = t_{RFC} \text{ (MIN)}$	I_{DD5}	2385	1980	mA
	$t_{REFC} = 15.625\mu\text{s}$	I_{DD5A}	45	45	
Self refresh current: CKE $\leq 0.2\text{V}$	I_{DD6}	36	36	36	mA
Operating bank interleave read current: Four device bank interleaving reads (BL = 4) with auto precharge; $t_{RC} = t_{RC} \text{ (MIN)}$; $t_{CK} = t_{CK} \text{ (MIN)}$; Address and control inputs change only during active READ or WRITE commands	I_{DD7}	3195	2970	2925	mA

Table 11: I_{DD} Specifications and Conditions – 256MB (Die Revision F)

Values are shown for the MT46V32M8 DDR SDRAM only and are computed from values specified in the 256Mb (32 Meg x 8) component data sheet

Parameter/Condition	Symbol	-40B	-335	-262	-265	Units
Operating one bank active-precharge current: t _{RC} = t _{RC} (MIN); t _{CK} = t _{CK} (MIN); DQ, DM, and DQS inputs changing once per clock cycle; Address and control inputs changing once every two clock cycles	I _{DD0}	1215	1125	1125	1080	mA
Operating one bank active-read-precharge current: BL = 4; t _{RC} = t _{RC} (MIN); t _{CK} = t _{CK} (MIN); I _{OUT} = 0mA; Address and control inputs changing once per clock cycle	I _{DD1}	1530	1530	1440	1305	mA
Precharge power-down standby current: All device banks idle; Power-down mode; t _{CK} = t _{CK} (MIN); CKE = LOW	I _{DD2P}	36	36	36	36	mA
Idle standby current: CS# = HIGH; All device banks idle; t _{CK} = t _{CK} (MIN); CKE = HIGH; Address and other control inputs changing once per clock cycle; V _{IN} = V _{REF} for DQ, DM, and DQS	I _{DD2F}	540	450	405	405	mA
Active power-down standby current: One device bank active; Power-down mode; t _{CK} = t _{CK} (MIN); CKE = LOW	I _{DD3P}	360	270	225	270	mA
Active standby current: CS# = HIGH; CKE = HIGH; One device bank active; t _{RC} = t _{RAS} (MAX); t _{CK} = t _{CK} (MIN); DQ, DM, and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle	I _{DD3N}	630	540	450	450	mA
Operating burst read current: BL = 2; Continuous burst reads; One device bank active; Address and control inputs changing once per clock cycle; t _{CK} = t _{CK} (MIN); I _{OUT} = 0mA	I _{DD4R}	1800	1575	1350	1350	mA
Operating burst write current: BL = 2; Continuous burst writes; One device bank active; Address and control inputs changing once per clock cycle; t _{CK} = t _{CK} (MIN); DQ, DM, and DQS inputs changing twice per clock cycle	I _{DD4W}	1755	1575	1350	1350	mA
Auto refresh current	t _{REFC} = t _{RFC} (MIN)	I _{DD5}	2340	2295	2115	mA
	t _{REFC} = 7.8125μs	I _{DD5A}	54	54	54	
Self refresh current: CKE ≤ 0.2V	I _{DD6}	36	36	36	36	mA
Operating bank interleave read current: Four device bank interleaving reads (BL = 4) with auto precharge; t _{RC} = t _{RC} (MIN); t _{CK} = t _{CK} (MIN); Address and control inputs change only during active READ or WRITE commands	I _{DD7}	4230	3690	3150	3285	mA

Table 12: I_{DD} Specifications and Conditions – 256MB (Die Revision K)

Values are shown for the MT46V32M8 DDR SDRAM only and are computed from values specified in the 256Mb (32 Meg x 8) component data sheet

Parameter/Condition	Symbol	-40B	-335	Units
Operating one bank active-precharge current: $t_{RC} = t_{RC}(\text{MIN})$; $t_{CK} = t_{CK}(\text{MIN})$; DQ, DM, and DQS inputs changing once per clock cycle; Address and control inputs changing once every two clock cycles	I_{DD0}	900	810	mA
Operating one bank active-read-precharge current: BL = 4; $t_{RC} = t_{RC}(\text{MIN})$; $t_{CK} = t_{CK}(\text{MIN})$; $I_{OUT} = 0\text{mA}$; Address and control inputs changing once per clock cycle	I_{DD1}	1080	1035	mA
Precharge power-down standby current: All device banks idle; Power-down mode; $t_{CK} = t_{CK}(\text{MIN})$; CKE = LOW	I_{DD2P}	36	36	mA
Idle standby current: CS# = HIGH; All device banks idle; $t_{CK} = t_{CK}(\text{MIN})$; CKE = HIGH; Address and other control inputs changing once per clock cycle; $V_{IN} = V_{REF}$ for DQ, DM, and DQS	I_{DD2F}	450	450	mA
Active power-down standby current: One device bank active; Power-down mode; $t_{CK} = t_{CK}(\text{MIN})$; CKE = LOW	I_{DD3P}	315	270	mA
Active standby current: CS# = HIGH; CKE = HIGH; One device bank active; $t_{RC} = t_{RAS}(\text{MAX})$; $t_{CK} = t_{CK}(\text{MIN})$; DQ, DM, and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle	I_{DD3N}	540	495	mA
Operating burst read current: BL = 2; Continuous burst reads; One device bank active; Address and control inputs changing once per clock cycle; $t_{CK} = t_{CK}(\text{MIN})$; $I_{OUT} = 0\text{mA}$	I_{DD4R}	1620	1440	mA
Operating burst write current: BL = 2; Continuous burst writes; One device bank active; Address and control inputs changing once per clock cycle; $t_{CK} = t_{CK}(\text{MIN})$; DQ, DM, and DQS inputs changing twice per clock cycle	I_{DD4W}	1620	1440	mA
Auto refresh current	$t_{REFC} = t_{RFC}(\text{MIN})$	I_{DD5}	1440	mA
	$t_{REFC} = 15.625\mu\text{s}$	I_{DD5A}	54	
Self refresh current: CKE $\leq 0.2\text{V}$	I_{DD6}	36	36	mA
Operating bank interleave read current: Four device bank interleaving reads (BL = 4) with auto precharge; $t_{RC} = t_{RC}(\text{MIN})$; $t_{CK} = t_{CK}(\text{MIN})$; Address and control inputs change only during active READ or WRITE commands	I_{DD7}	2610	2430	mA

Table 13: I_{DD} Specifications and Conditions – 256MB (Die Revision M)

Values are shown for the MT46V32M8 DDR SDRAM only and are computed from values specified in the 256Mb (32 Meg x 8) component data sheet

Parameter/Condition		Symbol	-40B	-335	Units
Operating one bank active-precharge current: $t_{RC} = t_{RC}(\text{MIN})$; $t_{CK} = t_{CK}(\text{MIN})$; DQ, DM, and DQS inputs changing once per clock cycle; Address and control inputs changing once every two clock cycles		I_{DD0}	630	540	mA
Operating one bank active-read-precharge current: BL = 4; $t_{RC} = t_{RC}(\text{MIN})$; $t_{CK} = t_{CK}(\text{MIN})$; $I_{OUT} = 0\text{mA}$; Address and control inputs changing once per clock cycle		I_{DD1}	765	675	mA
Precharge power-down standby current: All device banks idle; Power-down mode; $t_{CK} = t_{CK}(\text{MIN})$; CKE = LOW		I_{DD2P}	36	36	mA
Idle standby current: CS# = HIGH; All device banks idle; $t_{CK} = t_{CK}(\text{MIN})$; CKE = HIGH; Address and other control inputs changing once per clock cycle; $V_{IN} = V_{REF}$ for DQ, DM, and DQS		I_{DD2F}	207	207	mA
Active power-down standby current: One device bank active; Power-down mode; $t_{CK} = t_{CK}(\text{MIN})$; CKE = LOW		I_{DD3P}	126	126	mA
Active standby current: CS# = HIGH; CKE = HIGH; One device bank active; $t_{RC} = t_{RAS}(\text{MAX})$; $t_{CK} = t_{CK}(\text{MIN})$; DQ, DM, and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle		I_{DD3N}	270	270	mA
Operating burst read current: BL = 2; Continuous burst reads; One device bank active; Address and control inputs changing once per clock cycle; $t_{CK} = t_{CK}(\text{MIN})$; $I_{OUT} = 0\text{mA}$		I_{DD4R}	855	765	mA
Operating burst write current: BL = 2; Continuous burst writes; One device bank active; Address and control inputs changing once per clock cycle; $t_{CK} = t_{CK}(\text{MIN})$; DQ, DM, and DQS inputs changing twice per clock cycle		I_{DD4W}	945	855	mA
Auto refresh current	$t_{REFC} = t_{RFC}(\text{MIN})$	I_{DD5}	1035	945	mA
	$t_{REFC} = 15.625\mu\text{s}$	I_{DD5A}	54	54	
Self refresh current: CKE $\leq 0.2\text{V}$		I_{DD6}	36	36	mA
Operating bank interleave read current: Four device bank interleaving reads (BL = 4) with auto precharge; $t_{RC} = t_{RC}(\text{MIN})$; $t_{CK} = t_{CK}(\text{MIN})$; Address and control inputs change only during active READ or WRITE commands		I_{DD7}	1575	1575	mA

Table 14: I_{DD} Specifications and Conditions – 512MB (Die Revision F)

Values are shown for MT46V64M8 DDR SDRAM only and are computed from values specified in the 512Mb (64 Meg x 8) component data sheet

Parameter/Condition	Symbol	-40B	-335	-26A/ -265	Units
Operating one bank active-precharge current: t _{RC} = t _{RC} (MIN); t _{CK} = t _{CK} (MIN); DQ, DM, and DQS inputs changing once per clock cycle; Address and control inputs changing once every two clock cycles	I _{DD0}	1395	1170	1035	mA
Operating one bank active-read-precharge current: BL = 4; t _{RC} = t _{RC} (MIN); t _{CK} = t _{CK} (MIN); I _{OUT} = 0mA; Address and control inputs changing once per clock cycle	I _{DD1}	1665	1440	1305	mA
Precharge power-down standby current: All device banks idle; Power-down mode; t _{CK} = t _{CK} (MIN); CKE = LOW	I _{DD2P}	45	45	45	mA
Idle standby current: CS# = HIGH; All device banks idle; t _{CK} = t _{CK} (MIN); CKE = HIGH; Address and other control inputs changing once per clock cycle; V _{IN} = V _{REF} for DQ, DM, and DQS	I _{DD2F}	495	405	360	mA
Active power-down standby current: One device bank active; Power-down mode; t _{CK} = t _{CK} (MIN); CKE = LOW	I _{DD3P}	405	315	270	mA
Active standby current: CS# = HIGH; CKE = HIGH; One device bank active; t _{RC} = t _{RAS} (MAX); t _{CK} = t _{CK} (MIN); DQ, DM, and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle	I _{DD3N}	540	450	405	mA
Operating burst read current: BL = 2; Continuous burst reads; One device bank active; Address and control inputs changing once per clock cycle; t _{CK} = t _{CK} (MIN); I _{OUT} = 0mA	I _{DD4R}	1710	1485	1305	mA
Operating burst write current: BL = 2; Continuous burst writes; One device bank active; Address and control inputs changing once per clock cycle; t _{CK} = t _{CK} (MIN); DQ, DM, and DQS inputs changing twice per clock cycle	I _{DD4W}	1775	1575	1215	mA
Auto refresh current	t _{REFC} = t _{RFC} (MIN)	I _{DD5}	3105	2610	mA
	t _{REFC} = 7.8125μs	I _{DD5A}	99	90	
Self refresh current: CKE ≤ 0.2V	I _{DD6}	45	45	45	mA
Operating bank interleave read current: Four device bank interleaving reads (BL = 4) with auto precharge; t _{RC} = t _{RC} (MIN); t _{CK} = t _{CK} (MIN); Address and control inputs change only during active READ or WRITE commands	I _{DD7}	4050	3645	3150	mA

Table 15: I_{DD} Specifications and Conditions – 512MB (Die Revision J)

Values are shown for the MT46V64M8 DDR SDRAM only and are computed from values specified in the 512Mb (64 Meg x 8) component data sheet

Parameter/Condition		Symbol	-40B	-335	Units
Operating one bank active-precharge current: $t_{RC} = t_{RC}(\text{MIN})$; $t_{CK} = t_{CK}(\text{MIN})$; DQ, DM, and DQS inputs changing once per clock cycle; Address and control inputs changing once every two clock cycles		I_{DD0}	675	585	mA
Operating one bank active-read-precharge current: BL = 4; $t_{RC} = t_{RC}(\text{MIN})$; $t_{CK} = t_{CK}(\text{MIN})$; $I_{OUT} = 0\text{mA}$; Address and control inputs changing once per clock cycle		I_{DD1}	765	675	mA
Precharge power-down standby current: All device banks idle; Power-down mode; $t_{CK} = t_{CK}(\text{MIN})$; CKE = LOW		I_{DD2P}	45	45	mA
Idle standby current: CS# = HIGH; All device banks idle; $t_{CK} = t_{CK}(\text{MIN})$; CKE = HIGH; Address and other control inputs changing once per clock cycle; $V_{IN} = V_{REF}$ for DQ, DM, and DQS		I_{DD2F}	207	207	mA
Active power-down standby current: One device bank active; Power-down mode; $t_{CK} = t_{CK}(\text{MIN})$; CKE = LOW		I_{DD3P}	162	126	mA
Active standby current: CS# = HIGH; CKE = HIGH; One device bank active; $t_{RC} = t_{RAS}(\text{MAX})$; $t_{CK} = t_{CK}(\text{MIN})$; DQ, DM, and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle		I_{DD3N}	360	342	mA
Operating burst read current: BL = 2; Continuous burst reads; One device bank active; Address and control inputs changing once per clock cycle; $t_{CK} = t_{CK}(\text{MIN})$; $I_{OUT} = 0\text{mA}$		I_{DD4R}	1080	765	mA
Operating burst write current: BL = 2; Continuous burst writes; One device bank active; Address and control inputs changing once per clock cycle; $t_{CK} = t_{CK}(\text{MIN})$; DQ, DM, and DQS inputs changing twice per clock cycle		I_{DD4W}	1080	855	mA
Auto refresh current	$t_{REFC} = t_{RFC}(\text{MIN})$	I_{DD5}	1080	945	mA
	$t_{REFC} = 15.625\mu\text{s}$	I_{DD5A}	72	72	
Self refresh current: CKE $\leq 0.2\text{V}$		I_{DD6}	45	45	mA
Operating bank interleave read current: Four device bank interleaving reads (BL = 4) with auto precharge; $t_{RC} = t_{RC}(\text{MIN})$; $t_{CK} = t_{CK}(\text{MIN})$; Address and control inputs change only during active READ or WRITE commands		I_{DD7}	2070	1890	mA

Serial Presence-Detect

Table 16: Serial Presence-Detect EEPROM DC Operating Conditions

Parameter/Condition	Symbol	Min	Max	Units
Supply voltage	V_{DDSPD}	2.3	3.6	V
Input high voltage: Logic 1; All inputs	V_{IH}	$V_{DDSPD} \times 0.7$	$V_{DDSPD} + 0.5$	V
Input low voltage: Logic 0; All inputs	V_{IL}	-1.0	$V_{DDSPD} \times 0.3$	V
Output low voltage: $I_{OUT} = 3\text{mA}$	V_{OL}	–	0.4	V
Input leakage current: $V_{IN} = \text{GND to } V_{DD}$	I_{LI}	–	10	μA
Output leakage current: $V_{OUT} = \text{GND to } V_{DD}$	I_{LO}	–	10	μA
Standby current: $SCL = SDA = V_{DD} - 0.3\text{V}$; All other inputs = V_{SS} or V_{DD}	I_{SB}	–	30	μA
Power supply current: SCL clock frequency = 100 kHz	I_{CC}	–	2.0	mA

Table 17: Serial Presence-Detect EEPROM AC Operating Conditions

Parameter/Condition	Symbol	Min	Max	Units	Notes
SCL LOW to SDA data-out valid	t_{AA}	0.2	0.9	μs	1
Time the bus must be free before a new transition can start	t_{BUF}	1.3	–	μs	
Data-out hold time	t_{DH}	200	–	ns	
Clock/data fall time	t_F	–	300	ns	2
Clock/data rise time	t_R	–	300	ns	2
Data-in hold time	$t_{HD:DAT}$	0	–	μs	
Start condition hold time	$t_{H:STA}$	0.6	–	μs	
Clock HIGH period	t_{HIGH}	0.6	–	μs	
Noise suppression time constant at SCL , SDA inputs	t_I	–	50	ns	
Clock LOW period	t_{LOW}	1.3	–	μs	
SCL clock frequency	f_{SCL}	–	400	kHz	
Data-in setup time	$t_{SU:DAT}$	100	–	ns	
Start condition setup time	$t_{SU:STA}$	0.6	–	μs	3
Stop condition setup time	$t_{SU:STO}$	0.6	–	μs	
WRITE cycle time	t_{WRC}	–	10	ms	4

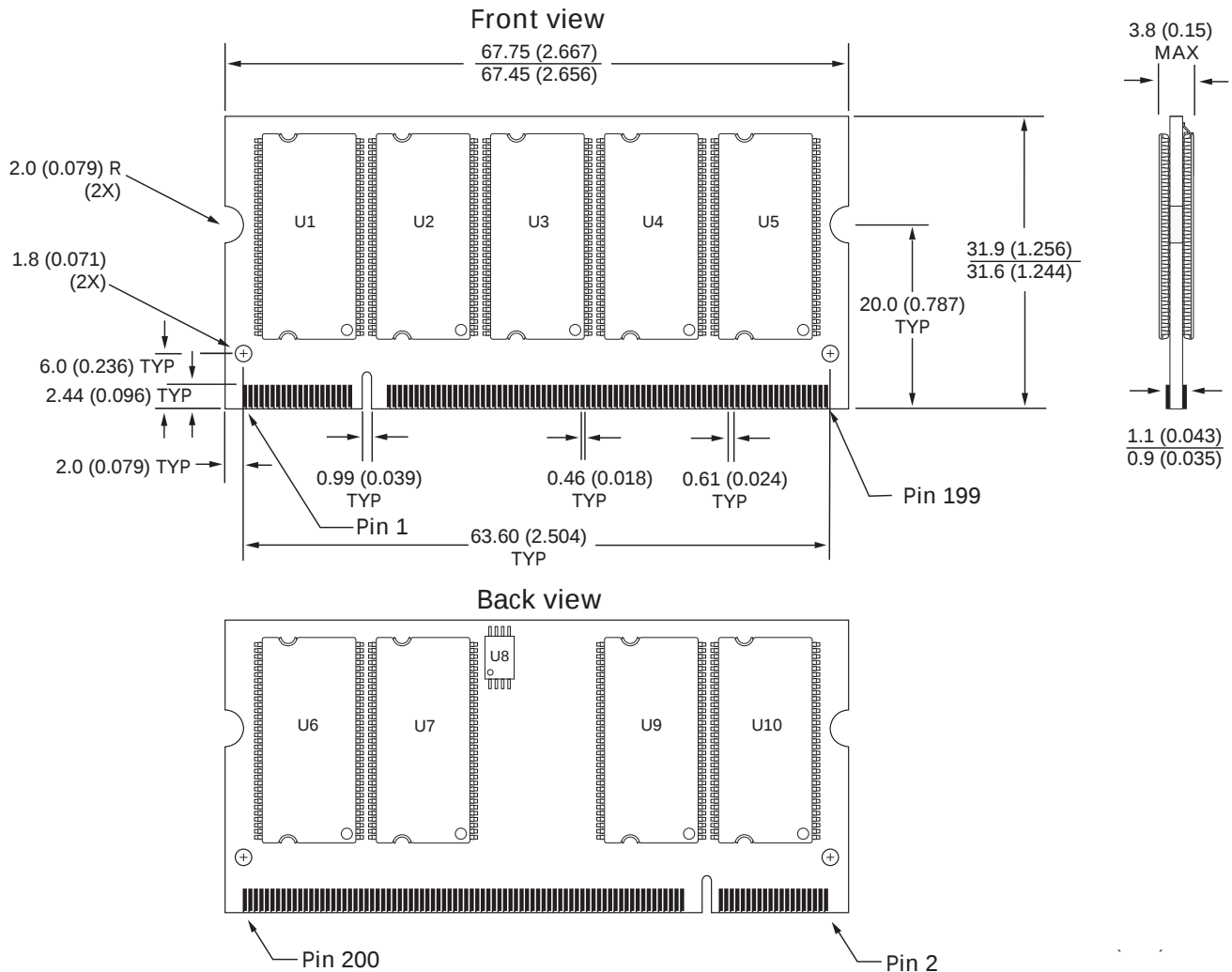
- Notes:
1. To avoid spurious start and stop conditions, a minimum delay is placed between $SCL = 1$ and the falling or rising edge of SDA .
 2. This parameter is sampled.
 3. For a restart condition or following a WRITE cycle.
 4. The SPD EEPROM WRITE cycle time (t_{WRC}) is the time from a valid stop condition of a write sequence to the end of the EEPROM internal ERASE/PROGRAM cycle. During the WRITE cycle, the EEPROM bus interface circuit is disabled, SDA remains HIGH due to pull-up resistance, and the EEPROM does not respond to its slave address.

Serial Presence-Detect Data

For the latest serial presence-detect data, refer to Micron's SPD page:
www.micron.com/SPD.

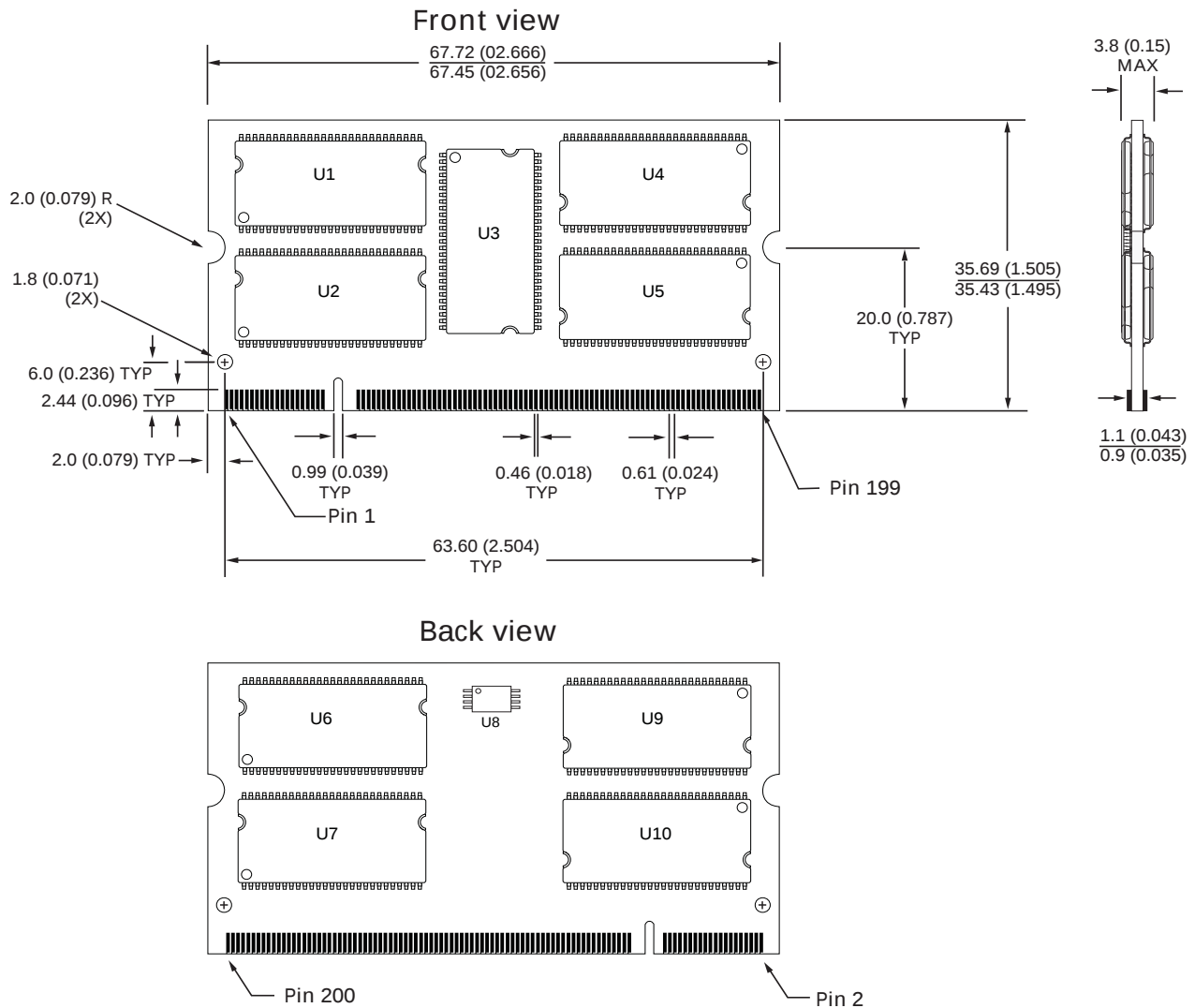
Module Dimensions

Figure 5: 200-Pin SODIMM – Low-Profile Layout



- Notes:
1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.
 2. The dimensional diagram is for reference only. Refer to the JEDEC MO document for additional design dimensions.

Figure 6: 200-Pin SODIMM – Standard Layout



- Notes:
1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.
 2. The dimensional diagram is for reference only. Refer to the JEDEC MO document for additional design dimensions.

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