19-3819; Rev. 0, 6/91

MAXIM

Precision Video Buffer Amplifier

General Description

The MAX405 high-speed, precision buffer amplifier guarantees a minimum gain of 0.99V/V over -40°C to +85°C, with loads as low as 50Ω. It operates from ±5V power supplies and drives ±3V signals into 50Ω loads, or ±2.25V into four 150Ω loads. The MAX405 features 180MHz bandwidth, 650V/µs slew rate, and 35ns settling time to 0.1%. Precision characteristics include 0.01° differential phase, 0.03% differential gain, and guaranteed 0.1% nonlinearity over temperature. Unlike other buffer amplifiers, the MAX405's inverting input can be used to increase the gain.

The MAX405 is ideal as a 50Ω and 75Ω coaxial cable driver for color video signals. Guaranteed 60mA continuous output current eliminates the need for multiple buffers, external power-booster circuits, or expensive hybrid modules common in video distribution applications. Greater PC-layout densities are provided by compact 8-pin DIP and SO packages.

Applications

Video Distribution
Flash A/D Input Buffers
Coaxial Line Drivers
Fast Sample-and-Hold Buffers

Features

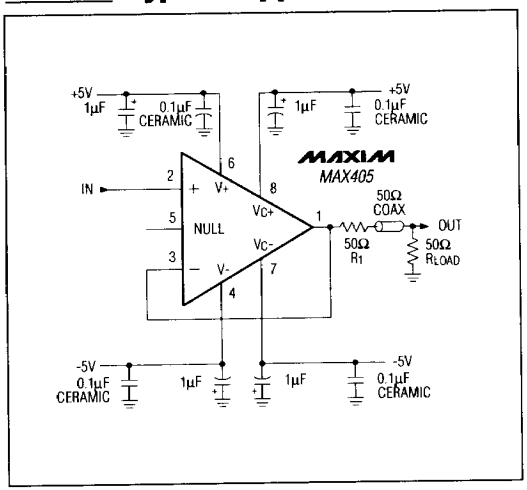
- ◆ **0.99V/V Min DC Gain (R_L = 50Ω) Over Temp**
- ◆ **0.01° Differential Phase**
- ◆ **0.03% Differential Gain**
- ◆ **0.1% Nonlinearity Over Temperature**
- ◆ **180MHz Bandwidth**
- ◆ **650V/µs Slew Rate**
- ◆ **60mA Continuous Output Current**
- ◆ **0.01Ω R_{OUT}**
- ◆ **0.6pF Input Capacitance**
- ◆ **Drives Four 150Ω Loads**
- ◆ **Adjustable Gain Control**

Ordering Information

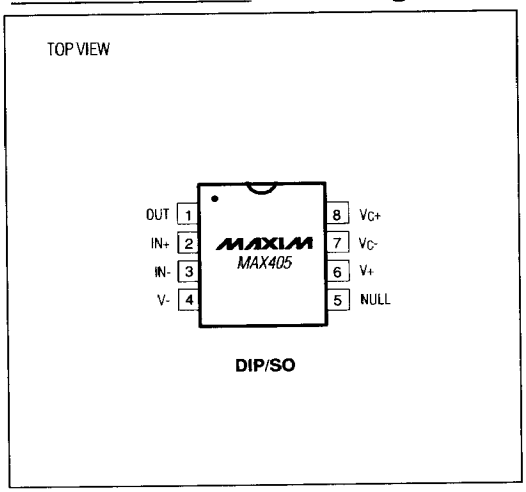
PART	TEMP. RANGE	PIN-PACKAGE
MAX405CPA	0°C to +70°C	8 Plastic DIP
MAX405CSA	0°C to +70°C	8 SO
MAX405C/D	0°C to +70°C	Dice*
MAX405EPA	-40°C to +85°C	8 Plastic DIP
MAX405ESA	-40°C to +85°C	8 SO

*Contact factory for dice specifications.

Typical Application Circuit



Pin Configuration



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Precision Video Buffer Amplifier

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V+ to V-) 12V
Voltage at Any Pin ..... (V- -0.3V) to (V+ +0.3V)
Output Current (I_{OUT}) 250mA
Short-Circuit Duration (I_{OUT}) ..... 10 sec
Continuous Power Dissipation
Plastic DIP (derate 8.3mW/°C above +70°C) 660mW
SO (derate 6mW/°C above +70°C) 470mW

Operating Temperature Ranges:
MAX405C_ A ..... 0°C to +70°C
MAX405E_ A ..... -40°C to +85°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10 sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

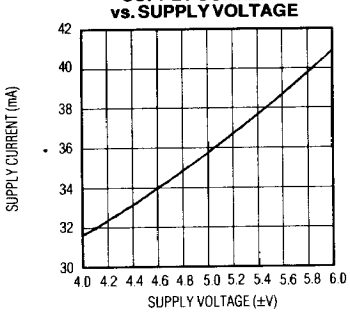
(V+ = V_{C+} = 5V, V- = V_{C-} = -5V, R_L = 50Ω, C_L = 15pF, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	T_A = +25°C			T_A = T_{MIN} to T_{MAX}			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Voltage Gain	A_V	Unadjusted	0.9910	0.9940	1	0.9900		1	V/V
		Adjusted			1.1			1.1	
Offset Voltage	V_{OS}		-5.0	±2.0	5.0				mV
		T_A = 0°C to +70°C				-6.5		6.5	
		T_A = -40°C to +85°C				-8.0		8.0	
Offset Voltage TC	TCV_{OS}						25		µV/°C
Input Bias Current	I_B(IN+)	V_{IN} = 0V	-2		2	-4		4	mA
	(IN-)			10					
Input Resistance	R_{IN}			2.5					MΩ
Input Capacitance	C_{IN}			0.6					pF
Output Voltage Swing	V_{OUT}		-3.0	±3.4	3.0	-3.0		3.0	V
Output Current	I_{OUT}	Continuous	60			60			mA
		Short-circuit (Note 1)	90	180		90	180		
Output Impedance	R_{OUT}	At DC		0.01					Ω
Power-Supply Rejection Ratio	PSRR	ΔV_S = ±5%	48	54		47			dB
Nonlinearity (Note 2)		±2V signal	-1.5	±1.0	1.5				mV
		T_A = 0°C to +70°C				-2.0		2.0	
		T_A = -40°C to +85°C				-2.5		2.5	
Supply Voltage (Note 3)	V+, V-		±4.75	±5	±5.25	±4.75	±5	±5.25	V
Supply Current (Note 3)	IQ	V+, V- = ±5V		±35	±40			±43	mA
AC SPECIFICATIONS (NOTE 1)									
-3dB Bandwidth	BW	V_{IN} = IV_{RMS}	125	180		110			MHz
Full-Power Bandwidth	FPBW	V_{OUT} = $6V_{p-p}$	24	34		18			MHz
Slew Rate	SR	V_{OUT} = 3V step	450	650		350			V/µs
Settling Time	t_S	t = 0.1%, V_{OUT} = 3V step		35	50			70	ns
Rise/Fall Time	$t_{R/F}$	V_{OUT} = 3V step		8	12			16	ns
Differential Phase				0.01					°
Differential Gain				0.03					%

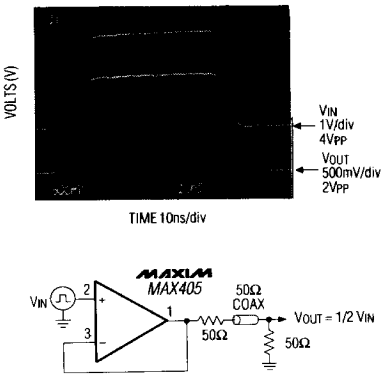
Note 1: Guaranteed by design.
Note 2: Nonlinearity is deviation from end-point line.
Note 3: V_{C+} = V, V_{C-} = V-. Current is for both supply pins.

Typical Operating Characteristics

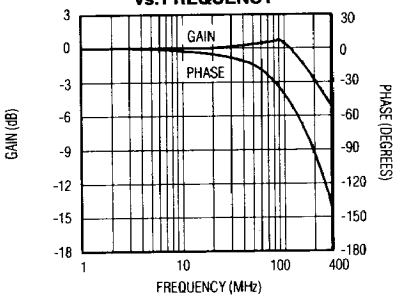
SUPPLY CURRENT vs. SUPPLY VOLTAGE



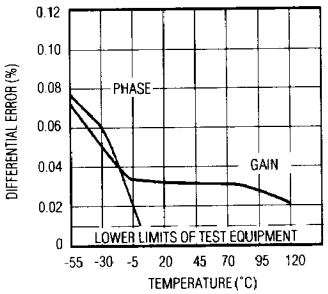
PULSE RESPONSE INTO 50Ω BACK-TERMINATED LOAD



GAIN AND PHASE vs. FREQUENCY



DIFFERENTIAL GAIN AND PHASE ERROR vs. TEMPERATURE



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Pin Description

PIN	NAME	FUNCTION
1	OUT	Buffer-Amplifier Output
2	IN+	Buffer-Amplifier Noninverting Input
3	IN-	Buffer-Amplifier Inverting Input. For unadjusted operation, connect to OUT. Connect to resistive divider from OUT (Figure 3) to adjust gain to exactly 1.0000V/V. IN- CANNOT be used as a conventional op-amp inverting input (see *Gain Trim* section).
4	V-	Negative Supply. Connect to -5V.
5	NULL	Voltage Offset Adjust. Leave open normally. Connect to arm of 1kΩ potentiometer (Figure 2) to null input offset voltage. One end of the potentiometer should be connected to V+. The other end should be connected to a 9kΩ resistor to V-.
6	V+	Positive Supply. Connect to +5V.
7	VC-	Output Stage (Collector) Negative Supply. Connect to -5V.
8	VC+	Output Stage (Collector) Positive Supply. Connect to +5V.

Detailed Description

Circuit Overview

The main circuit elements of the MAX405 are an input stage and a bipolar output stage with separate power-supply connections (Figure 1). This allows separate bypassing to improve high-frequency response while keeping high-frequency transients in the output stage from feeding back to the input. The MAX405 employs an unusual buffer configuration. The inverting input pin allows the gain to be increased above its initial value. In addition, input offset voltage may be trimmed externally.

Zero-Offset Trim

Offset voltage is the difference between IN+ and OUT when IN+ is 0V. The MAX405 is laser trimmed for offset voltage less than ±5mV. Offset voltage can be further reduced by connecting a 1kΩ trim potentiometer and a 9.1kΩ fixed resistor as shown in Figure 2. This circuit's offset nulling range is approximately ±25mV.

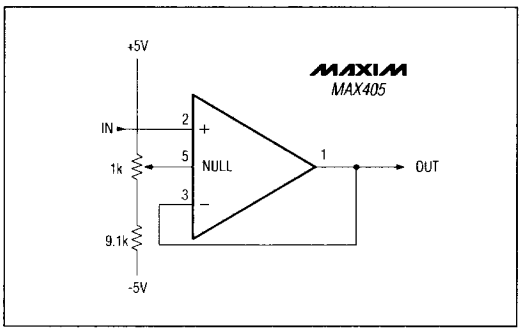

Figure 2. Zero-Offset Trim Circuit

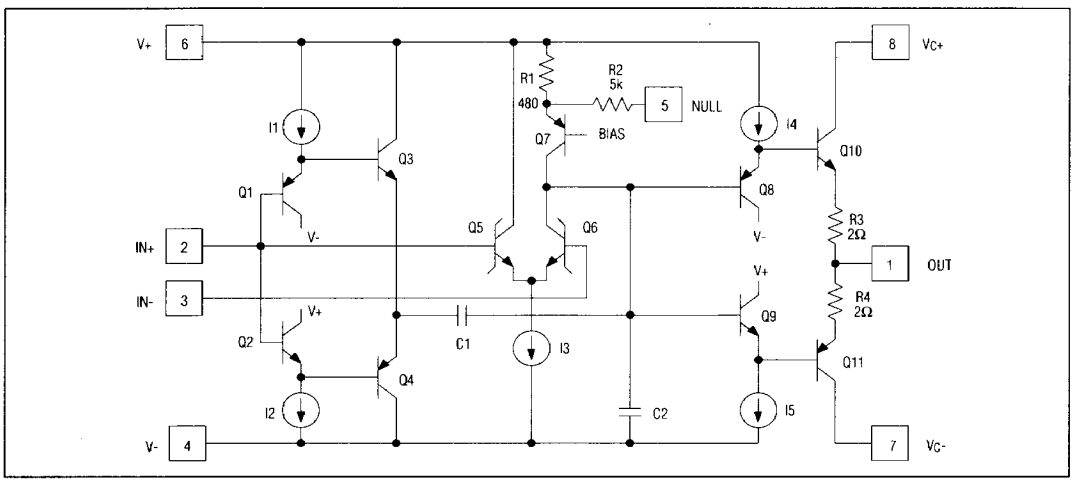

Figure 1. MAX405 Simplified Schematic

Gain Trim

The MAX405 drives 50Ω loads at a 0.9940V/V factory-set gain with no external components.

Unlike other buffer amplifiers, the MAX405 has an inverting input (IN-) that can be connected to an external voltage divider to increase the gain. Figure 3 shows a circuit in which a variable voltage divider trims the buffer to exactly 1.0000V/V. The gain can be adjusted to a maximum of 1.10V/V. Higher gain may produce nonlinearities and instability. Care must be exercised to minimize stray circuit capacitance in the feedback network.

When both offset and gain trims are used, the zero-offset trim should be set first, with 0mV applied to IN+. Next, gain should be adjusted with the full-scale voltage applied to IN+.

Input Capacitance

The MAX405 input capacitance is typically 0.6pF. IN+ is located between the IN- and OUT pins, which are at the same potential. This forms a high-frequency guard for the IN+ pin and minimizes input capacitance. When no gain trim is used, the printed circuit-board layout should include a guard ring (circular trace) around IN+, which is driven from OUT. It should form a complete circle on both sides of the board. The guard ring must be broken on the side of the board that has the input trace, or stretched to enclose the input component solder pad (Figure 4).

Source Impedance

To realize the benefits from the precision MAX405, source impedance must be kept low. Both DC and AC sources contribute errors.

The DC voltage errors are developed from two sources:
1) the input bias current through the source resistance,
2) the voltage divider formed by the source resistance and the finite input resistance (typically 2.5MΩ).

The AC error increases with frequency. It is caused by the action of a lowpass RC filter, consisting of the source (series) resistance and amplifier input (shunt) capacitance (0.6pF).

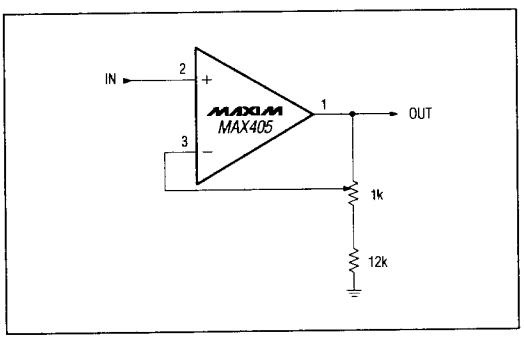

Figure 3. Gain-Trim Circuit

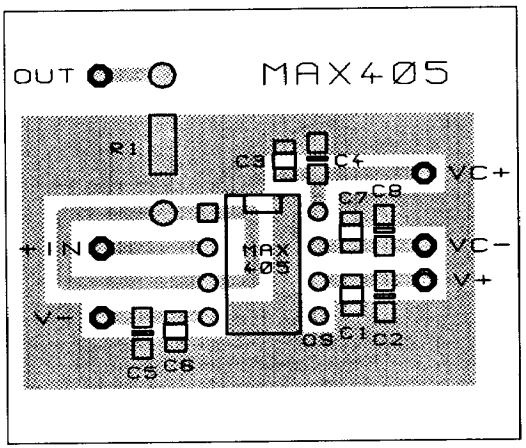

Figure 4. Typical Board Layout (see Typical Application Circuit)

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Output Stage

The MAX405 is stable while driving capacitive loads up to 100pF. Figure 5 shows how larger capacitive loads can be driven if they are isolated with a series resistor.

The OUT pin is protected against accidental short circuits. Internal current limiting keeps continuous output current at safe values at room temperature. Typical values of output short-circuit current are 180mA for positive polarity and 150mA for negative polarity when using ±5V supplies. Continuous short-circuit protection at elevated temperatures T_A > 50°C requires additional external circuitry connected to V_{C+} and V_{C-}. Figure 6 shows a typical circuit.

Coaxial Driver

The MAX405 is ideal as a 50Ω and 75Ω coaxial cable driver. With a guaranteed 60mA continuous output current, the MAX405 directly drives ±3V into 50Ω. Common applications include a back-termination resistor to match the cable impedance. The MAX405 is capable of driving up to four 150Ω (four 75Ω back-terminated loads) loads to ±2.25V.

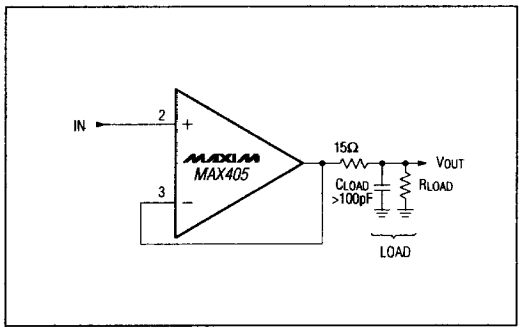

Figure 5. Driving Large Capacitive Loads

Bypassing

Good high-frequency performance demands careful layout, ground planes, and good bypassing. The input and output stages have separate power-supply pins for isolation. Even though the two positive (V+, V_{C+}) and two negative (V-, V_{C-}) supply pins may be connected together, they should have separate bypass capacitors located as close to the pins as possible. Each supply pin should have a 0.1µF ceramic and a 1µF tantalum capacitor connected to ground. Surface-mount chip capacitors (Figure 4) are recommended because they have extremely low impedance at high frequencies.

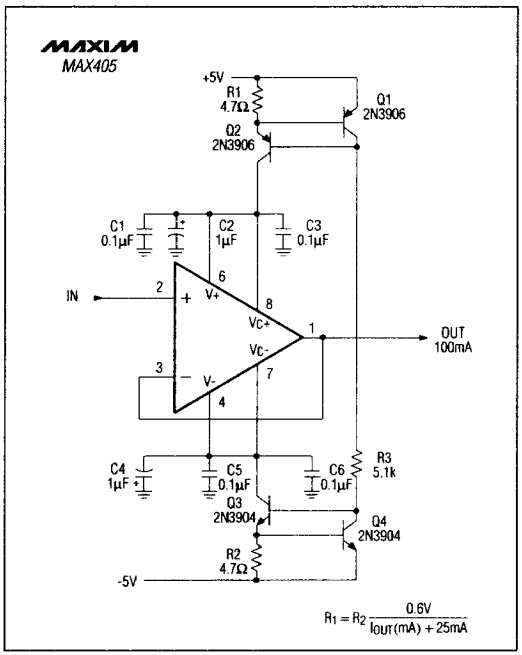

Figure 6. Continuous Output Short-Circuit Protection at Elevated Temperatures (T_A > 50°C)

Chip Topography