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3-Phase Sine Wave Generation Using the AD7226 Quad DAC

by Mike Byrne

This application note discusses the use of the AD7226 in waveform generation. It discusses how to generate 3-phase sine waves which can be used in driving small 3-phase motors. The AD7226 is a quad, 8-bit, CMOS D/A converter packaged in a 20-pin DIP (consult the datasheet for information on the part).

The circuit of Figure 1 shows one method of generating 3-phase sine waves using the AD7226. The circuit consists of a 2716 EPROM, in which sine wave values are stored in digital form; a counter, which counts through the 2716 addresses, and control logic which controls the counter and the loading of the AD7226. The proper codes for synthesizing three sine waves are stored in sets of three. Each set of three code values results in output sine wave values which have a 120° separation between them. For example, if Address X contains a code corresponding to 0° then Address X+1 contains a code corresponding to 120° and X+2 a code corresponding to 240°. The next address, X+3, is the start of another set of three codes and it contains a value corresponding to (0° + 1.4°) (i.e., 360°/256, assuming a 256-element sine wave table is used). Address X+4 contains a value corresponding to (120° + 1.4°) and so on. Therefore, for a 256-element sine wave, 768 (3 × 256) addresses in the EPROM are used.

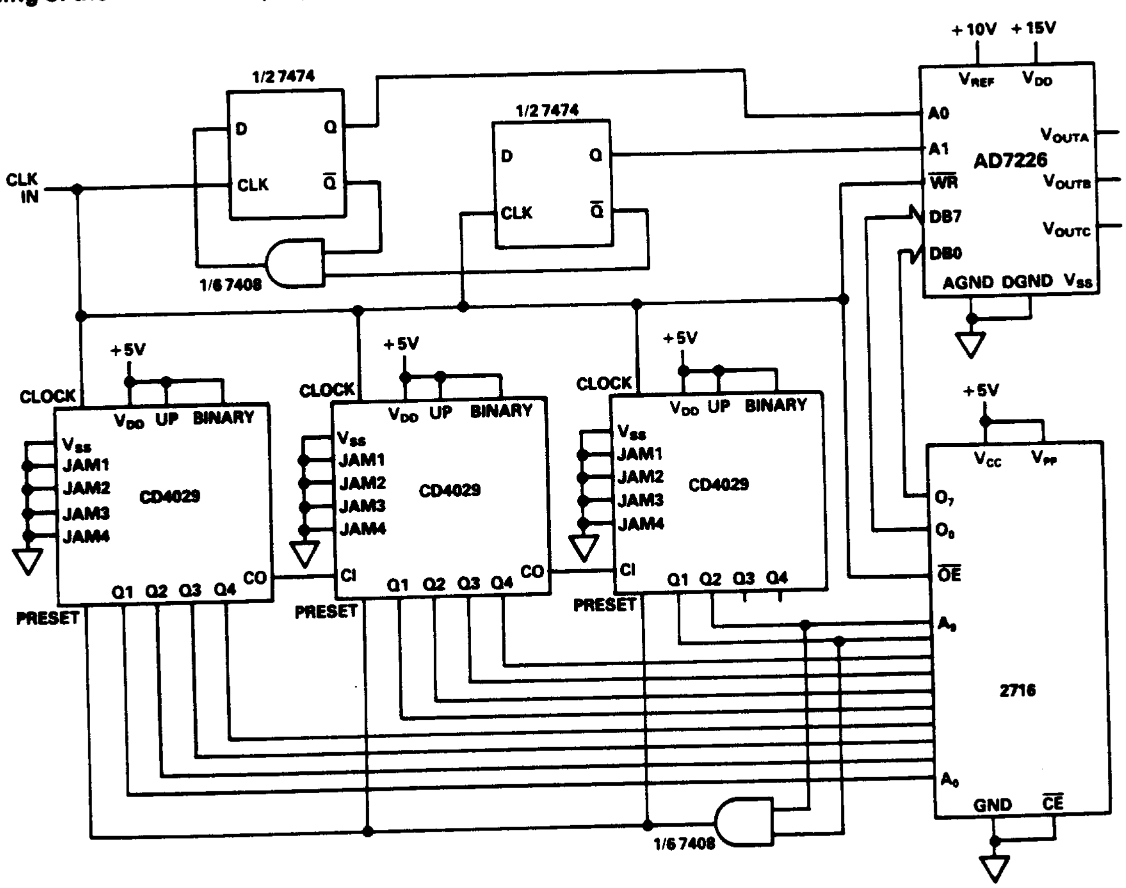

Figure 1. 3-Phase Sine Wave Circuit

The logic in the circuit controls the output of data from the 2716 and the loading of the D/A converters in the AD7226. It ensures that successive values from the EPROM are loaded to the D/A converters in turn. Referring to the example already given, data from Address X is loaded to DAC A, Address X+1 to DAC B, Address X+2 to DAC C, Address X+3 to DAC A again and so on. A full cycle for the three sine waves is generated by stepping through the full look-up table in the EPROM. When data from the last address has been loaded to the AD7226, the counter is reset and the cycle begins again.

With a 256-element sine table the output frequency is 1/768th of the input clock frequency. Varying the input clock frequency over the range 4kHz to 1MHz will vary the output frequency from a few Hz to 1.2kHz. The matching and tracking between the D/A converters of the AD7226 ensures a very good match between the output amplitude of each of the sine waves. Figure 2 shows some typical resulting waveforms, after filtering with a simple RC, for a 1.2kHz output frequency. This was found to be the maximum frequency at which the circuit could be run without appreciable change in the distortion figures for the output waveforms. The limiting factor on the frequency range is the 450ns data access time specification of the 2716 EPROM. To increase the frequency range, the 2716 should be replaced by an EPROM with a faster access time. Alternatively, if a sine wave look-up table with less elements is used then the frequency of the output sine waves will be increased since the time to cycle through a full look-up table is decreased. For example, if an 85-element sine table is used, with the same clock frequency, then the maximum output frequency (again using the 2716 EPROM) is increased to 3.6kHz.

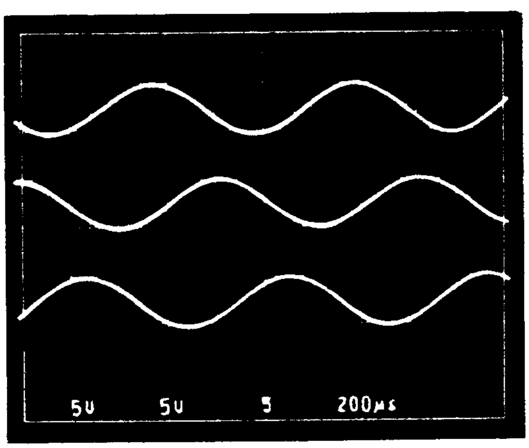

Figure 2. 3-Phase Sine Wave Output

Figure 3 shows typical harmonic distortion results using the circuit of Figure 1 after the output has been filtered by a single pole RC with a 3dB frequency slightly larger than the output frequency. The RC will not have a significant effect on the portion of the spectrum shown but will however remove harmonics of the sampling frequency. The results show that the largest harmonic of the sine wave is typically −55dB below the fundamental. The total harmonic distortion figure is typically −48dB. These distortion figures were achieved up to a frequency of 1.2kHz, using a 256-element sine wave table. When an 85-element table is used and the output frequency increased to 3.6kHz, the total harmonic distortion figures are not appreciably worse after the output has again been filtered with a simple RC circuit.

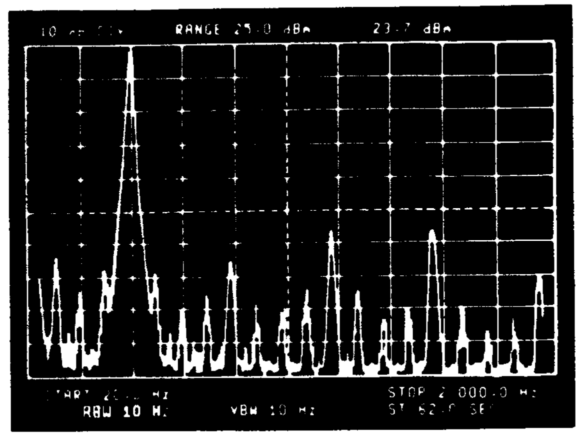

Figure 3a. Output Spectrum (400Hz)

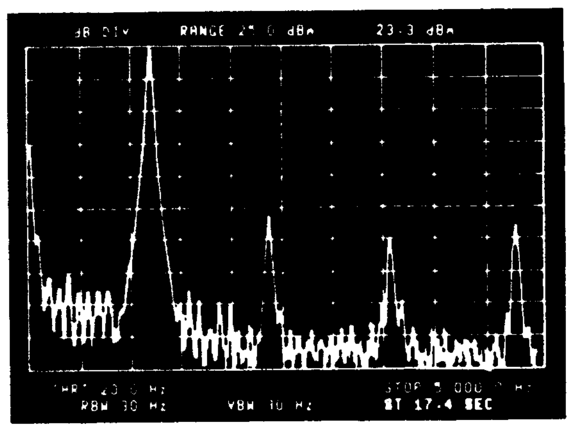

Figure 3b. Output Spectrum (1.2kHz)

A basic program for generating the code values for a 256-element sine wave table on the AIM-65 is shown in Table I. The program has to be run through a total of three times to fill all 768 locations of the sine wave look-up table.

```
INPUT "P";P
FOR X = 0 TO 255
LET A = SIN [(X * 1.40625 + P)/57.2958]
LET Y = INT (128.5 + 127 * A)
POKE L,Y
LET L = L + 3
NEXT X
END
```

NOTE: [L = 3328 and P = 0 for 1st Sine Wave
L = 3329 and P = 120 for 2nd Sine Wave
L = 3330 and P = 240 for 3rd Sine Wave]

Table I. Basic Program

In the program the numerical values which the SIN function acts upon are in radians. For lesser element sine tables line 2 in the program should be modified. For example, to get a 3 × 85-element table, STEP 3 should be added to the end of the line. The decoding to reset the counter would also have to be changed since the counter would now only count through 255 states.

In the circuit of Figure 1 the fourth D/A converter of the AD7226, DAC D, is not addressed. The circuit can easily be adapted to address this fourth DAC. In this case DAC D can be used in a feedback configuration to provide a programmable reference voltage for itself and the other three converters. This configuration is shown in the circuit of Figure 4. It means that the amplitude of the output sine waves can be programmed by varying the digital code in latch D. Note that varying the digital code in latch D varies the output amplitude of all three sine waves. The relationship of V_{REF} to V_{IN} is dependent upon digital code and upon the ratio of resistors R1 and R2. It can be expressed by the formula:

$$V_{REF} = \frac{(1+G)}{1+G \cdot D_D} \cdot V_{IN}$$

where $G = R2/R1$

and D_D is a fractional representation of the digital word in latch D $(0 \leq D_D \leq 255/256)$.

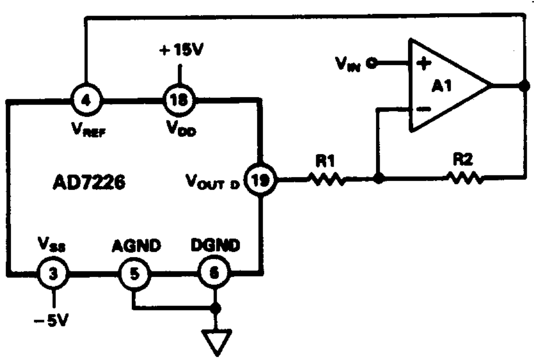

Figure 4. Self-Programmable Reference

Figure 5 shows typical plots of V_{REF} versus digital code for three different values of R2. With $V_{IN} = 2.5V$ and $R2 = 3R1$ the voltage at the output of A1 (i.e., the reference voltage for the AD7226) will vary between +2.5V and +10V over the digital input code range. The circuit of Figure 4 should only be used when the AD7226 is operated in dual supplies. This is because the AD7226 has reduced current sink capability at output voltages near 0V when used in single supply (see AD7226 data sheet). As a result the circuit would not operate correctly at lower values of digital input code. For correct operation with dual supplies R1 must be greater than 6.8kΩ.

The circuit of Figure 1 need not necessarily be used to generate 3-phase sine waves. Since the codes in the EPROM determine the shape of the output waveforms then the D/A converters can be made to produce various different outputs. For example, the circuit can be used to generate a square wave output from DAC A, a triangular wave output from DAC B and a sine wave output from DAC C, with all waveforms at the same frequency. The method for storing the codes in EPROM is as outlined before with the codes stored in sets of three. The resulting waveforms are shown in Figure 6. Once again, only three of the AD7226 outputs are used. This is because the circuit of Figure 1 is designed for selecting only three of the D/A converters. It can easily be adapted so that the fourth D/A converter can be used to provide a fourth output waveform. Alternatively, the fourth D/A converter can be used to program the amplitude of the output waveforms as before.

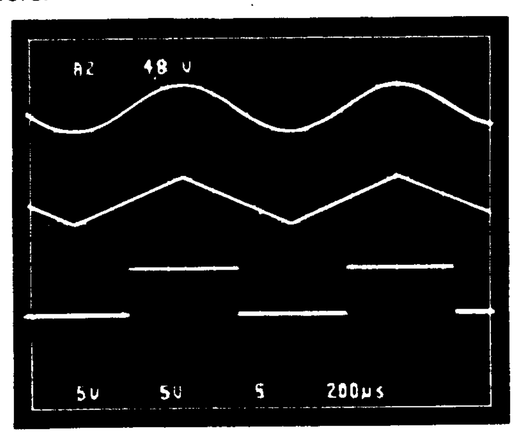

Figure 6. Output Waveforms

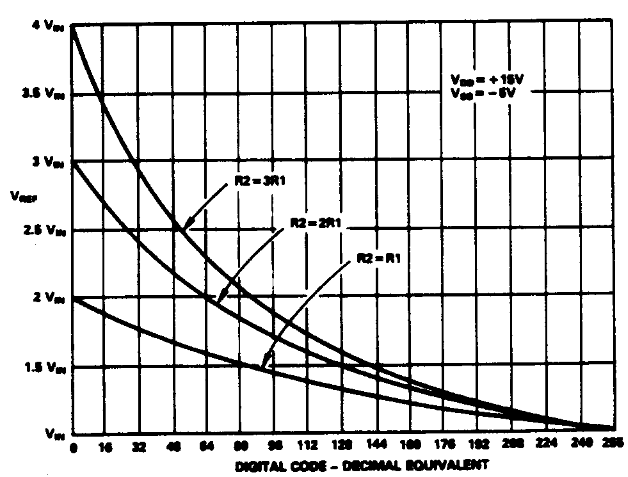

Figure 5. Variation of V_{REF} with Feedback Configuration