REAL TIME CLOCK

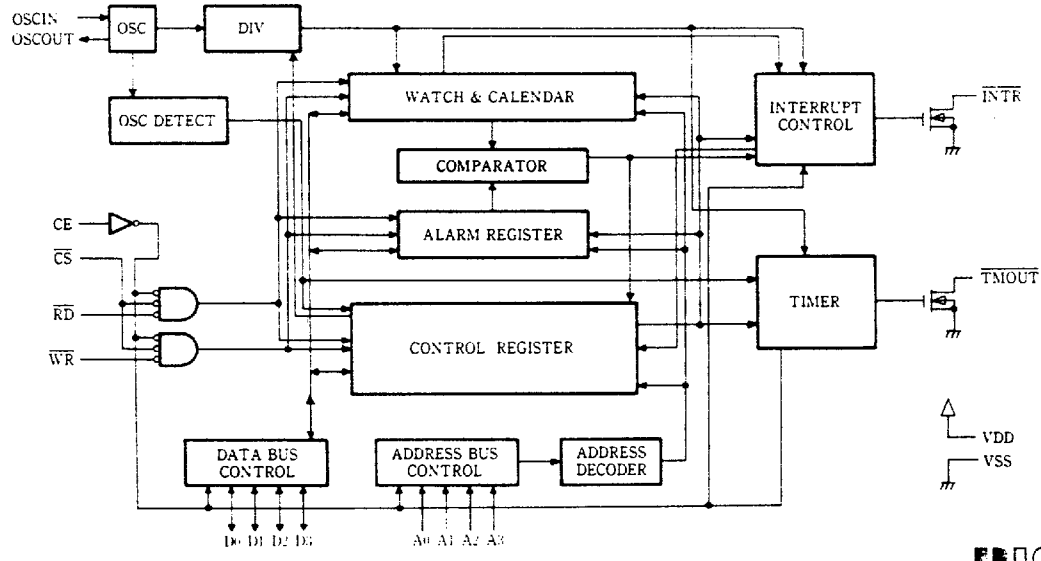
RP/RF/RS5C62

RP/RF/RS5C62 are CMOS real time clock LSIs for microcomputers. RP/RF/RS5C62 have clock, calendar, and alarm functions. They can be directly connected to the data buses of 8 bit or 16 bit CPUs such as 8086, Z80, 6809, 6502 and 68000. With a built-in timer counter, they can be used as watch-dog-timer or interrupt timer.

■ FEATURES

- Directly connected to CPU, enabling fast access.
- 4 bit bidirectional data bus, and 4 bit address bus.
- The oscillator is driven by a constant voltage, so the oscillation frequency is stable even when the power supply voltage fluctuates.
- Built-in timer counter using internal clock.
- Generates cyclic CPU interrupts, and generates alarm-match interrupts.
- Interrupt flag and interrupt inhibit.
- Clock (hour, minute, second), calendar (leap year, year, month, day, day of the week), alarm (hour, minute).
- 12- or 24-hour mode is selectable.
- Recognizes leap years automatically.
- All clock and alarm data expressed in BCD codes.
- ±30 seconds adjustment function.
- Determines whether clock data is valid or invalid.
- Consumes very low power due to CMOS technology, so it can be backed up by batteries.
- 5V single power supply.
- Package: 18-pin DIP for RP5C62, 18-pin SOP for RF5C62, 20-pin SSOP for RS5C62.

■ BLOCK DIAGRAM



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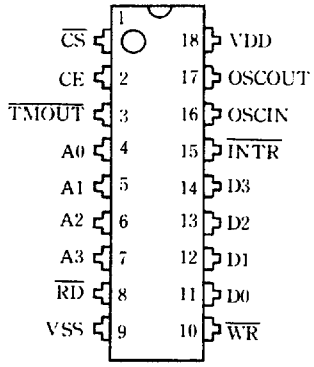
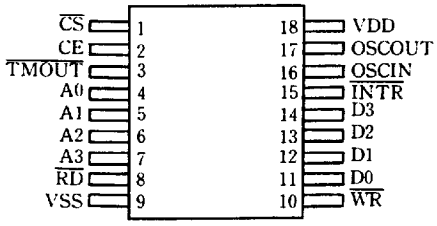
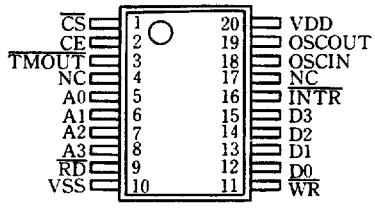
■ PIN CONFIGURATION



18 pin DIP



18 pin SOP



20 pin SSOP

■ PIN DESCRIPTION

Symbol	Name	Function
$\overline{CS}$ CE	Chip select Chip enable input	$\overline{CS}$ and CE are used when interfacing external devices. They may be accessed when $\overline{CS}$ is low and CE is high. CE is connected to a power down detector on the system power supply side, and $\overline{CS}$ is connected to the microcomputer address bus.
$\overline{TMOUT}$	Timer output	Timer output may be used as an interrupt free-run timer or watchdog timer. When CE is low (running on battery backup), operation stops (there is no output). It is N-ch open drain output.
A0 ~ A3	Address input	Address input is connected to the CPU address bus. It is gated internally with CE.
$\overline{RD}$	Read control input	When $\overline{RD}$ is set low, the contents of the counters or registers specified by A0~A3 are output to D0~D3. It is valid when $\overline{CS}$ is low and CE is high. It is CMOS input.
$\overline{WR}$	Write control input	When $\overline{WR}$ is low or rises from low to high, the contents of D0~D3 are written to registers or counters specified by A0~A3. $\overline{WR}$ is valid when $\overline{CS}$ is low and CE is high. It is CMOS input.
D0~D3	Bi-directional data bus	D0~D3 are connected to the CPU data bus. The input section is gated internally with CE. It is CMOS input/output.
$\overline{INTR}$	Interrupt output	$\overline{INTR}$ outputs timing CLOCK interrupts or alarm match interrupts to CPU. It also operates when CE is low (at battery backup). It is N-ch open drain output.
OSCIN OSCOUT	Oscillator circuit input/output	Crystal oscillator of 32.768 KHz must be connected between OSCIN and OSCOUT. Capacitance is connected externally between VDD and OSCIN and VDD and OSCOUT, forming the oscillator circuit.
VDD VSS	Power supply	VDD connects to +5V and VSS to ground.

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■ ABSOLUTE MAXIMUM RATINGS

(VSS = 0V)

Symbol	Parameter	Condition	Value	Unit
VDD	Supply Voltage		–0.3 ~ +7.0	V
VI	Input Voltage		–0.3 ~ +VDD+0.3	V
VO	Output Voltage 1	$\overline{INTR}$, $\overline{TMOUT}$	–0.3 ~ +12.0	V
	Output Voltage 2	Except $\overline{INTR}$, $\overline{TMOUT}$	–0.3 ~ +VDD+0.3	V
PD	Maximum Power Dissipation	TA = 25°C	300	mW
TA	Operating Temperature		–20 ~ +70	°C
TSTG	Storage Temperature		–40 ~ +125	°C

■ RECOMMENDED OPERATING CONDITION

(VSS = 0V, TA = –20 ~ +70°C)

Symbol	Parameter	Condition	MIN.	TYP.	MAX.	Unit
VDD	Supply Voltage		2.7	5.0	6.0	V
VCLK	Supply Voltage of Clock		2.0		6.0	V
fXT	Crystal Oscillation Frequency			32.768		kHz
V PUP	Pull-up Voltage for $\overline{INTR}$, $\overline{TMOUT}$ pin	$\overline{INTR}$, $\overline{TMOUT}$			10	V

■ DC CHARACTERISTICS

Symbol	Parameter	Pin Name	Condition	MIN.	TYP.	MAX.	Unit
VIH1	"H" input voltage	A0~A3, D0~D3		2.2		VDD+0.3	V
VIL1	"L" input voltage	$\overline{CS}$, $\overline{RD}$, $\overline{WR}$		–0.3		0.8	V
VIH2	"H" input voltage	CE		0.8*VDD		VDD+0.3	V
VIL2	"L" input voltage			–0.3		0.2*VDD	V
VOH1	"H" output voltage	D0~D3	IOH1 = –400µA	2.4			V
VOL1	"L" output voltage		IOL1 = 2mA			0.4	V
VOL2	"L" output voltage	$\overline{INTR}$, $\overline{TMOUT}$	IOL2 = 2mA			0.4	V
IILK	Input leak current	A0~A3, CE, $\overline{CS}$, $\overline{RD}$, $\overline{WR}$	VILK = VDD or VSS	–1		1	µA
IOZ1	Output off leak current	D0~D3	VOZ1 = VDD or VSS	–5		5	µA
IOZ2		$\overline{INTR}$, $\overline{TMOUT}$	VOZ2 = VDD	–2		2	µA
IOZ3		$\overline{INTR}$, $\overline{TMOUT}$	VOZ3 = 10V	–5		5	µA
IDD1	Consumption current for back-up	VDD	VDD = 2.5V, CE = L Others: OPEN			3	µA
IDD2	Consumption current for stand-by	VDD	VDD = 5.5V, CE = H $\overline{CS}$ = H, Output: OPEN Input: VDD or VSS			8	µA
∂f	Oscillation frequency drift for voltage drift	OSCIN OSCOUT	VDD = 2.5~5.5V	–1		1	ppm

(Unless Noted, VSS = 0V, VDD = 5V±10%, TA = –20~+70°C,
X'tal = 32.768 kHz (CI ≤ 35 kΩ), CG = CD = 10 pF)

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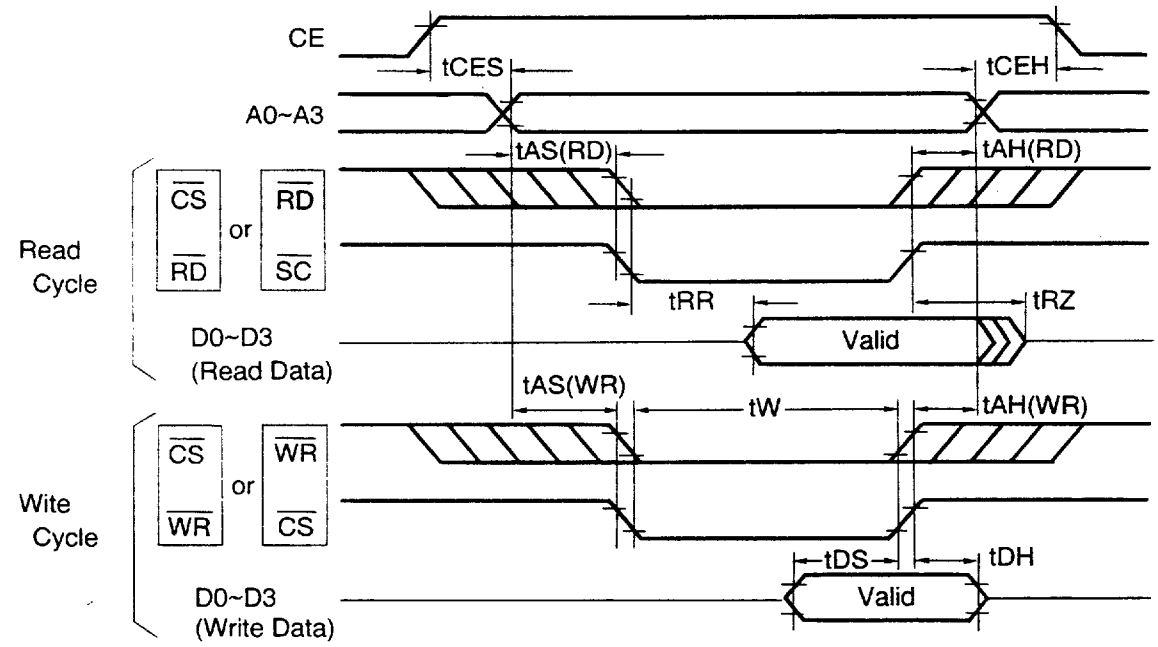
■ AC CHARACTERISTICS

(VSS = 0V, TA = −20 ~ +70°C)

Symbol	Parameter	VDD=5V±10%		VDD=3V±10%		VDD=5V±20%		Unit
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
tCES	CE Setup Time	500		1,000		500		ns
tCEH	CE Hold Time	500		1,000		500		ns
tAS(RD)	Address Setup Time(For Read)	20		20		20		ns
tAS(WR)	Address Setup Time(For Write)	20		20		20		ns
tAH(RD)	Address Hold Time(For Read)	10		10		10		ns
tAH(WR)	Address Hold Time(For Write)	10		10		10		ns
tRR	Output Data Delay Time(CL=100PF)		120		295		150	ns
tRZ	Output Data Floating Time		70		95		75	ns
tW	Write Pulse Width	120		195		150		ns
tDS	Input Data Setup Time	60		95		75		ns
tDH	Input Data Hold Time	10		10		10		ns

■ TIMING DIAGRAM



Input/Output Conditions

(VDD = 5V ± 10%)	(VDD = 3V ± 10%)	(VDD = 5V ± 20%)
VIH = 2.2V	VIH = 0.8 × VDD	VIH = 2.4V
VIL = 0.8V	VIL = 0.2 × VDD	VIL = 0.4V
VOH = 2.2V	VOH = 0.8 × VDD	VOH = 2.4V
VOL = 0.8V	VOL = 0.2 × VDD	VOL = 0.4V

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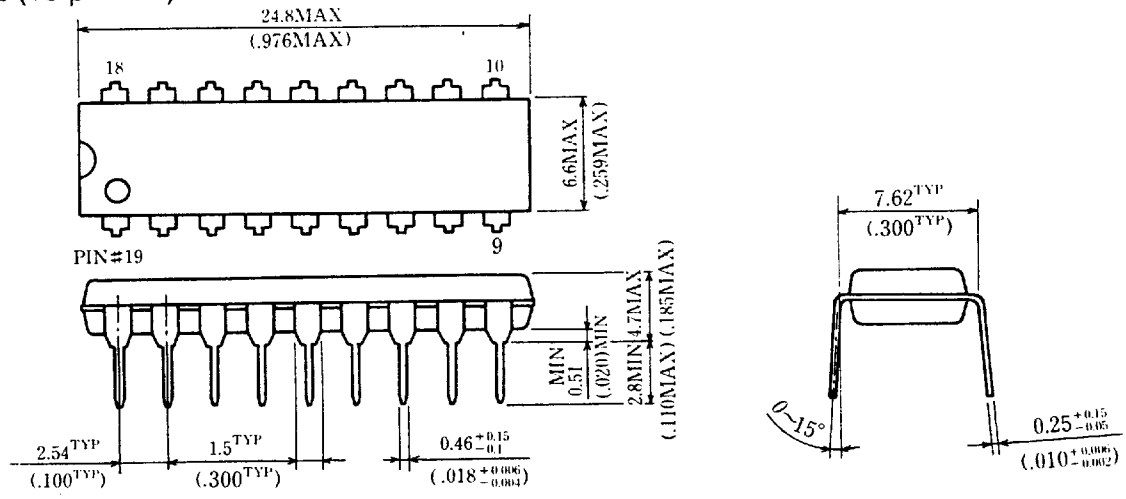
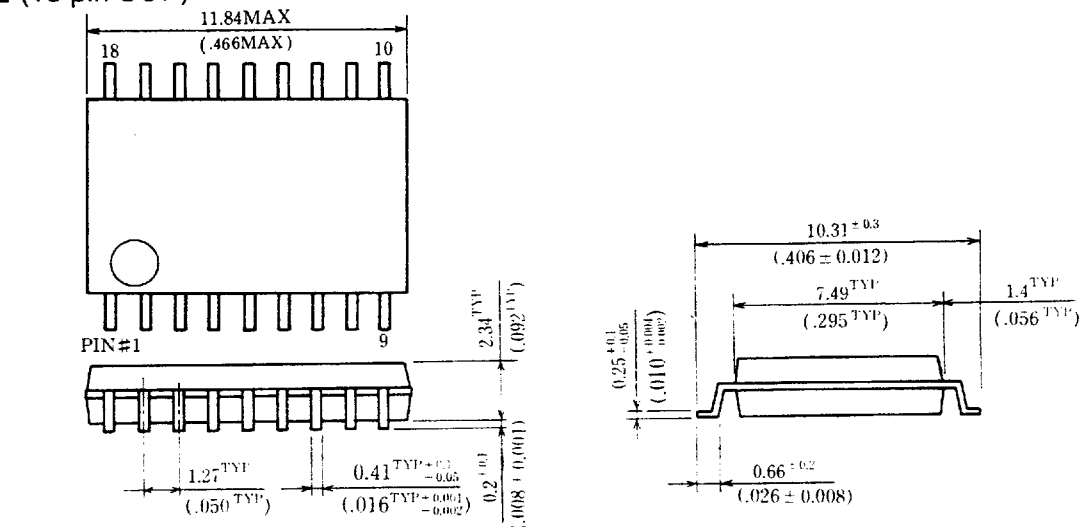
■ PACKAGE DIMENSION (Unit: mm/(inch))

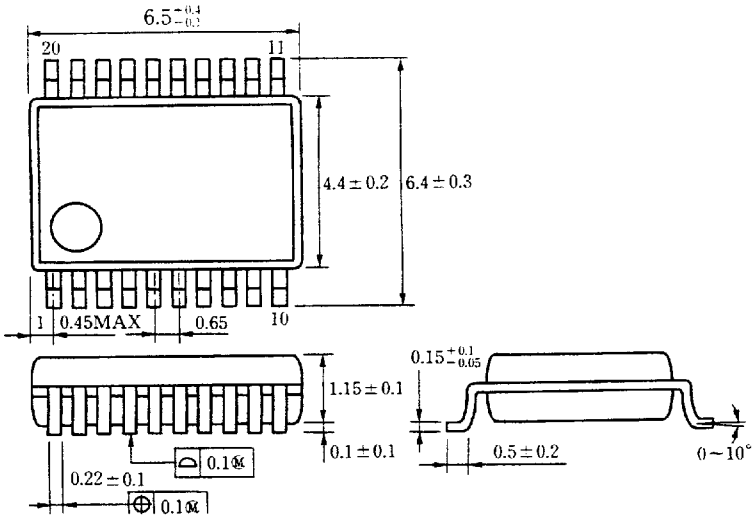
● RP5C62 (18 pin DIP)



● RF5C62 (18 pin SOP)



● RS5C62 (20 pin SSOP)



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■ FUNCTIONAL DESCRIPTION

1. Addressing

	Address Bus				BANK 0 (BANK = 0)					BANK 1 (BANK = 1)					
	A3	A2	A1	A0	Description	D3	D2	D1	D0	Description		D3	D2	D1	D0
0	0	0	0	0	Second Counter R/W	S_8	S_4	S_2	S_1	Cyclic interrupt select Reg.	W/O	CT_3	CT_2	CT_1	CT_0
1	0	0	0	1	10 sec. ↑		S_{40}	S_{20}	S_{10}	Adjust Reg.	W/O				ADJ
2	0	0	1	0	1 min. ↑	M_8	M_4	M_2	M_1	Alarm 1 min. Reg.	R/W	AM_8	AM_4	AM_2	AM_1
3	0	0	1	1	10 min. ↑		M_{40}	M_{20}	M_{10}	↑ 10 min.	↑		AM_{40}	AM_{20}	AM_{10}
4	0	1	0	0	1 hour ↑	H_8	H_4	H_2	H_1	↑ 1 hour	↑	AH_8	AH_4	AH_2	AH_1
5	0	1	0	1	10 hour ↑			P/$\overline{A}$ or H_{20}	H_{10}	↑ 10 hour	↑			AP/$\overline{A}$ or AH_{20}	AH_{10}
6	0	1	1	0	day of week ↑		W_4	W_2	W_1						
7	0	1	1	1	1 day ↑	D_8	D_4	D_2	D_1						
8	1	0	0	0	10 day ↑			D_{20}	D_{10}						
9	1	0	0	1	1 month ↑	MO_8	MO_4	MO_2	MO_1						
A	1	0	1	0	10 month ↑				MO_{10}	$\overline{12}$/24 select Reg.	W/O				$\overline{12}$/24
B	1	0	1	1	1 year ↑	Y_8	Y_4	Y_2	Y_1	Leap Year Reg.	R/O R/W		$\overline{LYE}$	LY_1	LY_0
C	1	1	0	0	10 year ↑	Y_{80}	Y_{40}	Y_{20}	Y_{10}	Timer Clock Select Reg.	W/O R/O	TM_3 TM_3	TM_2	TM_1	TM_0 TMFG
D	1	1	0	1	Control Reg. 1 W/O	WTEN	ALEN	TMR	BANK	Control Reg. 1	W/O	WTEN	ALEN	TMR	BANK
E	1	1	1	0	Control Reg. 2 R/O R/W	BSY	CTFG	ALFG	XSTP	Control Reg. 2	R/O R/W	BSY	CTFG	ALFG	XSTP
F	1	1	1	1	Control Reg. 3 W/O	$\overline{TSTA}$	$\overline{TSTB}$	WTRST		Control Reg. 3	W/O	$\overline{TSTA}$	$\overline{TSTB}$	WTRST	

Note 1) R/W bits can be read and written. R/O bits can only be read. W/O bits can only be written.
Note 2) It is no problem to attempt writing to R/O bits and don't care bits, but the attempt will fail.
Note 3) If W/O bits and don't care bits are read, the returned value is 0.

2. Counter/register functions

1) Clock and calendar counter (addresses 0 to C of BANK 0) (read and write)
   - The clock is in units of hour, minute, and second. The calendar function includes year, month, day and day of the week.
   - Data is expressed in BCD codes.
   - 12- or 24-hour time display is selectable for clock output. The display in the hour counter is as follows:
     12-hour display: AM12 → AM1 → ... → AM11 → PM12 → PM1 → ... → PM11 → AM12
     (The P/$\overline{A}$ bit indicates AM when 0 and PM when 1.)
     24-hour display: 0 → ... → 23 → 0
   - Write to the hour counter after selecting 12- or 24-hour time display by the 12/24 select register.
   - The day-of-week counter is a septinary counter, and is incremented when carried to the day counter. (Count $W_4 \cdot W_2 \cdot W_1 = 000 \rightarrow 001 \rightarrow 010 \rightarrow \ldots \rightarrow 110 \rightarrow 000$)

   Note 1) DO NOT write values which are not valid (such as AM15, or February 30). This causes misoperation.

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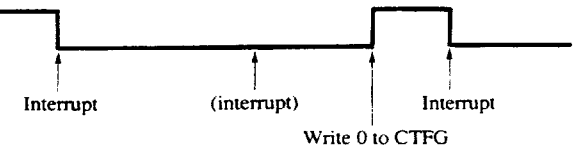
2) Cyclic interrupt select register (BANK 1 address 0) (write only)
   - Selects the cycle for cyclic interrupt based on the $\overline{INTR}$ output and the output mode.

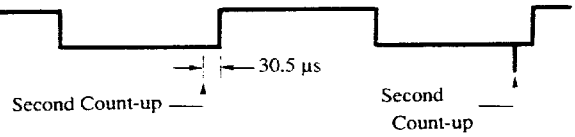
CT_3	CT_2	CT_1	CT_0	$\overline{INTR}$	Description
*	0	0	0	"OFF"	Inhibit cyclic interrupt
*	0	0	1	2048 Hz	Cycle T 0.488 ms (2048 Hz)
*	0	1	0	1024 Hz	↑ 0.977 ms (1024 Hz)
*	0	1	1	128 Hz	↑ 7.813 ms (128 Hz)
*	1	0	0	16 Hz	↑ 62.5 ms (16 Hz)
*	1	0	1	1 Hz	↑ 1 s (1 Hz)
*	1	1	0	1/60 Hz	↑ 60 s (1/60 Hz)
*	1	1	1	"ON"	$\overline{INTR}$ Output = "L"
0	*	*	*	Pulse mode	Cyclic pulse duty 50%
1	*	*	*	Level mode	Note 1)

Note 1) $\overline{INTR}$

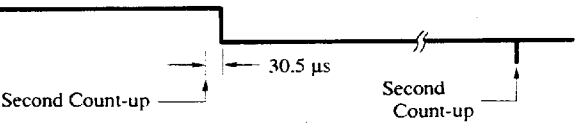


Note 2) $\overline{INTR}$ and Second Count-up

① pulse mode (1 Hz or 1/60 Hz select)



② level mode (1 Hz or 1/60 Hz select)



3) Adjustment register (BANK 1 address 1) (write only)
   - The adjustment register is for correcting seconds of clock and calendar counters. The second is adjusted by writing 1 to the ADJ bit.
     (a) When the second is 00 to 29: Makes the second counter 00, and does not carry to the minutes counter.
     (b) When the second is 30 to 59: Makes the second counter 00, and carries to the minutes counter.
   - It takes 122.1 µs at most to complete the adjustment after writing 1 to the ADJ bit. The BSY bit of the control register 2 is set to 1 until adjustment is completed. During that time, do not write to or read from the clock or calendar counter.

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4) Alarm register (BANK 1 addresses 2 to 5) (read and write)
   - This register stores hours and minutes for the alarm.
   - Data is expressed in BCD codes.
     (DO NOT write invalid values such as AM15. This causes misoperation.)

5) $\overline{12}$/24 select register (BANK 1 address A) (write only)
   - When the $\overline{12}$/24 bit of the $\overline{12}$/24 select register is 1, the 12-hour time display selected. If it is 0, the 24-hour time display is selected.
   - Set the 12- or 24-hour time display before adjusting the clock or setting the alarm.

6) Leap year register (BANK 1 address B) (read, partially write)
   - This register indicates leap years. When $LY_1 = LY_0 = 0$, it is a leap year. (LY_1 and LY_0 are read only.) Every time the year counter is incremented, LY_1 and LY_0 change as follows:
     $00 \rightarrow 01 \rightarrow 10 \rightarrow 11 \rightarrow 00$.
   - Setting the year counter automatically sets the leap year register. (A leap year is set when 84, 88, ... and 00 are set to the year counter.)
   - The $\overline{LYE}$ bit can be written to. It performs leap year operation when set to 0, and does not when set to 1. Writing to the year counter sets the $\overline{LYE}$ bit to 0.

7) Timer clock select register (BANK 1 address C) (write, partially read)
   - Selects the input clock for the timer counter (in the write mode).

TM_3	TM_2	TM_1	TM_0	T1 Note 1)	T2 Note 2)	T3 Note 3)
0	*	*	*	Timer Inhibit Note 5) ($\overline{TMOUT}$ = OFF)	←	←
1	0	0	0	562 ms	562 ~ 626 ms	625 ms
1	0	0	1	281 ms	281 ~ 313 ms	312.5 ms
1	0	1	0	140 ms	140 ~ 157 ms	156.3 ms
1	0	1	1	70.3 ms	70.3 ~ 78.2 ms	78.13 ms
1	1	0	0	35.1 ms	35.1 ~ 39.1 ms	39.06 ms
1	1	0	1	17.5 ms	17.5 ~ 19.6 ms	19.53 ms
1	1	1	0	8.78 ms	8.78 ~ 9.77 ms	9.766 ms
1	1	1	1	4.39 ms	4.39 ~ 4.89 ms	4.833 ms

Note 1) The maximum time for the reset cycle (maximum reset cycle when used as a watch-dog timer) not to output L from the $\overline{TMOUT}$ output after resetting the timer counter (writing 1 to the TMR bit of the control register 1).
Note 2) Time between the timer counter reset and the "L" pulse output from the $\overline{TMOUT}$ output.
Note 3) The cycle of a pulse output from the $\overline{TMOUT}$ output when the timer counter is not reset (That is, when used as a free-run timer. However, the time between the timer counter reset and the first pulse output from the $\overline{TMOUT}$ output is T2. The cycle for the second and subsequent pulses is T3).

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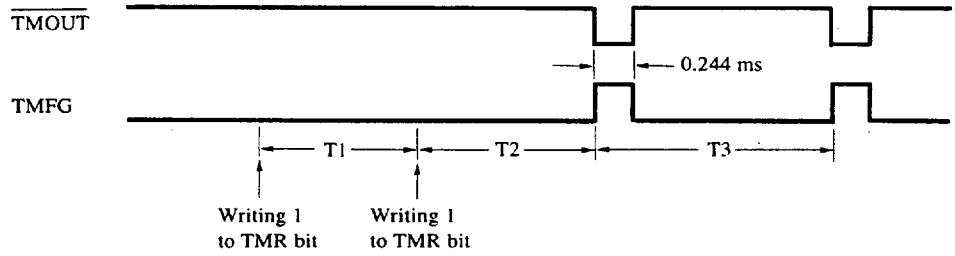
Note 4) When CE = "L" (battery backup), the timer stops ($\overline{TMOUT}$ output = OFF).
Note 5) When oscillation stop is detected (XSTP bit = 1), the TM_3 bit is reset to 0 and the timer is inhibited ($\overline{TMOUT}$ output = OFF).
Note 6) When TM_3 bit = 0, the timer counter is reset.

- When the $\overline{TMOUT}$ output is "L", the TMFG bit is "H" (in read mode).



8) Control register 1 (address D of BANK 0 or 1) (write only)
- Correspondence with data buses

D3	D2	D1	D0
WTEN	ALEN	TMR	BANK

① WTEN bit ..... When the WTEN bit is 1, clock counting is valid. When it is 0, clock counting is disabled (carrying of seconds is inhibited). This bit is also used when reading the time. (To read time, this bit is set to 0, then returned to 1 after reading. If a carry pulse is input to the seconds' counter while WTEN = 0, the seconds' counter is incremented by only +1 for compensation when WTEN bit is returned to 1. Only one carry is compensated correctly by +1. Even when there are two carries, only one carry is compensated.) When the CE input terminal is "L", this bit is set to 1.

② ALEN bit ..... When the ALEN bit is 1, the $\overline{INTR}$ output becomes "L" if the specified alarm time and the actual time match (alarm match operation). When this bit is 0, the alarm match operation is disabled.

③ TMR bit ..... Writing 1 to this bit resets the timer counter. This bit is used for watch-dog timers.

④ BANK bit ..... The BANK bit is for switching the address banks. When this bit is set to 0, BANK 0 is selected. When set to 1, BANK 1 is selected.

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9) Control register 2 (address E of BANK 0 or 1) (read, partially write)

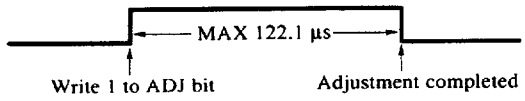
- Correspondence with data buses

D3	D2	D1	D0
BSY	CTFG	ALFG	XSTP

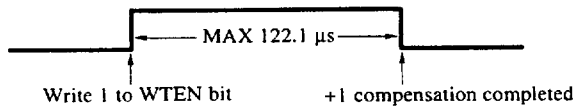
① BSY bit ..... When the BSY bit is 1, DO NOT read or write the time or calendar. The BSY bit is read only.

This bit is set to 1 in the following cases:

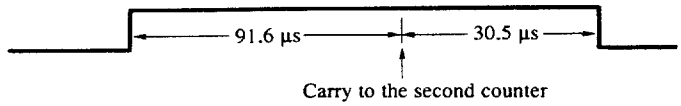
(i) ±30 second adjustment



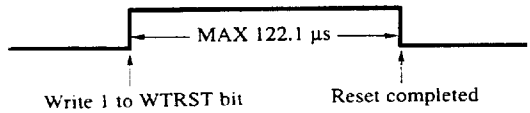
(ii) +1 compensation
(When one second is carried for compensation when returning WTEN from 0 to 1.)



(iii) Normal one second carry

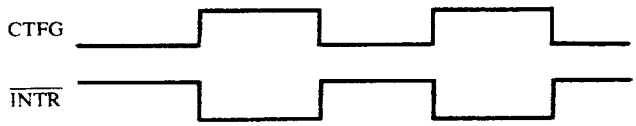


(iv) WTRST
(Resetting the 8 Hz to 1 Hz dividers)

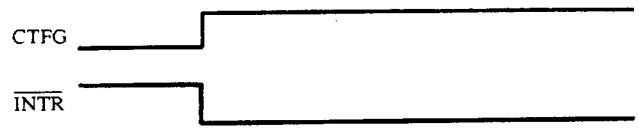


② CTFG bit ..... The CTFG bit is set to 1 when cyclic interrupts occur (INTR = "L"). The CTFG can be read. Only 0 can be written to it. A value of 1 cannot be written to it.

When CT_3 bit = 0
(pulse mode)



When CT_3 bit = 1
(level mode)



When CT_3 = 1 (level mode), writing 0 to this bit makes the $\overline{INTR}$ output "OFF" (in pulse mode, a write is not possible).

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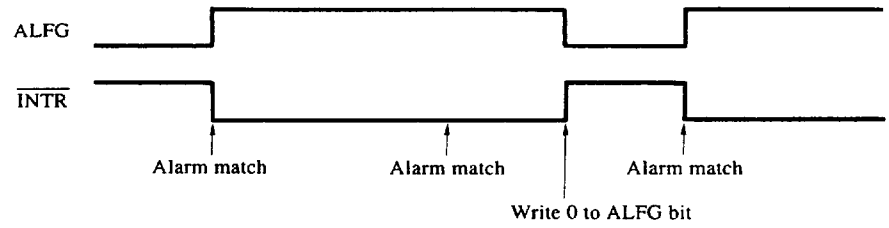
③ ALFG bit ..... The ALFG bit is set to 1 when there is an alarm match interrupt ($\overline{INTR}$ = "L"). The ALFG can be read. Only 0 can be written to it. 1 cannot be written to it.

When ALFG = 1, writing 0 to this bit makes the $\overline{INTR}$ output "OFF".



When ALFG = 1, writing 0 to this bit makes the $\overline{INTR}$ output "OFF".

④ XSTP bit ..... The XSTP bit is an oscillator stop detection bit, and is set to 1 once oscillation stops. This value is maintained even after oscillation restarts. When power is initially applied, this bit is set to 1 before oscillation starts. This bit can be used for determining whether the clock or alarm data is valid. The XSTP bit can be read. Only 0 can be written to it. A value of 1 cannot be written to it. When an oscillation stop is detected, the TM_3 bit of the timer clock select register is reset to 0, and the timer is inhibited ($\overline{TMOUT}$ output = OFF).

10) Control register 3 (Address F of BANK 0 or 1) (write only)

- Correspondence with data buses

D3	D2	D1	D0
$\overline{TSTA}$	$\overline{TSTB}$	WTRST	

① $\overline{TSTA}$ bit ..... The TSTA bit is a test bit. Writing 0 to this bit sets the test mode. Set this bit to 1 at initialization. This bit is set to 1 when CE = "L".

② $\overline{TSTB}$ bit ..... The TSTB bit is a test bit. Writing 0 to this bit sets the test mode. Set this bit to 1 at initialization. This bit is set to 1 when CE = "L".

③ WTRST bit ..... Writing 1 to the WTRST bit resets 8 Hz to 1 Hz dividers. The reset is released and counting starts a maximum of 122.1 μs after 1 is written to this bit. This bit is used to adjust the values of the seconds and lower counter.

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