

## MOSFET LDO Driver/Controller

Check for Samples: [LP2975](#)

### FEATURES

- Simple to Use, Few External Components
- Ultra-small VSSOP-8 Package
- 1.5% (A Grade) Precision Output Voltage
- Low-power Shutdown Input
- < 1  $\mu\text{A}$  in Shutdown
- Low Operating Current (180  $\mu\text{A}$  Typical @  $V_{\text{IN}} = 5\text{V}$ )
- Wide Supply Voltage Range (1.8V to 24V)
- Built-in Current Limit Amplifier
- Overtemperature Protection
- 5.0V, and 3.3V Standard Output Voltages
- Can be Programmed Using External Divider
- $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  Junction Temperature Range

### APPLICATIONS

- High-current 5V to 3.3V Regulator
- Post Regulator for Switching Converter
- Current-limited Switch

### DESCRIPTION

A high-current LDO regulator is simple to design with the LP2975 LDO Controller. Using an external P-FET, the LP2975 will deliver an ultra low dropout regulator with extremely low quiescent current.

High open loop gain assures excellent regulation and ripple rejection performance.

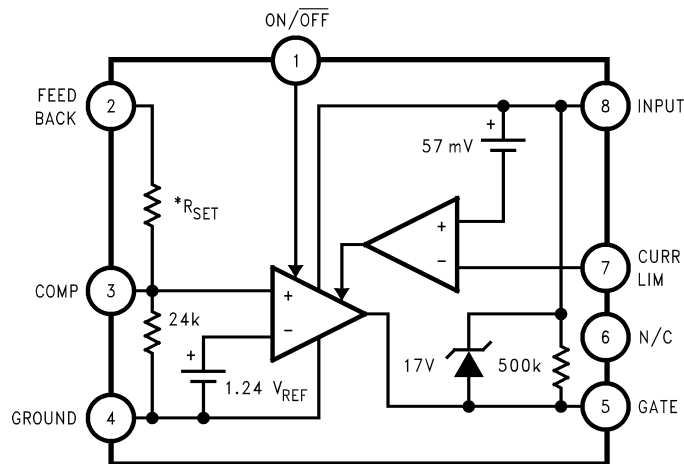
The trimmed internal bandgap reference provides precise output voltage over the entire operating temperature range.

Dropout voltage is “user selectable” by sizing the external FET: the minimum input-output voltage required for operation is the maximum load current multiplied by the  $R_{\text{DS(ON)}}$  of the FET.

Overcurrent protection of the external FET is easily implemented by placing a sense resistor in series with  $V_{\text{IN}}$ . The 57 mV detection threshold of the current sense circuitry minimizes dropout voltage and power dissipation in the resistor.

The standard product versions available provide output voltages of 5.0V, or 3.3V with specified  $25^{\circ}\text{C}$  accuracy of 1.5% (“A” grade) and 2.5% (standard grade).

### Block Diagram



\* $R_{\text{SET}}$  values are: 208k for 12V part, 72.8k for 5V part, and 39.9k for 3.3V part.



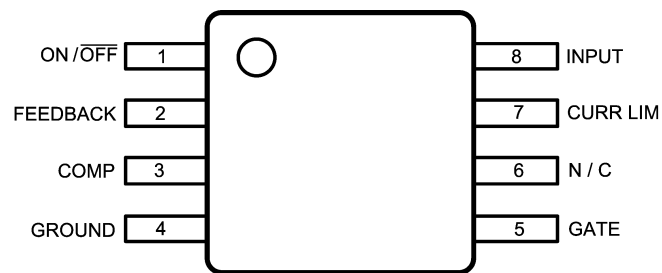
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## Connection Diagram



Device Pin 6 (N / C) has no internal connection

**Figure 1. 8-Lead VSSOP Surface Mount Package  
Top View  
See Package Number DGK0008A**



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Storage Temperature Range	–65°C to +150°C
Lead Temp. (Soldering, 5 seconds)	260°C
ESD Rating	2 kV
Power Dissipation <sup>(2)</sup>	Internally Limited
Input Supply Voltage (Survival)	–0.3V to +26V
Current Limit Pins (Survival)	–0.3V to +V <sub>IN</sub>
Comp Pin (Survival)	–0.3V to +2V
Gate Pin (Survival)	–0.3V to +V <sub>IN</sub>
ON/OFF Pin (Survival)	–0.3V to +20V
Feedback Pin (Survival)	–0.3V to +24V

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Electrical specifications do not apply when operating the device outside of its rated operating conditions.
- (2) The LP2975 has internal thermal shutdown which activates at a die temperature of about 150°C. It should be noted that the power dissipated within the LP2975 is low enough that this protection circuit should never activate due to self-heating, even at elevated ambient temperatures.

## OPERATING RATINGS

Junction Temperature, T <sub>J</sub>	–40°C to +125°C
Input Supply Voltage, V <sub>IN</sub>	+1.8V to +24V

## ELECTRICAL CHARACTERISTICS

Limits in standard typeface are for T<sub>J</sub> = 25°C, and limits in **boldface type** apply over the full operating junction temperature range. Unless otherwise specified: V<sub>ON/OFF</sub> = 1.5V, V<sub>IN</sub> = 15V.

Symbol	Parameter	Conditions	Typ	LM2975AI-X.X (1)		LM2975I-X.X (1)		Units
				Min	Max	Min	Max	
V <sub>REG</sub>	Regulation Voltage (12V Versions)	12.5 < V <sub>IN</sub> < 24V (V <sub>IN</sub> - 0.5V) > V <sub>GATE</sub> > (V <sub>IN</sub> - 5V)	12.0	11.820 <b>11.640</b>	12.180 <b>12.360</b>	11.700 <b>11.520</b>	12.300 <b>12.480</b>	V
	Regulation Voltage (5V Versions)	5.5 < V <sub>IN</sub> < 24V (V <sub>IN</sub> - 0.5V) > V <sub>GATE</sub> > (V <sub>IN</sub> - 4.5V)	5.0	4.925 <b>4.850</b>	5.075 <b>5.150</b>	4.875 <b>4.800</b>	5.125 <b>5.200</b>	
	Regulation Voltage (3.3V Versions)	3.8 < V <sub>IN</sub> < 24V (V <sub>IN</sub> - 0.5V) > V <sub>GATE</sub> > (V <sub>IN</sub> - 3.3V)	3.3	3.250 <b>3.201</b>	3.350 <b>3.399</b>	3.217 <b>3.168</b>	3.383 <b>3.432</b>	
V <sub>COMP</sub>	Comp Pin Voltage	V <sub>REG</sub> < V <sub>IN</sub> < 24V	1.240	1.215 <b>1.209</b>	1.265 <b>1.271</b>	1.203 <b>1.196</b>	1.277 <b>1.284</b>	V
I <sub>Q</sub>	Quiescent Current	V <sub>IN</sub> = 5V	180		240 <b>320</b>		240 <b>320</b>	μA
		V <sub>ON/OFF</sub> = 0V	0.01		<b>1</b>		<b>1</b>	
V <sub>CL</sub>	Current Limit Sense Voltage	V <sub>IN</sub> = 15V V <sub>FB</sub> = 0.9 X V <sub>REG</sub>	57	45 <b>39</b>	69 <b>72</b>	45 <b>39</b>	69 <b>72</b>	mV
V <sub>ON/OFF</sub>	ON/OFF Threshold	Output = ON	0.94	1.10 <b>1.20</b>		1.10 <b>1.20</b>		V
		Output = OFF	0.87		0.70 <b>0.40</b>		0.70 <b>0.40</b>	
I <sub>ON/OFF</sub>	ON/OFF Input Bias Current	V <sub>ON/OFF</sub> = 1.5V	34		50 <b>75</b>		50 <b>75</b>	μA
I <sub>G</sub>	Gate Drive Current (Sourcing)	V <sub>G</sub> = 7.5V V <sub>FB</sub> = 1.1 X V <sub>REG</sub>	3.5	1.3 <b>0.3</b>		1.3 <b>0.3</b>		mA
	Gate Drive Current (Sinking)	V <sub>G</sub> = 7.5V V <sub>FB</sub> = 0.9 X V <sub>REG</sub>	1100	350 <b>40</b>		350 <b>40</b>		

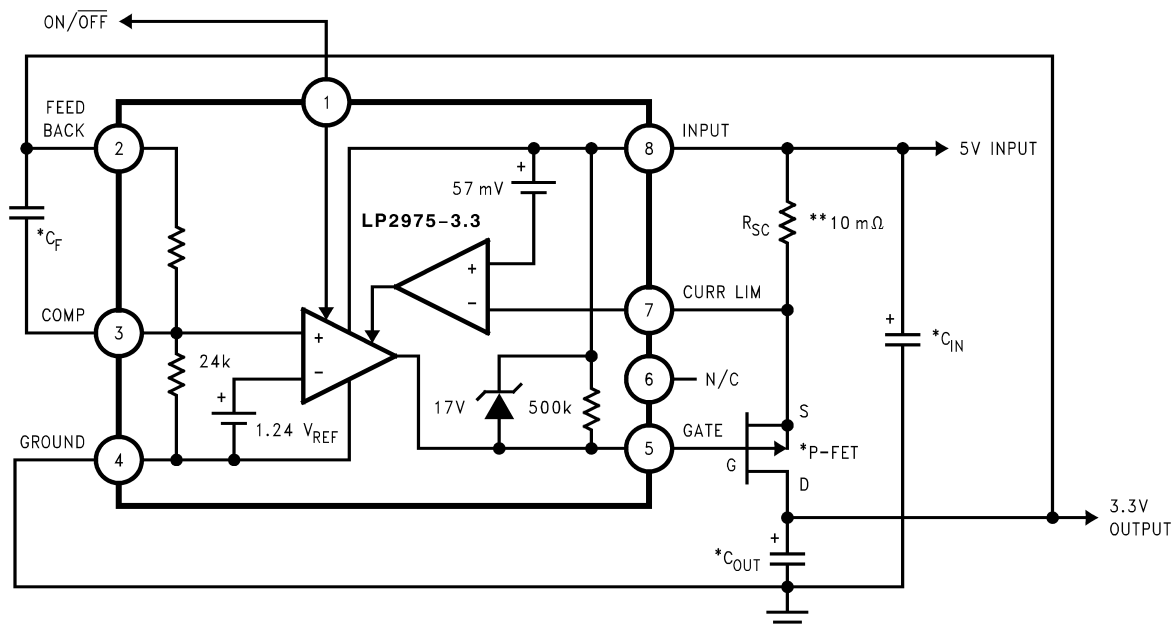
- (1) Limits are 100% production tested at 25°C. Limits over the operating temperature range are specified through correlation using Statistical Quality Control (SQC) methods. The limits are used to calculate TI's Average Outgoing Quality Level (AOQL).

## ELECTRICAL CHARACTERISTICS (continued)

Limits in standard typeface are for  $T_J = 25^\circ\text{C}$ , and limits in **boldface type** apply over the full operating junction temperature range. Unless otherwise specified:  $V_{\text{ON/OFF}} = 1.5\text{V}$ ,  $V_{\text{IN}} = 15\text{V}$ .

Symbol	Parameter	Conditions	Typ	LM2975AI-X.X (1)		LM2975I-X.X (1)		Units
				Min	Max	Min	Max	
$V_{\text{G(MIN)}}$	Gate Clamp Voltage	$V_{\text{IN}} = 24\text{V}$ $V_{\text{FB}} = 0.9 \times V_{\text{REG}}$	17	15	19	15	19	V
$R(V_{\text{IN-G}})$	Resistance from Gate to $V_{\text{IN}}$	$V_{\text{IN}} = 24\text{V}$ $V_{\text{ON/OFF}} = 0$	500					k $\Omega$
$\Delta V_{\text{GATE}} / \Delta V_{\text{COMP}}$	Open Loop Voltage Gain	$V_{\text{IN}} = 15\text{V}$ $0.5\text{V} \leq V_{\text{GATE}} \leq 13$	5000					V/V

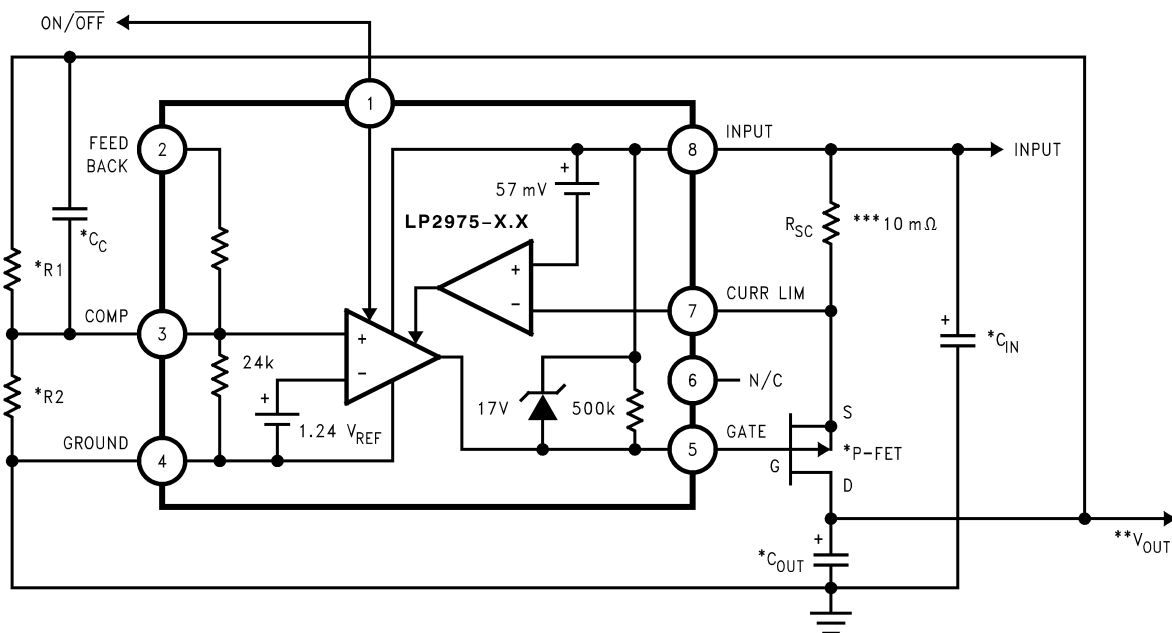
## TYPICAL APPLICATION CIRCUITS



\* See Application Hints: [Feed-Forward Capacitor](#).

\*\* If current limiting is not required, short out this resistor.

**Figure 2. 5V - 3.3V @ 5A LDO Regulator**



\* See Application Hints: [ADJUSTING THE OUTPUT VOLTAGE](#).

\*\*\* If current limiting is not required, short out this resistor.

**Figure 3. Adjustable Voltage 5A LDO Regulator**

## TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise specified:  $T_A = 25^\circ\text{C}$ ,  $C_{IN} = 1\ \mu\text{F}$ , ON/OFF pin is tied to 1.5V.

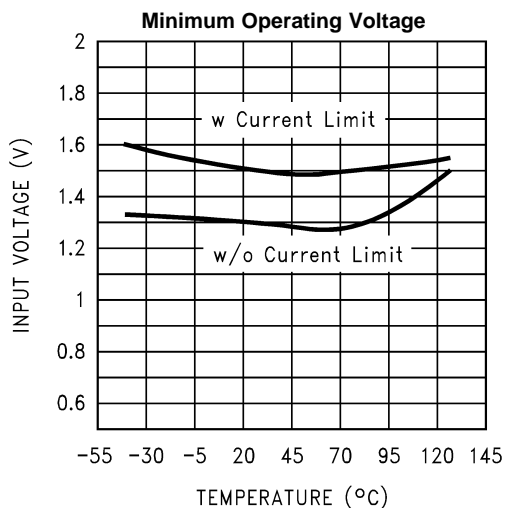


Figure 4.

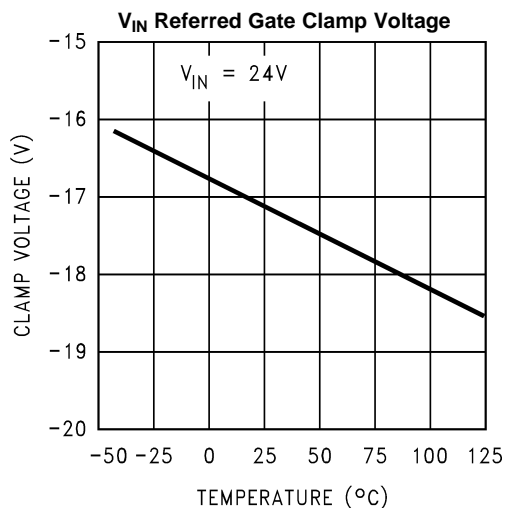


Figure 5.

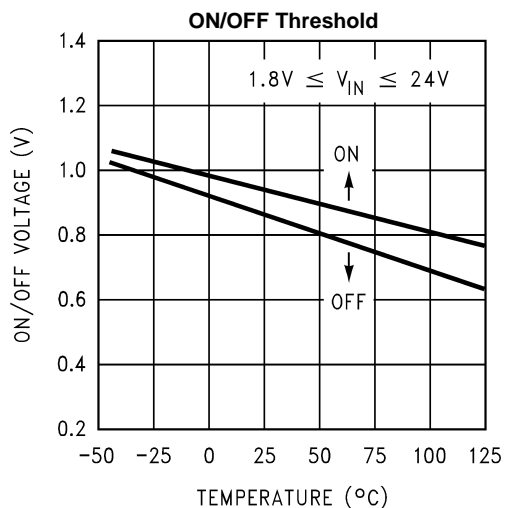


Figure 6.

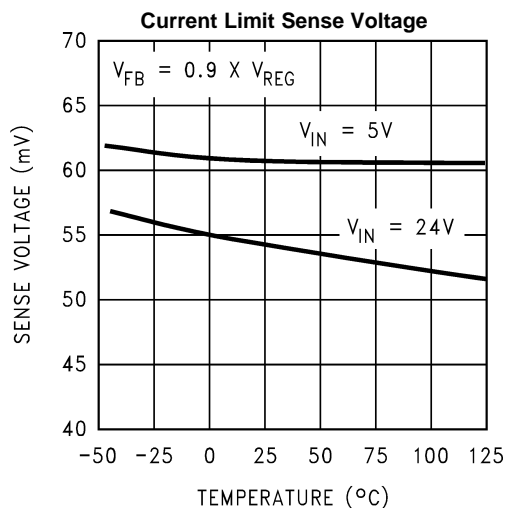


Figure 7.

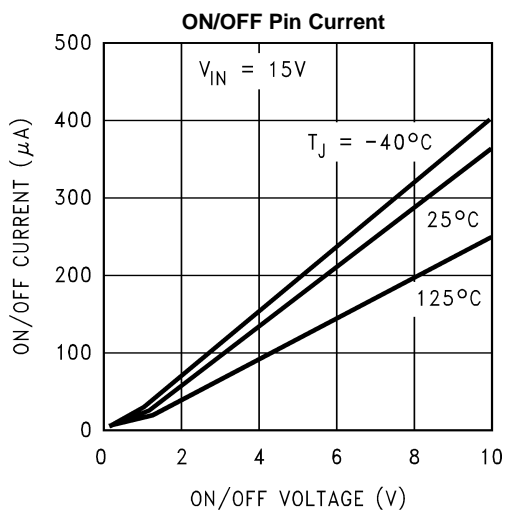


Figure 8.

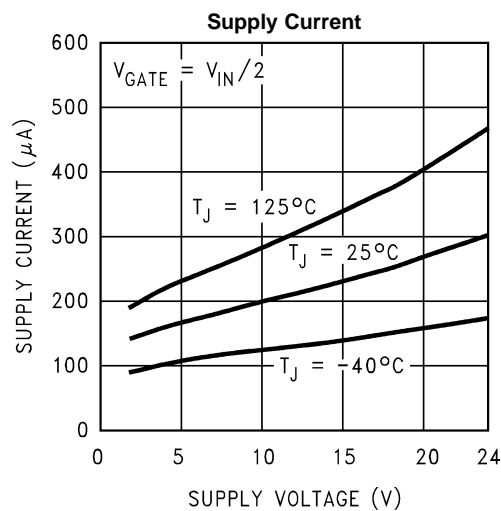


Figure 9.

## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified:  $T_A = 25^\circ\text{C}$ ,  $C_{IN} = 1\ \mu\text{F}$ , ON/OFF pin is tied to 1.5V.

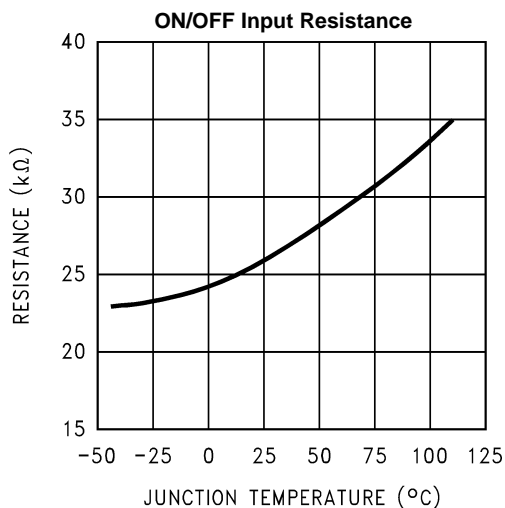


Figure 10.

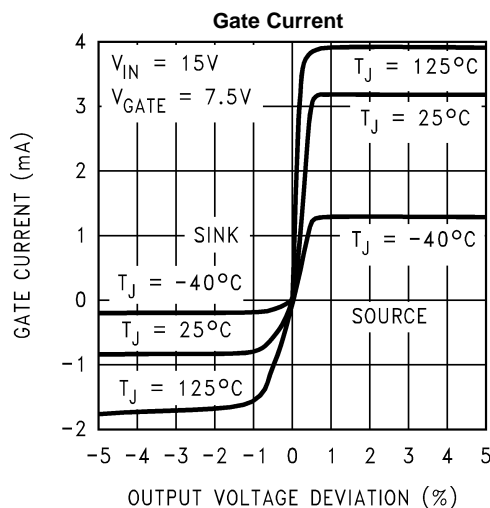


Figure 11.

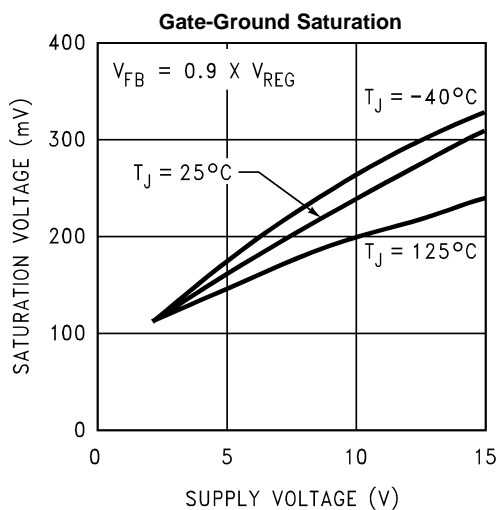


Figure 12.

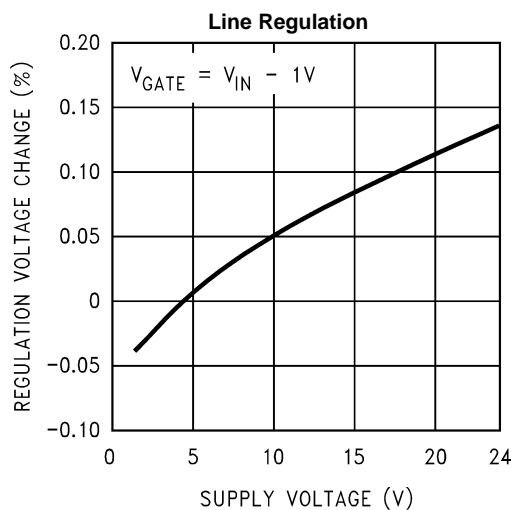


Figure 13.

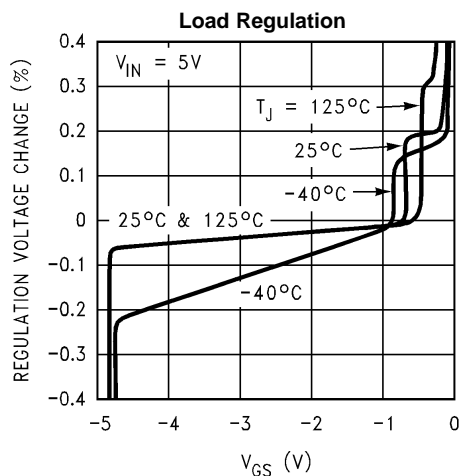


Figure 14.

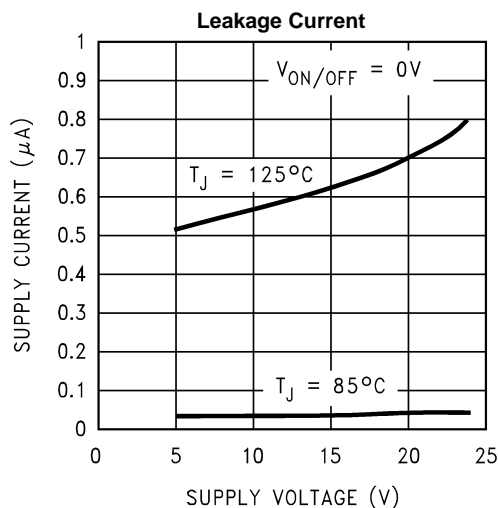
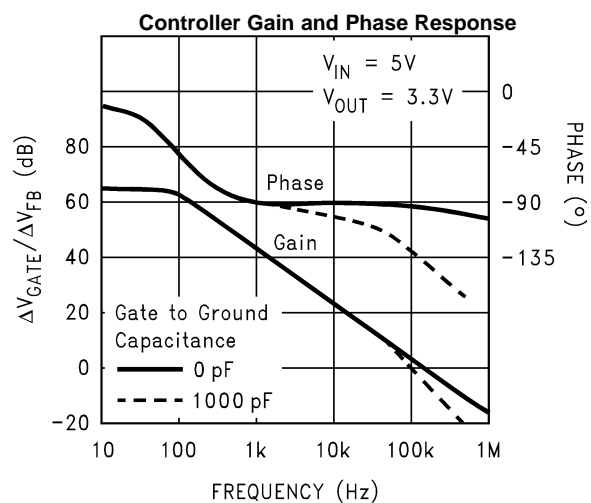


Figure 15.

## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified:  $T_A = 25^\circ\text{C}$ ,  $C_{IN} = 1\ \mu\text{F}$ , ON/OFF pin is tied to 1.5V.





## REFERENCE DESIGNS

The LP2975 controller can be used with virtually any P-channel MOSFET to build a wide variety of linear voltage regulators.

Since it would be impossible to document all the different voltage and current combinations that could be built, a number of reference designs will be presented along with performance data for each.

THE PERFORMANCE DATA SHOWN IS ACTUAL TEST DATA, BUT IS **NOT ENSURED**. The following reference designs have been confirmed with  $T_A = 25^\circ\text{C}$  only, and no design consideration is given for operating at any other ambient temperature.

### DESIGN #1: $V_{\text{OUT}} = 5\text{V} @ 5\text{A}$

(Refer to [TYPICAL APPLICATION CIRCUITS](#))

#### Components

$C_{\text{IN}} = 82\ \mu\text{F}$  Aluminum Electrolytic

$C_{\text{OUT}} = 120\ \mu\text{F}$  Aluminum Electrolytic

$C_F = 220\ \text{pF}$

$R_{\text{SC}} = 10\ \text{m}\Omega$

P-FET = NDP6020P

Heatsink: (assuming  $V_{\text{IN}} \leq 7\text{V}$  and  $T_A \leq 60^\circ\text{C}$ ) if protection against a *continuous* short-circuit is required, a heatsink with  $\theta_{\text{S-A}} \leq 1.5^\circ\text{C/W}$  must be used. However, if continuous short-circuit survivability is not needed, a heatsink with  $\theta_{\text{S-A}} \leq 6^\circ\text{C/W}$  is adequate.

#### Performance Data

##### Dropout Voltage

*Dropout voltage* is defined as the minimum input-to-output differential voltage required by the regulator to keep the output in regulation. It is measured by reducing  $V_{\text{IN}}$  until the output voltage drops below the nominal value (the nominal value is the output voltage measured with  $V_{\text{IN}} = 5.5\text{V}$ ).  $I_L = 5\text{A}$  for this test.

DROPOUT VOLTAGE = 323 mV

##### Load Regulation

*Load regulation* is defined as the maximum change in output voltage as the load current is varied. It is measured by changing the load resistance and recording the minimum/maximum output voltage. The measured change in output voltage is divided by the nominal output voltage and expressed as a percentage.  $V_{\text{IN}} = 5.6\text{V}$  for this test.

$5\ \text{mA} \leq I_L \leq 5\text{A}$ : LOAD REGULATION = 0.012%

$0 \leq I_L \leq 5\text{A}$ : LOAD REGULATION = 0.135%

##### Line Regulation

*Line regulation* is defined as the maximum change in output voltage as the input voltage is varied. It is measured by changing the input voltage and recording the minimum/maximum output voltage. The measured change in output voltage is divided by the nominal output voltage and expressed as a percentage.  $I_L = 5\text{A}$  for this test.

$5.4\text{V} \leq V_{\text{IN}} \leq 10\text{V}$ : LINE REGULATION = 0.03%

##### Output Noise Voltage

Output noise voltage was measured by connecting a wideband AC voltmeter (HP 400E) directly across the output capacitor.  $V_{\text{IN}} = 6\text{V}$  and  $I_L = 5\text{A}$  for this test.

NOISE = 75  $\mu\text{V}$  (rms)

### Transient Response

*Transient response* is defined as the change in output voltage which occurs after the load current is suddenly changed.  $V_{IN} = 5.6V$  for this test.

The load resistor is connected to the regulator output using a switch so that the load current increases from 0 to 5A abruptly. The change in output voltage is shown in the scope photo below (the vertical scale is 200 mV/division and the horizontal scale is 10  $\mu$ s/division). The regulator nominal output (5V) is located on the center line of the photo.

The output shows a maximum change of about -600 mV compared to nominal. This is due to the relatively small output capacitor chosen for this design. Increasing  $C_{OUT}$  greatly improves transient response (see [Design #2](#) and [Design #3](#)).

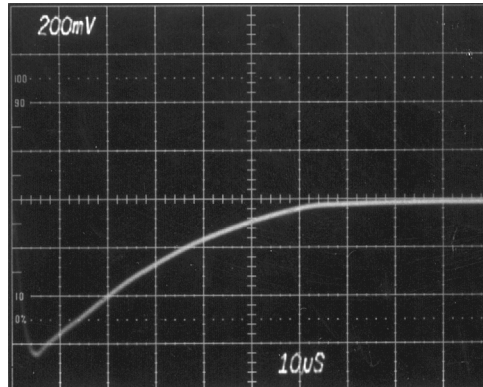


Figure 17. Transient Response for 0–5A Load Step

### DESIGN #2: $V_{OUT} = 3V @ 0.5A$

(Refer to [TYPICAL APPLICATION CIRCUITS, Adjustable Voltage Regulator](#))

#### Components

$C_{IN} = 68 \mu F$  Tantalum

$C_{OUT} = 2 \times 68 \mu F$  Tantalum

$C_C = 470 pF$

$R1 = 237 k\Omega$ , 1%

$R2 = \text{NOT USED}$

$R_{SC} = 0.1\Omega$

Tie feedback pin to  $V_{OUT}$

P-FET = NDT452P

Heatsink: Tab of N-FET is soldered down to 0.6 in<sup>2</sup> copper area on PC board.

Output Voltage Adjustment: For this application, a 3.3V part is “trimmed” down to 3V by using a single external 237 k $\Omega$  resistor at R1, which parallels the internal 39.9 k $\Omega$  resistor (reducing the effective resistance to 34.2 k $\Omega$ ).

Because the tempco of the external resistor will not match the tempco of the internal resistor (which is typically 3000 ppm), this method of adjusting  $V_{OUT}$  by using a single resistor is only recommended in cases where the output voltage is adjusted  $\leq 10\%$  away from the nominal value.

## Performance Data

### Dropout Voltage

*Dropout voltage* is defined as the minimum input-to-output differential voltage required by the regulator to keep the output in regulation. It is measured by reducing  $V_{IN}$  until the output voltage drops below the nominal value (the nominal value is the output voltage measured with  $V_{IN} = 5V$ ).  $I_L = 0.5A$  for this test.

DROPOUT VOLTAGE = 141 mV

### Load Regulation

*Load regulation* is defined as the maximum change in output voltage as the load current is varied. It is measured by changing the load resistance and recording the minimum/maximum output voltage. The measured change in output voltage is divided by the nominal output voltage and expressed as a percentage.  $V_{IN} = 3.5V$  for this test.

$0 \leq I_L \leq 0.5A$ : LOAD REGULATION = 0.034%

### Line Regulation

*Line regulation* is defined as the maximum change in output voltage as the input voltage is varied. It is measured by changing the input voltage and recording the minimum/maximum output voltage. The measured change in output voltage is divided by the nominal output voltage and expressed as a percentage.  $I_L = 0.5A$  for this test.

$3.5V \leq V_{IN} \leq 6V$ : LINE REGULATION = 0.017%

### Output Noise Voltage

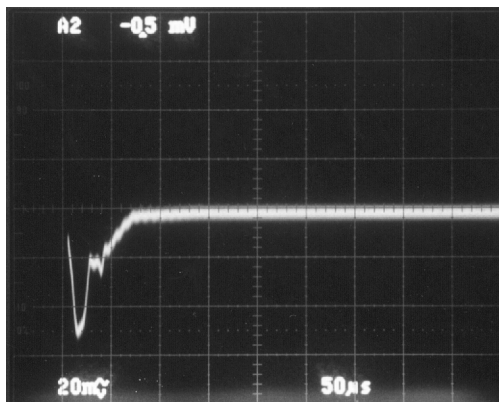
*Output noise voltage* was measured by connecting a wideband AC voltmeter (HP 400E) directly across the output capacitor.  $V_{IN} = 5V$  and  $I_L = 0.5A$  for this test.

NOISE = 85  $\mu V$  (rms)

### Transient Response

*Transient response* is defined as the change in output voltage which occurs after the load current is suddenly changed.  $V_{IN} = 3.5V$  for this test.

The load resistor is connected to the regulator output using a switch so that the load current increases from 0 to 0.5A abruptly. The change in output voltage is shown in the scope photo (the vertical scale is 20 mV/division and the horizontal scale is 50  $\mu s$ /division). The regulator nominal output (3V) is located on the center line of the photo. A maximum change of about -50 mV is shown.



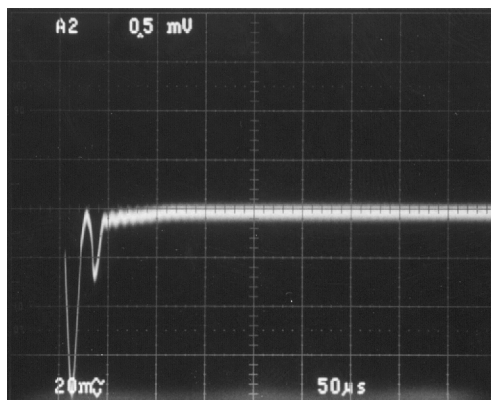
**Figure 18. Transient Response for 0–0.5A Load Step**

### Minimizing $C_{OUT}$

It is often desirable to decrease the value of  $C_{OUT}$  to save cost and reduce size. The design guidelines suggest selecting  $C_{OUT}$  to set the first pole  $\leq 200$  Hz (see later section, [Output Capacitor](#)), but this is not an absolute requirement in all cases.

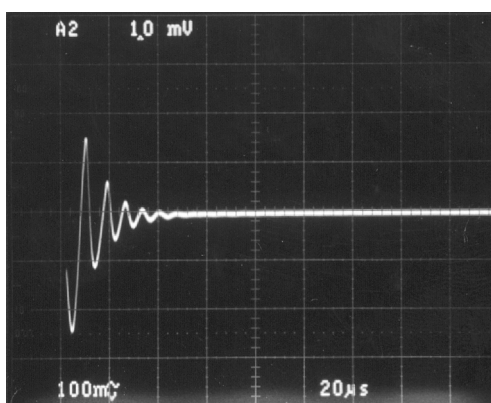
The effect of reducing  $C_{OUT}$  is to decrease phase margin. As phase margin is decreased, the output ringing will increase when a load step is applied to the output. Eventually, if  $C_{OUT}$  is made small enough, the regulator will oscillate.

To demonstrate these effects, the value of  $C_{OUT}$  in reference design #2 is halved by removing one of the two 68  $\mu\text{F}$  output capacitors and the transient response test is repeated (see photo below). The total overshoot increases from  $-50\text{ mV}$  to about  $-75\text{ mV}$ , and the second “ring” on the transient is noticeably larger.



**Figure 19. Transient Response with Output Capacitor Halved**

The design is next tested with only a 4.7  $\mu\text{F}$  output capacitor (see scope photo below). Observe that the vertical scale has been increased to 100 mV/division to accommodate the  $-250\text{ mV}$  undershoot. More important is the severe ringing as the transient decays. Most designers would recognize this immediately as the warning sign of a marginally stable design.



**Figure 20. Transient Response with Only 4.7  $\mu\text{F}$  Output Cap**

The reason this design is marginally stable is that the 4.7  $\mu\text{F}$  output capacitor (along with the 6  $\Omega$  output load) sets the pole  $f_p$  at 5 kHz. Analysis shows that the unity-gain frequency of the loop is increased to about 100 kHz, allowing the FET's gate capacitance pole  $f_{pg}$  to cause significant phase shift before the loop gain goes below unity. Also, because of the low output voltage, the feedforward capacitor provides less than  $10^\circ$  of positive phase shift. For good stability, the output capacitor needs to be larger than 4.7  $\mu\text{F}$ .

For detailed information on stability and phase margin, see the [Application Hints](#) section.

### DESIGN #3: $V_{OUT} = 1.5V @ 6A$ .

(Refer to [TYPICAL APPLICATION CIRCUITS](#), Adjustable Voltage Regulator)

#### Components

$C_{IN} = 1000 \mu F$  Aluminum Electrolytic

$C_{OUT} = 4 \times 330 \mu F$  OSCON Aluminum Electrolytic

$C_C =$  NOT USED

$R1 = 261\Omega$ , 1%

$R2 = 1.21 k\Omega$ , 1%

$R_{SC} = 6 m\Omega$

P-FET = NDP6020P

Heatsink: (Assuming  $V_{IN} \leq 3.3V$  and  $T_A \leq 60^\circ C$ ) if protection against a *continuous* short-circuit is required, a heatsink with  $\theta_{S-A} < 2.5^\circ C/W$  must be used. However, if continuous short-circuit survivability is not needed, a heatsink with  $\theta_{S-A} < 7^\circ C/W$  is adequate.

#### Performance Data

##### Dropout Voltage

*Dropout voltage* is defined as the minimum input-to-output differential voltage required by the regulator to keep the output in regulation. It is measured by reducing  $V_{IN}$  until the output voltage drops below the nominal value (the nominal value is the output voltage measured with  $V_{IN} = 3.3V$ ).  $I_L = 6A$  for this test.

DROPOUT VOLTAGE = 0.68V

##### Load Regulation

*Load regulation* is defined as the maximum change in output voltage as the load current is varied. It is measured by changing the load resistance and recording the minimum/maximum output voltage. The measured change in output voltage is divided by the nominal output voltage and expressed as a percentage.  $V_{IN} = 3.3V$  for this test.

$0 \leq I_L \leq 6A$ : LOAD REGULATION = 0.092%

##### Line Regulation

*Line regulation* is defined as the maximum change in output voltage as the input voltage is varied. It is measured by changing the input voltage and recording the minimum/maximum output voltage. The measured change in output voltage is divided by the nominal output voltage and expressed as a percentage.  $I_L = 6A$  for this test.

$3.3V \leq V_{IN} \leq 5V$ : LINE REGULATION = 0.033%

##### Output Noise Voltage

Output noise voltage was measured by connecting a wideband AC voltmeter (HP 400E) directly across the output capacitor.  $V_{IN} = 3.3V$  and  $I_L = 6A$  for this test.

NOISE = 60  $\mu V$  (rms)

##### Transient Response

*Transient response* is defined as the change in output voltage which occurs after the load current is suddenly changed.  $V_{IN} = 3.3V$  for this test.

The load resistor is connected to the regulator output using a switch so that the load current increases from 0 to 6A abruptly. The change in output voltage is shown in the scope photo (the vertical scale is 50 mV/division and the horizontal scale is 20  $\mu s$ /division. The regulator nominal output (1.5V) is located on the center line of the photo. A maximum change of about -80 mV is shown.

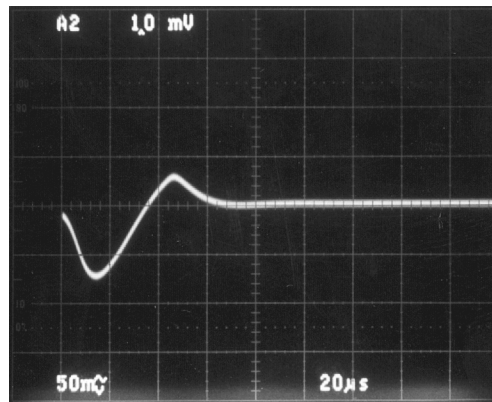


Figure 21. Transient Response for 0–6A Load Step

## Application Hints

### SELECTING THE FET

The best choice of FET for a specific application will depend on a number of factors:

**VOLTAGE RATING:** The FET must have a Drain-to-Source breakdown voltage (sometimes called  $BV_{DSS}$ ) which is greater than the input voltage.

**DRAIN CURRENT:** On-state Drain current must be specified to be greater than the worst-case (short circuit) load current for the application.

**TURN-ON THRESHOLD:** The Gate-to-Source voltage where the FET turns on (called the Gate Threshold Voltage) is very important. Many FET's are intended for use with G-to-S voltages in the 5V to 10V range. These should only be used in applications where the input voltage is high enough to provide >5V of drive to the Gate.

Newer FET's are becoming available with lower turn-on thresholds (Logic-Level FET's) which turn on fully with a gate voltage of only 3V to 4V. Low threshold FET's should be used in applications where the input voltage is  $\leq 5V$ .

**ON RESISTANCE:** FET on resistance (often called  $R_{DS(ON)}$ ) is a critical parameter since it directly determines the minimum input-to-output voltage required for operation at a given load current (also called **dropout voltage**).

$R_{DS(ON)}$  is highly dependent on the amount of Gate-to-Source voltage applied. For example, the  $R_{DS(ON)}$  of a FET with  $V_{G-S} = 5V$  will typically decrease by about 25% as the  $V_{G-S}$  is increased to 10V.  $R_{DS(ON)}$  is also temperature dependent, increasing at higher temperatures.

The dropout voltage of any LDO design is directly related to  $R_{DS(ON)}$ , as given by:

$$V_{DROPOUT} = I_{LOAD} \times (R_{DS(ON)} + R_{SC})$$

where

- $R_{SC}$  is the short-circuit current limit set resistor (see [TYPICAL APPLICATION CIRCUITS](#))

**GATE CAPACITANCE:** Selecting a FET with the lowest possible Gate capacitance improves LDO performance in two ways:

1. The Gate pin of the LP2975 (which drives the Gate of the FET) has a limited amount of current to source or sink. This means faster changes in Gate voltage (which corresponds to faster transient response) will occur with a smaller amount of Gate capacitance.
2. The Gate capacitance forms a pole in the loop gain which can reduce phase margin. When possible, this pole should be kept at a higher frequency than the cross-over frequency of the regulator loop (see later section, [Crossover Frequency and Phase Margin](#)).

A high value of Gate capacitance may require that a feedforward capacitor be used to cancel some of the excess phase shift (see later section, [Feed-Forward Capacitor](#)) to prevent loop instability.



**POWER DISSIPATION:** The maximum power dissipated in the FET in any application can be calculated from:

$$P_{MAX} = (V_{IN} - V_{OUT}) \times I_{MAX}$$

where

- $I_{MAX}$  is the maximum output current

It should be noted that if the regulator is to be designed to withstand short-circuit, a current sense resistor must be used to limit  $I_{MAX}$  to a safe value (refer to section [SHORT-CIRCUIT CURRENT LIMITING](#)).

The power dissipated in the FET determines the best choice for package type. A TO-220 package device is best suited for applications where power dissipation is less than 15W. Power levels above 15W would almost certainly require a TO-3 type device.

In low power applications, surface-mount package devices are size-efficient and cost-effective, but care must be taken to not exceed their power dissipation limits.

## POWER DISSIPATION AND HEATSINKING

Since the LP2975 controller is suitable for use with almost any external P-FET, it follows that designs can be built which have very high power dissipation in the pass FET. Since the controller can not protect the FET from overtemperature damage, thermal design must be carefully done to assure a reliable design.

**THERMAL DESIGN METHOD:** The temperature of the FET and the power dissipated is defined by the equation:

$$T_J = (\theta_{JA} \times P_D) + T_A$$

where

- $T_J$  is the junction temperature of the FET.
- $T_A$  is the ambient temperature.
- $P_D$  is the power dissipated by the FET.
- $\theta_{JA}$  is the junction-to-ambient thermal resistance.

To ensure a reliable design, the following guidelines are recommended:

1. Design for a maximum (worst-case) FET junction temperature which does not exceed 150°C.
2. Heatsinking should be designed for worst-case (maximum) values of  $T_A$  and  $P_D$ .
3. In designs which must survive a short circuit on the output, the maximum power dissipation must be calculated assuming that the output is shorted to ground:

$$P_D(MAX) = V_{IN} \times I_{SC}$$

where

- $I_{SC}$  is the short-circuit output current.

4. If the design is not intended to be short-circuit proof, the maximum power dissipation for intended operation will be:

$$P_D(MAX) = (V_{IN} - V_{OUT}) \times I_{MAX}$$

where

- $I_{MAX}$  is the maximum output current.

**LOW POWER (<2W) APPLICATIONS:** In most cases, some type of small surface-mount device will be used for the FET in low power designs. Because of the increased cell density (and tiny packages) used by modern FET's, the current carrying capability may easily exceed the power dissipation limits of the package. It is possible to parallel two or more FET's, which divides the power dissipation among all of the packages.

It should be noted that the "heatsink" for a surface mount package is the copper of the PC board and the package itself (direct radiation).

Surface-mount devices have the value of  $\theta_{JA}$  specified for a typical PC board mounting on their data sheet. In most cases it is best to start with the known data for the application ( $P_D$ ,  $T_A$ ,  $T_J$ ) and calculate the required value of  $\theta_{JA}$  needed. This value will define the type of FET and, possibly, the heatsink required for cooling.

$$\theta_{JA} = (T_J - T_A) / P_D(MAX)$$

**DESIGN EXAMPLE:** A design is to be done with  $V_{IN} = 5V$  and  $V_{OUT} = 3.3V$  with a maximum load current of 300 mA. Based on these conditions, power dissipation in the FET during normal operation would be:

$$P_D = (V_{IN} - V_{OUT}) \times I_{LOAD}$$

Solving, we find that  $P_D = 0.51W$ . Assuming that the maximum allowable value of  $T_J$  is  $150^\circ C$  and the maximum  $T_A$  is  $70^\circ C$ , the value of  $\theta_{J-A}$  is found to be  **$157^\circ C/W$** .

However, if this design must survive a continuous short on the output, the power dissipated in the FET is higher:

$$P_D(SC) = V_{IN} \times I_{SC} = 5 \times 0.33 = \mathbf{1.65W}$$

(This assumes the current sense resistor is selected for an  $I_{SC}$  value that is 10% higher than the required 0.3A).

The value of  $\theta_{J-A}$  required to survive continuous short circuit is calculated to be  **$49^\circ C/W$** .

Having solved for the value(s) of  $\theta_{J-A}$ , a FET can be selected. It should be noted that a FET must be used with a  $\theta_{J-A}$  value *less than or equal to the calculated value*.

**HIGH POWER ( $\geq 2W$ ) APPLICATIONS:** As power dissipation increases above 2W, a FET in a larger package must be used to obtain lower values of  $\theta_{J-A}$ . The same formulae derived in the previous section are used to calculate  $P_D$  and  $\theta_{J-A}$ .

Having found  $\theta_{J-A}$ , it becomes necessary to calculate the value of  $\theta_{S-A}$  (the heatsink-to-ambient thermal resistance) so that a heatsink can be selected:

$$\theta_{S-A} = \theta_{J-A} - (\theta_{J-C} + \theta_{C-S})$$

where

- $\theta_{J-C}$  is the junction-to-case thermal resistance. This parameter is the measure of thermal resistance between the semiconductor die inside the FET and the surface of the case of the FET where it mounts to the heatsink (the value of  $\theta_{J-C}$  can be found on the data sheet for the FET). A typical FET in a TO-220 package will have a  $\theta_{J-C}$  value of approximately  $2\text{--}4^\circ C/W$ , while a device in a TO-3 package will be about  $0.5\text{--}2^\circ C/W$ .
- $\theta_{C-S}$  is the case-to-heatsink thermal resistance, which measures how much thermal resistance exists between the surface of the FET and the heatsink.  $\theta_{C-S}$  is dependent on the package type and mounting method. A TO-220 package with mica insulator and thermal grease secured to a heatsink will have a  $\theta_{C-S}$  value in the range of  $1\text{--}1.5^\circ C/W$ . A TO-3 package mounted in the same manner will have a  $\theta_{C-S}$  value of  $0.3\text{--}0.5^\circ C/W$ . The best source of information for this is heatsink catalogs (Wakefield, Aavid, Thermalloy) since they also sell mounting hardware.
- $\theta_{S-A}$  is the heatsink-to-ambient thermal resistance, which defines how well a heatsink transfers heat into the air. Once this is determined, a heatsink must be selected which has a value which is less than or equal to the computed value.

The value of  $\theta_{S-A}$  is usually listed in the manufacturer's data sheet for a heatsink, but the information is sometimes given in a graph of temperature rise vs. dissipated power.

**DESIGN EXAMPLE:** A design is to be done which takes 3.3V in and provides 2.5V out at a load current of 7A. The power dissipation will be calculated for both normal operation and short circuit conditions.

For normal operation:

$$P_D = (V_{IN} - V_{OUT}) \times I_{LOAD} = \mathbf{5.6W}$$

If the output is shorted to ground:

$$P_D(SC) = V_{IN} \times I_{SC} = 3.3 \times 7.7 = \mathbf{25.4W}$$

(Assuming that a sense resistor is selected to set the value of  $I_{SC}$  10% above the nominal 7A).

$\theta_{J-A}$  will be calculated assuming a maximum  $T_A$  of  $70^\circ C$  and a maximum  $T_J$  of  $150^\circ C$ :

$$\theta_{J-A} = (T_J - T_A) / P_D(MAX)$$

For normal operation:

$$\theta_{J-A} = (150 - 70) / 5.6 = \mathbf{14.3^\circ C/W}$$

For designs which must operate with the output shorted to ground:

$$\theta_{J-A} = (150 - 70) / 25.4 = \mathbf{3.2^\circ C/W}$$



The value of 14.3°C/W can be easily met using a TO-220 device. Calculating the value of  $\theta_{S-A}$  required (assuming a value of  $\theta_{J-C} = 3^{\circ}\text{C/W}$  and  $\theta_{C-S} = 1^{\circ}\text{C/W}$ ):

$$\theta_{S-A} = \theta_{J-A} - (\theta_{J-C} + \theta_{C-S})$$

$$\theta_{S-A} = 14.3 - (3 + 1) = \mathbf{10.3^{\circ}\text{C/W}}$$

Any heatsink may be used with a thermal resistance  $\leq 10.3^{\circ}\text{C/W}$  @ 5.6W power dissipation (refer to manufacturer's data sheet curves). Examples of suitable heatsinks are Thermalloy #6100B and IERC #LATO127B5CB.

However, if the design must survive a sustained short on the output, the calculated  $\theta_{J-A}$  value of 3.2°C/W eliminates the possibility of using a TO-220 package device.

Assuming a TO-3 device is selected with a  $\theta_{J-C}$  value of 1.5°C/W and  $\theta_{C-S} = 0.4^{\circ}\text{C/W}$ , we can calculate the required value of  $\theta_{S-A}$ :

$$\theta_{S-A} = \theta_{J-A} - (\theta_{J-C} + \theta_{C-S})$$

$$\theta_{S-A} = 3.2 - (1.5 + 0.4) = \mathbf{1.3^{\circ}\text{C/W}}$$

A  $\theta_{S-A}$  value  $\leq 1.3^{\circ}\text{C/W}$  would require a relatively large heatsink, or possibly some kind of forced airflow for cooling.

## SHORT-CIRCUIT CURRENT LIMITING

Short-circuit current limiting is easily implemented using a single external resistor ( $R_{SC}$ ). The value of  $R_{SC}$  can be calculated from:

$$R_{SC} = V_{CL} / I_{SC}$$

where

- $I_{SC}$  is the desired short circuit current.
- $V_{CL}$  is the current limit sense voltage.

The value of  $V_{CL}$  is 57 mV (typical), with specified limits listed in the [ELECTRICAL CHARACTERISTICS](#) section. When doing a worst-case calculation for power dissipation in the FET, it is important to consider both the tolerance of  $V_{CL}$  and the tolerance (and temperature drift) of  $R_{SC}$ .

For maximum accuracy, the *INPUT* and *CURRENT LIMIT* pins must be Kelvin connected to  $R_{SC}$ , to avoid errors caused by voltage drops along the traces carrying the current from the input supply to the *Source* pin of the FET.

## EXTERNAL CAPACITORS

The best capacitors for use in a specific design will depend on voltage and load current (examples of tested circuits for several different output voltages and currents are provided in a previous section.)

Information in the next sections is provided to aid the designer in the selection of the external capacitors.

### Input Capacitor

Although not always required, an input capacitor is recommended. Good bypassing on the input assures that the regulator is working from a source with a low impedance, which improves stability. A good input capacitor can also improve transient response by providing a reservoir of stored energy that the regulator can utilize in cases where the load current demand suddenly increases. The value used for  $C_{IN}$  may be increased without limit. Refer to the [REFERENCE DESIGNS](#) section for examples of input capacitors.

### Output Capacitor

The output capacitor is required for loop stability (compensation) as well as transient response. During sudden changes in load current demand, the output capacitor must source or sink current during the time it takes the control loop of the LP2975 to adjust the gate drive to the pass FET. As a general rule, a larger output capacitor will improve both transient response and phase margin (stability). The value of  $C_{OUT}$  may be increased without limit.

**OUTPUT CAPACITOR AND COMPENSATION:** Loop compensation for the LP2975 is derived from  $C_{OUT}$  and, in some cases, the feed-forward capacitor  $C_F$  (see next section).

$C_{OUT}$  forms a pole (referred to as  $f_p$ ) in conjunction with the load resistance which causes the loop gain to roll off (decrease) at an additional  $-20$  dB/decade. The frequency of the pole is:

$$f_p = 0.16 / [(R_L + ESR) \times C_{OUT}]$$

where

- $R_L$  is the load resistance.
- $C_{OUT}$  is the value of the output capacitor.
- ESR is the equivalent series resistance of  $C_{OUT}$ .

As a general guideline, the frequency of  $f_p$  should be  $\leq 200$  Hz. It should be noted that higher load currents correspond to lower values of  $R_L$ , which requires that  $C_{OUT}$  be increased to keep  $f_p$  at a given frequency.

**DESIGN EXAMPLE:** Select the minimum required output capacitance for a design whose output specifications are 5V @ 1A:

$$f_p = 0.16 / [(R_L + ESR) \times C_{OUT}]$$

Re-written:

$$C_{OUT} = 0.16 / [f_p \times (R_L + ESR)]$$

Values used for the calculation:

$$f_p = 200 \text{ Hz}, R_L = 5\Omega, ESR = 0.1\Omega \text{ (assumed)}.$$

Solving for  $C_{OUT}$ , we get **157  $\mu$ F** (nearest standard size would be 180  $\mu$ F).

The ESR of the output capacitor is very important for stability, as it creates a zero ( $f_z$ ) which cancels much of the phase shift resulting from one of the poles present in the loop. The frequency of the zero is calculated from:

$$f_z = 0.16 / (ESR \times C_{OUT})$$

For best results in most designs, the frequency of  $f_z$  should fall between 5 kHz and 50 kHz. It must be noted that the values of  $C_{OUT}$  and ESR usually vary with temperature (severely in the case of aluminum electrolytics), and this must be taken into consideration.

For the design example ( $V_{OUT} = 5V @ 1A$ ), select a capacitor which meets the  $f_z$  requirements. Solving the equation for ESR yields:

$$ESR = 0.16 / (f_z \times C_{OUT})$$

Assuming  $f_z = 5$  kHz and 50 kHz, the limiting values of ESR for the 180  $\mu$ F capacitor are found to be:

$$18 \text{ m}\Omega \leq ESR \leq 0.18\Omega$$

A good-quality, low-ESR capacitor type such as the Panasonic HFQ is a good choice. However, the 10V/180  $\mu$ F capacitor (#ECA-1AFQ181) has an ESR of 0.3 $\Omega$  which is not in the desired range.

To assure a stable design, some of the options are:

1. Use a different type capacitor which has a lower ESR such as an organic-electrolyte OSCON.
2. Use a higher voltage capacitor. Since ESR is inversely proportional to the physical size of the capacitor, a higher voltage capacitor with the same C value will typically have a lower ESR (because of the larger case size). In this example, a Panasonic ECA-1EFQ181 (which is a 180  $\mu$ F/25V part) has an ESR of 0.17 $\Omega$  and would meet the desired ESR range.
3. Use a feed-forward capacitor (see next section).

### Feed-Forward Capacitor

Although not required in every application, the use of a feed-forward capacitor ( $C_F$ ) can yield improvements in both phase margin and transient response in most designs.

The added phase margin provided by  $C_F$  can prevent oscillations in cases where the required value of  $C_{OUT}$  and ESR can not be easily obtained (see previous section).

$C_F$  can also reduce the phase shift due to the pole resulting from the Gate capacitance, stabilizing applications where this pole occurs at a low frequency (before cross-over) which would cause oscillations if left uncompensated (see later section, [Gate Capacitance Pole Frequency \( \$f\_{pg}\$ \)](#)).

Even in a stable design, adding  $C_F$  will typically provide more optimal loop response (faster settling time). For these reasons, **the use of a feed-forward capacitor is always recommended.**

$C_F$  is connected across the top resistor in the divider used to set the output voltage (see [TYPICAL APPLICATION CIRCUITS](#)). This forms a zero in the loop response (defined as  $f_{zf}$ ), whose frequency is:

$$f_{zf} = 6.6 \times 10^{-6} / [C_F \times (V_{OUT} / 1.24 - 1)]$$

When solved for  $C_F$ , the  $f_{zf}$  equation is:

$$C_F = 6.6 \times 10^{-6} / [f_{zf} \times (V_{OUT} / 1.24 - 1)]$$

For most applications,  $f_{zf}$  should be set between 5 kHz and 50 kHz.

## ADJUSTING THE OUTPUT VOLTAGE

If an output voltage is required which is not available as a standard voltage, the LP2975 can be configured as an adjustable regulator (see [TYPICAL APPLICATION CIRCUITS](#)). The external resistors R1 and R2 (along with the internal 24 kΩ resistor) set the output voltage.

The use of any external resistors to alter the LP2975 pre-set output voltage is outside the specified operating conditions. Output voltage accuracy with external resistors will be inferior when compared to the tolerances of the LP2975 pre-set voltages options, and some external trim mechanism may be needed to achieve an acceptable initial accuracy of the custom output voltage. Users of this methodology are strongly encouraged to confirm that their custom circuit meets all of their performance requirements.

It is important to note that the external R2 is connected in parallel with the internal 24 kΩ resistor (typical). If we define  **$R_{EQ}$  as the total resistance between the COMP pin and ground**, then its value will be the parallel combination of R2 and 24 kΩ:

$$R_{EQ} = (R2 \times 24k) / (R2 + 24k)$$

It follows that the output voltage will be:

$$V_{OUT} = 1.24 [ (R1 / R_{EQ}) + 1 ]$$

Some important considerations for an adjustable LP2975 design:

The tolerance of the internal 24 kΩ resistor is about  $\pm 20\%$ . Also, its temperature coefficient is almost certainly different than the TC of any external resistor that is used for R2.

For these reasons, it is recommended that R2 be set at a value that is not greater than 1.2k. In this way, the value of R2 will dominate  $R_{EQ}$ , and the tolerance and TC of the internal 24k resistor will have a negligible effect on output voltage accuracy.

While this guideline for the value of R2 will generally provide adequate performance when operating with  $T_A = 25^\circ\text{C}$ , it is important to note that loading the COMP pin with 1.2kΩ, or less, to ground will impair device operation at elevated temperatures. For operation at temperatures above approximately  $50^\circ\text{C}$  it is recommended that the value of R2 should not be less than approximately 5kΩ.

To determine the value for R1:

$$R1 = R_{EQ} [ (V_{OUT} / 1.24) - 1 ]$$

### External Capacitors (Adjustable Application)

All information in the previous section, [EXTERNAL CAPACITORS](#), applies to the adjustable application with the exception of how to select the value of the feed-forward capacitor.

The feed-forward capacitor  $C_C$  in the adjustable application (see [TYPICAL APPLICATION CIRCUITS](#)) performs exactly the same function as described in the previous section, [Feed-Forward Capacitor](#). However, because R1 is user-selected, a different formula must be used to determine the value of  $C_C$ :

$$C_C = 1 / (2 \pi \times R1 \times f_{zf})$$

As stated previously, the optimal frequency at which to place the zero  $f_{zf}$  is usually between 5 kHz and 50 kHz.

## OPTIMIZING DESIGN STABILITY

Because the LP2975 can be used with a variety of different applications, there is no single set of components that are best suited to every design. This section provides information which will enable the designer to select components that optimize stability (phase margin) for a specific application.

### Gate Capacitance

An important consideration of a design is to identify the frequency of the pole which results from the capacitance of the Gate of the FET (this pole will be referred to as  $f_{pg}$ ). As  $f_{pg}$  gets closer to the loop crossover frequency, the phase margin is reduced. Information will now be provided to allow the total Gate capacitance to be calculated so that  $f_{pg}$  can be approximated.

The first step in calculating  $f_p$  is to determine how much **effective Gate capacitance ( $C_{EFF}$ )** is present. The formula for calculating  $C_{EFF}$  is:

$$C_{EFF} = C_{GS} + C_{GD} [1 + G_m (R_L // ESR)]$$

where

- $C_{GS}$  is the Gate-to-Source capacitance, which is found from the values (refer to FET data sheet for values of  $C_{ISS}$  and  $C_{RSS}$ ):

$$C_{GS} = C_{ISS} - C_{RSS}$$

where

- $C_{GD}$  is the Gate-to-Drain capacitance, which is equal to:

$$C_{GD} = C_{RSS}$$

where

- $G_m$  is the transconductance of the FET.

The FET data sheet specifies forward transconductance ( $G_{fs}$ ) at some value of drain current (defined as  $I_D$ ). To find  $G_m$  at the desired value of load current (defined as  $I_L$ ), use the formula:

$$G_m = G_{fs} \times (I_L / I_D)^{1/2}$$

where

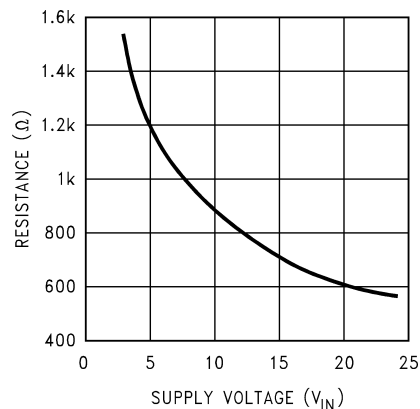
- $R_L$  is the load resistance.

ESR is the equivalent series resistance of the output capacitor.

- The term  $R_L // ESR$  is defined as:

$$(R_L \times ESR) / (R_L + ESR)$$

It can be seen from these equations that  $C_{EFF}$  varies with  $R_L$ . To get the worst-case (maximum) value for  $C_{EFF}$ , use the maximum value of load current, which also means the minimum value of load resistance  $R_L$ . It should be noted that in most cases, the ESR is the dominant term which determines the value of  $R_L // ESR$ .



**Figure 22. Gate Pin Output Impedance**

### Gate Capacitance Pole Frequency ( $f_{pg}$ )

The pole frequency resulting from the Gate capacitance  $C_{EFF}$  is defined as  $f_{pg}$  and can be approximated from:

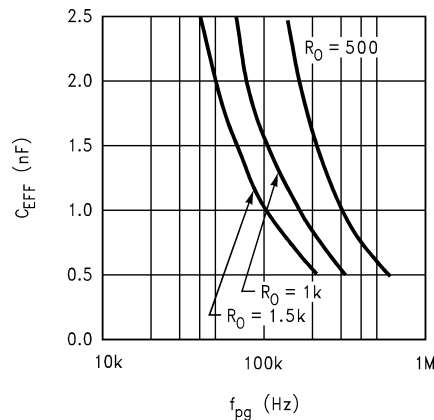
$$f_{pg} \approx 0.16 / (R_O \times C_{EFF})$$

where

- $R_O$  is the output impedance of the LP2975 Gate pin which drives the Gate of the FET.

It is important to note that  $R_O$  is a function of input supply voltage (see [Figure 22](#)). As shown, the minimum value of  $R_O$  is about  $550\Omega$  @  $V_{IN} = 24V$ , increasing to about  $1.55\text{ k}\Omega$  @  $V_{IN} = 3V$ .

Using the equation for  $f_{pg}$ , a family of curves are provided showing how  $f_{pg}$  varies with  $C_{EFF}$  for several values of  $R_O$  (see [Figure 23](#)).



**Figure 23.  $f_{pg}$  vs.  $C_{EFF}$**

As can be seen in the graph, values of  $C_{EFF}$  in the  $500\text{ pF}$ – $2500\text{ pF}$  range produce values for  $f_{pg}$  between  $40\text{ kHz}$  and  $700\text{ kHz}$ . To determine what effect  $f_{pg}$  will have on stability, the bandwidth of the regulator loop must be calculated (see next section, [Crossover Frequency and Phase Margin](#)).

### Crossover Frequency and Phase Margin

The term  $f_c$  will be used to define the crossover frequency of the regulator loop (which is the frequency where the gain curve crosses the  $0\text{ dB}$  axis). The importance of this frequency is that it is the point where the loop gain goes below unity, which marks the usable bandwidth of the regulator loop.

It is the **phase margin** (or lack of it) at  $f_c$  that determines whether the regulator is stable. Phase margin is defined as the total phase shift subtracted from  $180^\circ$ . In general, a stable loop requires at least  $20^\circ$ – $30^\circ$  of phase margin at  $f_c$ .

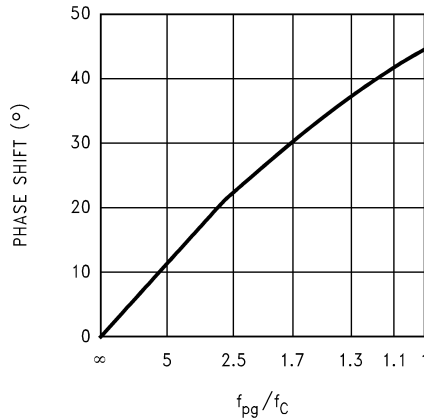
$f_c$  can be approximated by the following equation (all terms have been previously defined):

$$f_c \approx \frac{[3 \times 10^5 \times G_m \times (1.24/V_O)]^{1/2}}{[2 \times \pi \times C_{OUT}]^{1/2}}$$

This equation assumes that no  $C_F$  is used and  $f_{pg}/f_c > 1$ .

If the frequency of the Gate capacitance pole  $f_{pg}$  has been calculated (previous section), the amount of added phase shift may now be determined. As shown in the graph below (see [Figure 24](#), the amount of added phase shift increases as  $f_{pg}$  approaches  $f_c$ .

The amount of phase shift due to  $f_{pg}$  that can occur before oscillation takes place depends on how much added phase shift is present as a result of the  $C_{OUT}$  pole (see previous section, [Output Capacitor](#)).



**Figure 24. Phase Shift Due to  $f_{pg}$**

Because of this, there is no exact number for  $f_{pg}/f_c$  that can be given as a fixed limit for stable operation. However, as a general guideline, it is recommended that  $f_{pg} \geq 3 f_c$ .

If this is not found to be true after initial calculations, the ratio of  $f_{pg}/f_c$  can be increased by either reducing  $C_{EFF}$  (selecting a different FET) or using a larger value of  $C_{OUT}$ .

Along with these two methods, another technique for improving loop stability is the use of a feed-forward capacitor (see next section, [Feed-Forward Compensation](#)). This can improve phase margin by cancelling some of the excess phase shift.

### Feed-Forward Compensation

Phase shift in the loop gain of the regulator results from  $f_p$  (the pole from the output capacitor and load resistance),  $f_{pg}$  (the pole from the FET gate capacitance), as well as the IC's internal controller pole (see typical curve). If the total phase shift becomes excessive, instability can result.

The total phase shift can be reduced using feed-forward compensation, which places a zero in the loop to reduce the effects of the poles.

The feed-forward capacitor  $C_F$  can accomplish this, provided it is selected to set the zero at the correct frequency. It is important to point out that the feed-forward capacitor produces *both a zero and a pole*. The frequency where the zero occurs will be defined as  $f_{zf}$ , and the frequency of the pole will be defined as  $f_{pf}$ . The equations to calculate the frequencies are:

$$f_{zf} = 6.6 \times 10^{-6} / [C_F \times (V_{OUT}/1.24 - 1)]$$

$$f_{pf} = 6.6 \times 10^{-6} / [C_F \times (1 - 1.24/V_{OUT})]$$

In general, the feed-forward capacitor gives the greatest improvement in phase margin (provides the maximum reduction in phase shift) when the zero occurs at a frequency where the loop gain is  $>1$  (before the crossover frequency). The pole must occur at a higher frequency (the higher the better) where most of the phase shift added by the new pole occurs beyond the crossover frequency. For this reason, the pole-zero pair created by  $C_F$  become more effective at improving loop stability as they get farther apart in frequency.

In reviewing the equations for  $f_{zf}$  and  $f_{pf}$ , it can be seen that they get closer together in frequency as  $V_{OUT}$  decreases. For this reason, the use of  $C_F$  gives greatest benefit at higher output voltages, declining as  $V_{OUT}$  approaches 1.24V (where  $C_F$  has no effect at all).

In selecting a value of feed-forward capacitor, the crossover frequency  $f_c$  must first be calculated. In general, the frequency of the zero ( $f_{zf}$ ) set by this capacitor should be in the range:

$$0.2 f_c \leq f_{zf} \leq 1.0 f_c$$

The equation to determine the value of the feed-forward capacitor in fixed-voltage applications is:

$$C_F = 6.6 \times 10^{-6} / [f_{zf} \times (V_{OUT}/1.24 - 1)]$$

In adjustable applications (using an external resistive divider) the capacitor is found using:

$$C_C = 1/(2 \pi \times R1 \times f_{zf})$$

## Summary of Stability Information

This section will present an explanation of theory and terminology used to analyze loop stability, along with specific information related to stabilizing LP2975 applications.

### Bode Plots and Phase Shift

Loop gain information is most often presented in the form of a **Bode Plot**, which plots **Gain** (in dB) versus **Frequency** (in Hertz).

A Bode Plot also conveys phase shift information, which can be derived from the locations of the **poles** and **zeroes**.

**POLE:** A pole causes the slope of the gain curve to **decrease by an additional  $-20$  dB/decade**, and it also causes **phase lag** (defined as **negative phase shift**) to occur.

A single pole will cause a maximum  $-90^\circ$  of phase lag (see Figure 25). It should be noted that when the total phase shift at 0 dB reaches (or gets close to)  $-180^\circ$ , oscillations will result. Therefore, it can be seen that at least **two poles** in the gain curve are required to cause instability.

**ZERO:** A zero has an effect that is exactly *opposite to a pole*. A zero will add a maximum  $+90^\circ$  of **phase lead** (defined as **positive phase shift**). Also, a zero causes the slope of the gain curve to **increase** by an additional  $+20$  dB/decade (see Figure 26).

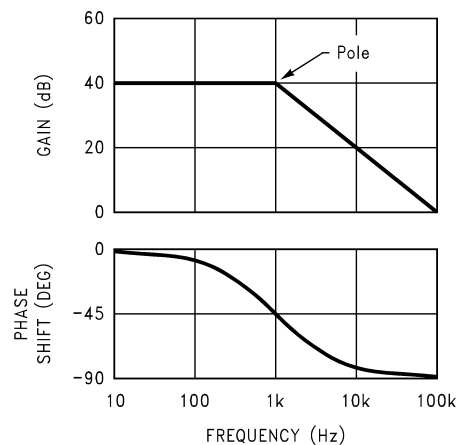


Figure 25. Effects of a Single Pole

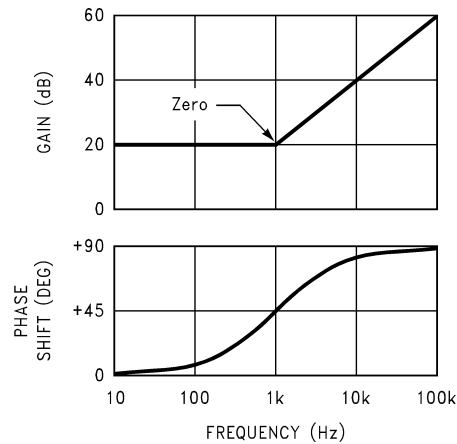
### Total phase shift

The actual test of whether or not a regulator is stable is the amount of phase shift that is present when the gain curve crosses the 0 dB axis (the frequency where this occurs was previously defined as  $f_c$ ).

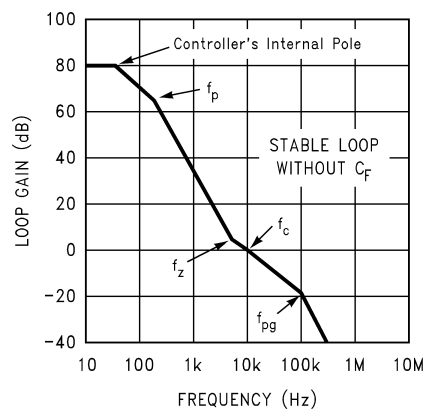
The phase shift at  $f_c$  can be estimated by looking at all of the poles and zeroes on the Bode plot and adding up the contributions of phase lag and lead from each one. As shown in the graphs, most of the phase lag (or lead) contributed by a pole (or zero) occurs within one decade of the frequency of the pole (or zero).

In general, a **phase margin** (defined as the difference between the total phase shift and  $-180^\circ$ ) of at least  $20^\circ$  to  $30^\circ$  is required for a stable loop.



**Figure 26. Effects of a Single Zero****Stability Analysis of Typical Applications**

The first application to be analyzed is a fixed-output voltage regulator with no feed-forward capacitor (see [Figure 27](#)).

**Figure 27. Stable Plot without Feed-Forward**

In this example, the value of  $C_{OUT}$  is selected so that the pole formed by  $C_{OUT}$  and  $R_L$  (previously defined as  $f_p$ ) is set at 200 Hz. The ESR of  $C_{OUT}$  is selected so that zero formed by the ESR and  $C_{OUT}$  (defined as  $f_z$ ) is set at 5 kHz (these selections follow the general guidelines stated previously in this document). Note that the gate capacitance is assumed to be moderate, with the pole formed by the  $C_{GATE}$  (defined as  $f_{pg}$ ) occurring at 100 kHz.

To estimate the total phase margin, the individual phase shift contributions of each pole and zero will be calculated assuming  $f_p = 200$  Hz,  $f_z = 5$  kHz,  $f_c = 10$  kHz and  $f_{pg} = 100$  kHz:

Controller pole shift =  $-90^\circ$

$f_p$  shift =  $-\arctan(10k/200) = -89^\circ$

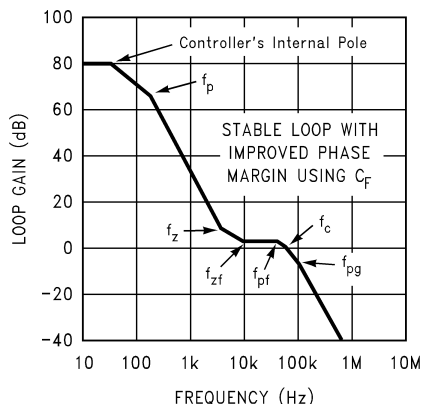
$f_z$  shift =  $\arctan(10k/5k) = +63^\circ$

$f_{pg}$  shift =  $-\arctan(10k/100k) = -6^\circ$

Summing the four numbers, the estimate for the **total phase shift is  $-122^\circ$** , which corresponds to a **phase margin of  $58^\circ$** . This application is stable, but could be improved by using a feed-forward capacitor (see next section).

**EFFECT OF FEED-FORWARD:** The example previously used will be continued with the addition of a feed-forward capacitor  $C_F$  (see [Figure 28](#)). The zero formed by  $C_F$  (previously defined as  $f_{zf}$ ) is set at 10 kHz and the pole formed by  $C_F$  (previously defined as  $f_{pf}$ ) is set at 40 kHz (the 4X ratio of  $f_{pf}/f_{zf}$  corresponds to  $V_{OUT} = 5V$ ).





**Figure 28. Improved Phase Margin with Feed-Forward**

To estimate the total phase margin, the individual phase shift contributions of each pole and zero will be calculated assuming  $f_p = 200$  Hz,  $f_z = 5$  kHz,  $f_{zf} = 10$  kHz,  $f_{pf} = 40$  kHz,  $f_c = 50$  kHz, and  $f_{pg} = 100$  kHz:

Controller pole shift =  $-90^\circ$

$f_p$  shift =  $-\arctan(50k/200) = -90^\circ$

$f_z$  shift =  $\arctan(50k/5k) = +84^\circ$

$f_{zf}$  shift =  $\arctan(50k/100k) = +79^\circ$

$f_{pf}$  shift =  $-\arctan(50k/40k) = -51^\circ$

$f_{pg}$  shift =  $-\arctan(50k/100k) = -27^\circ$

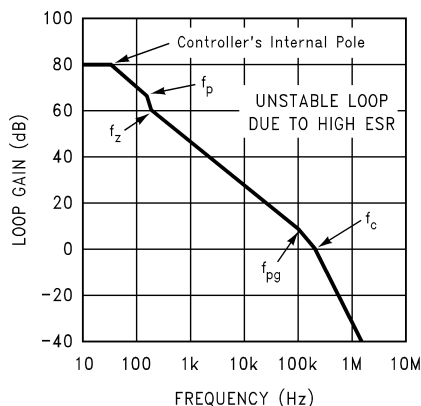
Summing the six numbers, the estimate for the **total phase shift is  $-95^\circ$** , which corresponds to a **phase margin of  $85^\circ$**  (a  $27^\circ$  improvement over the same application without the feed-forward capacitor).

For this reason, a feed-forward capacitor is recommended in all applications. Although not always required, the added phase margin typically gives faster settling times and provides some design guard band against  $C_{OUT}$  and ESR variations with temperature.

### Causes and Cures of Oscillations

The most common cause of oscillations in an LDO application is the output capacitor ESR. If the ESR is too high or too low, the zero ( $f_z$ ) does not provide enough phase lead.

**HIGH ESR:** To illustrate the effect of an output capacitor with high ESR, the previous example will be repeated except that the ESR will be **increased** by a factor of 20X. This will cause the frequency of the zero  $f_z$  to **decrease** by 20X, which moves it from 5 kHz down to 250 Hz (see Figure 29).

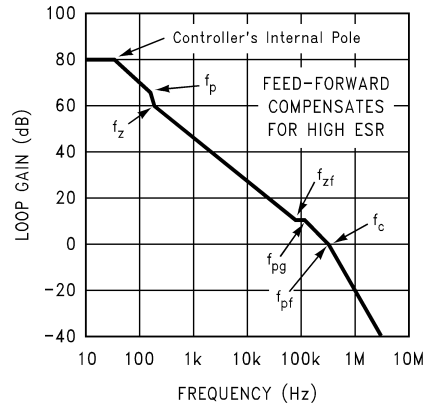


**Figure 29. High ESR Unstable without Feed-Forward**

As shown, moving the location of  $f_z$  lower in frequency extends the bandwidth, pushing the crossover frequency  $f_c$  out to about 200 kHz. In viewing the plot, it can be seen that  $f_p$  and  $f_z$  essentially cancel out, leaving only the controller pole and  $f_{pg}$ . However, since  $f_{pg}$  now occurs well before  $f_c$ , it will cause enough phase shift to leave very little phase margin. This application would either oscillate continuously or be marginally stable (meaning it would exhibit severe ringing on transient steps).

This can be improved by adding a feed-forward capacitor  $C_F$ , which adds a zero ( $f_{zf}$ ) and a pole ( $f_{pf}$ ) to the gain plot (see Figure 30).

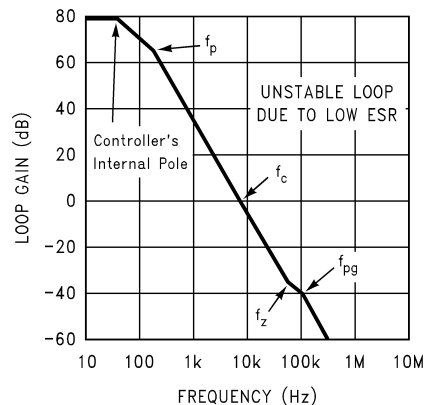
In this case,  $C_F$  is selected to place  $f_{zf}$  at about the same frequency as  $f_{pg}$  (essentially cancelling out the phase shift due to  $f_{pg}$ ). Assuming the added pole  $f_{pf}$  is near or beyond the  $f_c$  frequency, it will add  $< 45^\circ$  of phase lag, leaving a phase margin of  $> 45^\circ$  (adequate for good stability).



**Figure 30. High ESR Corrected with Feed-Forward**

**LOW ESR:** To illustrate how an output capacitor with low ESR can cause an LDO regulator to oscillate, the same example will be shown except that the ESR will be reduced sufficiently to increase the original  $f_z$  from 5 kHz to 50 kHz.

The plot now shows (see Figure 31) that the crossover frequency  $f_c$  has moved down to about 8 kHz. Since  $f_z$  is 6X  $f_c$ , it means that the zero  $f_z$  can only provide about  $9^\circ$  of phase lead at  $f_c$ , which is not sufficient for stability.



**Figure 31. Low ESR Unstable without Feed-Forward**

This application can also be improved by adding a feed-forward capacitor.  $C_F$  will add both a zero  $f_{zf}$  and pole  $f_{pf}$  to the gain plot (see Figure 32).

The crossover frequency  $f_c$  is now about 10 kHz. If  $C_F$  is selected so that  $f_{zf}$  is about 5 kHz, and  $f_{pf}$  is about 20 kHz (which means  $V_{OUT} = 5V$ ), the phase margin will be considerably improved. Calculating out all the poles and zeroes, the phase margin is increased from  $9^\circ$  to  $43^\circ$  (adequate for good stability).

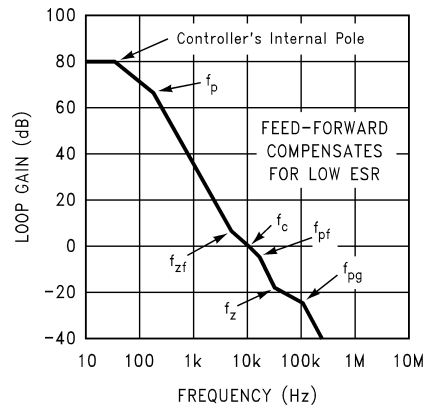


Figure 32. Low ESR Corrected with Feed-Forward

**EXCESSIVE GATE CAPACITANCE:** Higher values of gate capacitance shift the pole  $f_{pg}$  to lower frequencies, which can cause stability problems (see previous section [Gate Capacitance Pole Frequency \( \$f\_{pg}\$ \)](#)). As shown in [Figure 23](#), the pole  $f_{pg}$  will likely fall somewhere between 40 kHz and 500 kHz. How much phase shift this adds depends on the crossover frequency  $f_c$ .

The effect of gate capacitance becomes most important at high values of ESR for the output capacitor (see [Figure 29](#)). Higher values of ESR increase  $f_c$ , which brings  $f_{pg}$  more into the positive gain portion of the curve. As  $f_{pg}$  moves to a lower frequency (corresponding to higher values of gate capacitance), this effect becomes even worse.

This points out why FET's should be selected with the lowest possible gate capacitance: it makes the design more tolerant of higher ESR values on the output capacitor.

The use of a feed-forward capacitor  $C_F$  will help reduce excess phase shift due to  $f_{pg}$ , but its effectiveness depends on output voltage (see next section).

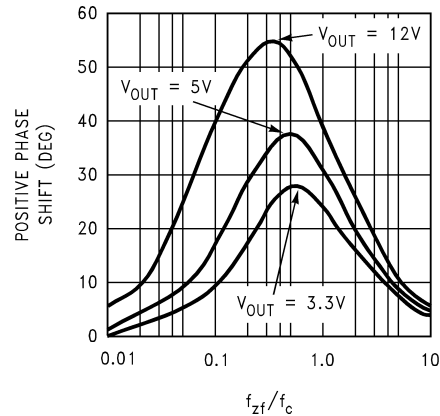
### LOW OUTPUT VOLTAGE AND $C_F$

The feed-forward capacitor  $C_F$  will provide a positive phase shift (lead) which can be used to cancel some of the excess phase lag from any of the various poles present in the loop. However, it is important to note that the effectiveness of  $C_F$  decreases with output voltage.

This is due to the fact that the frequencies of the zero  $f_{zf}$  and pole  $f_{pf}$  get closer together as the output voltage is reduced (see equations in [Feed-Forward Compensation](#)).

$C_F$  is more effective when the pole-zero pair are farther apart, because there is less self cancellation. The net benefit in phase shift provided by  $C_F$  is the **difference** between the lead (positive phase shift) from  $f_{zf}$  and the lag (negative phase shift) from  $f_{pf}$  which is present at the crossover frequency  $f_c$ . As the pole and zero frequency approach each other, that difference diminishes to nothing.

The amount of phase lead at  $f_c$  provided by  $C_F$  depends both on the  $f_{zf}/f_{pf}$  ratio and the location of  $f_z$  with respect to  $f_c$ . To illustrate this more clearly, a graph is provided which shows how much phase lead can be obtained for  $V_{OUT} = 12V, 5V, \text{ and } 3.3V$  (see [Figure 33](#)).



**Figure 33. Phase Lead Provided by  $C_F$**

The most important information on the graph is the frequency range of  $f_{zf}$  which will provide the maximum benefit (most positive phase shift):

For  $V_{OUT} = 12V$ :  $0.1 f_c < f_z < 1.0 f_c$

For  $V_{OUT} = 5V$ :  $0.2 f_c < f_z < 1.2 f_c$

For  $V_{OUT} = 3.3V$ :  $0.2 f_c < f_z < 1.3 f_c$

It's also important to note how the maximum available phase shift that  $C_F$  can provide drops off with  $V_{OUT}$ . At 12V, more than  $50^\circ$  can be obtained, but at 3.3V less than  $30^\circ$  is possible. The lesson from this is that higher voltage designs are more tolerant of phase shifts from both  $f_{pg}$  (the gate capacitance pole) and incorrect placement of  $f_z$  (which means the output capacitor ESR is not at its nominal value). At lower values of  $V_{OUT}$ , these parameters must be more precisely selected since  $C_F$  can not provide as much correction.

## GENERAL DESIGN PROCEDURE

Assuming that  $V_{IN}$ ,  $V_{OUT}$ , and  $R_L$  are defined:

1. Calculate the required value of capacitance for  $C_{OUT}$  so that the pole  $f_p \leq 200$  Hz (see previous section, [Output Capacitor](#)). For this calculation, an ESR of about  $0.1\Omega$  can be assumed for the purpose of determining  $C_{OUT}$ .

**IMPORTANT:** If a smaller value of output capacitor is used (so that the value of  $f_p > 200$  Hz), the phase margin of the control loop will be reduced. This will result in increased ringing on the output voltage during a load transient. If the output capacitor is made extremely small, oscillations will result.

To illustrate this effect, scope photos have been presented showing the output voltage of reference design #2 as the output capacitor is reduced to approximately 1/30 of the nominal value (the value which sets  $f_p = 200$  Hz). As shown, the effect of deviating from the nominal value is gradual and the regulator is quite robust in resisting going into oscillations.

2. Approximate the crossover frequency  $f_c$  using the equation in the previous section [Crossover Frequency and Phase Margin](#).
3. Calculate the required ESR of the output capacitor so that the frequency of the zero  $f_z$  is set to  $0.5 f_c$  (see previous section, [Output Capacitor](#)).
4. Calculate the value of the feed-forward capacitor  $C_F$  so that the zero  $f_{zf}$  occurs at the frequency which yields the maximum phase gain for the output voltage selected (see previous section, [LOW OUTPUT VOLTAGE AND  \$C\_F\$](#) ). The formula for calculating  $C_F$  is in the previous section, [Feed-Forward Capacitor](#).

Lower ESR electrolytics are available which use organic electrolyte (OSCON types), but are more costly than typical aluminum electrolytics.

If the calculated value of ESR is higher than what is found in the selected capacitor, an external resistor can be placed in series with  $C_{OUT}$ .

**LOW VOLTAGE DESIGNS:** Designs which have a low output voltage (where the positive effects of  $C_F$  are very small) may be marginally stable if the  $C_{OUT}$  and ESR values are not carefully selected.

Also, if the FET gate capacitance is large (as in the case of a high-current FET), the pole  $f_{pg}$  could possibly get low enough in frequency to cause a problem.

The solution in both cases is to increase the amount of output capacitance which will shift  $f_p$  to a lower frequency (and reduce overall loop bandwidth). The ESR and  $C_F$  calculations should be repeated, since this changes the crossover frequency  $f_c$ .

## REVISION HISTORY

### Changes from Revision E (April 2013) to Revision F

### Page

- Changed layout of National Data Sheet to TI format ..... [29](#)

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP2975AIMM-3.3/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L45A	<a href="#">Samples</a>
LP2975AIMM-5.0	ACTIVE	VSSOP	DGK	8	1000	TBD	Call TI	Call TI	-40 to 125	L46A	<a href="#">Samples</a>
LP2975AIMM-5.0/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L46A	<a href="#">Samples</a>
LP2975AIMMX-5.0	ACTIVE	VSSOP	DGK	8	3500	TBD	Call TI	Call TI	-40 to 125	L46A	<a href="#">Samples</a>
LP2975AIMMX-5.0/NOPB	ACTIVE	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L46A	<a href="#">Samples</a>
LP2975IMM-3.3/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L45B	<a href="#">Samples</a>
LP2975IMM-5.0/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L46B	<a href="#">Samples</a>
LP2975IMMX-5.0/NOPB	ACTIVE	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L46B	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

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(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP2975A1MM-3.3/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP2975A1MM-5.0	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP2975A1MM-5.0/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP2975A1MMX-5.0	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP2975A1MMX-5.0/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP29751MM-3.3/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP29751MM-5.0/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP29751MMX-5.0/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP2975AIMM-3.3/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LP2975AIMM-5.0	VSSOP	DGK	8	1000	210.0	185.0	35.0
LP2975AIMM-5.0/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LP2975AIMMX-5.0	VSSOP	DGK	8	3500	367.0	367.0	35.0
LP2975AIMMX-5.0/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LP2975IMM-3.3/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LP2975IMM-5.0/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LP2975IMMX-5.0/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0

DGK (S-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



## NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
- E. Falls within JEDEC MO-187 variation AA, except interlead flash.

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