

## DATA SHEET

# SKY12347-362LF: DC-3.0 GHz Six-Bit Digital Attenuator with Serial or Parallel Driver (0.5 dB LSB)

## Applications

- Cellular, 3G/4G, WiMAX, and LTE Infrastructures

## Features

- Broadband operation: DC to 3.0 GHz
- Attenuation: 31.5 dB with 0.5 dB LSB
- TTL/CMOS-compatible serial, parallel, or latched parallel control interface
- Single supply voltage: +3.3 or +5 V
- Small, QFN (24-pin, 4 x 4 mm) package (MSL1, 260 °C per JEDEC J-STD-020)

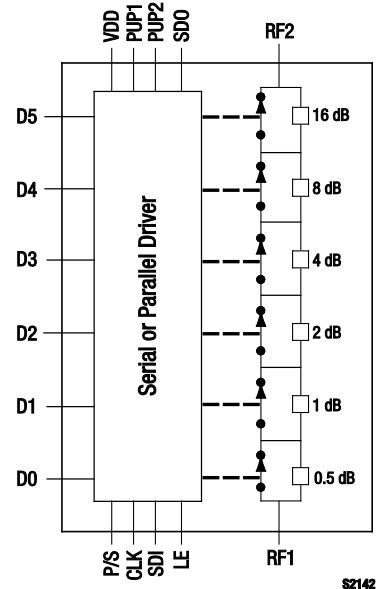


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## Description

The SKY12347-362LF is a GaAs pHEMT six-bit broadband digital attenuator with a 0.5 dB Least Significant Bit (LSB). A Transistor-to-Transistor Logic (TTL)/CMOS-compatible, dual-mode serial or parallel interface controller is integrated into the device.

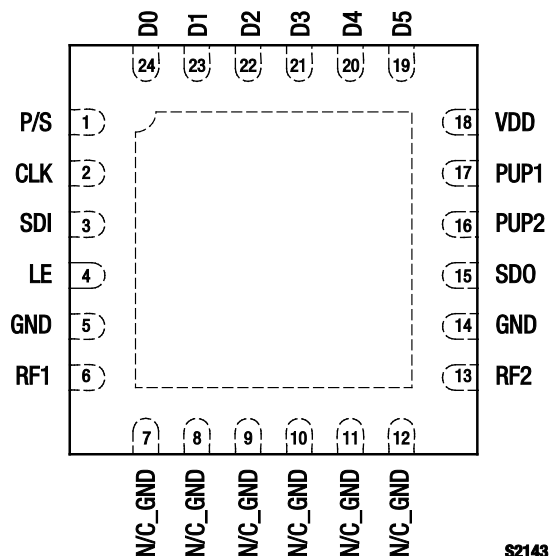
The attenuator features low insertion loss, excellent attenuation accuracy, a 31.5 dB attenuation range, and high linearity performance. The SKY12347-362LF is an ideal choice for a wide variety of cellular 3G and 4G infrastructure applications.



**Figure 1. SKY12347-362LF Block Diagram**

Attenuation is controlled by a Serial Peripheral Interface (SPI). Depending on the SPI sequence applied to the SDI pin, the attenuation state between the RF1 and RF2 pins can vary between a low insertion loss state or up to 31.5 dB. The D0 through D5 DC control pins determine the attenuation state if parallel mode is enabled.

The device is provided in a 4 x 4 mm, 24-pin Quad Flat No-Lead (QFN) package. A functional block diagram is shown in Figure 1. The pin configuration and package are shown in Figure 2. Signal pin assignments and functional pin descriptions are provided in Table 1.



**Figure 2. SKY12347-362LF Pinout – 24-Pin QFN  
(Top View)**

**Table 1. SKY12347-362LF Signal Descriptions**

Pin #	Name	Description	Pin #	Name	Description
1	P/S	Selects serial or parallel operation. Logic low enables parallel mode.	13	RF2	RF input/output to digital attenuator.
2	CLK	Serial clock input	14	GND	Ground
3	SDI	Serial data input	15	SD0	Serial data output
4	LE	On rising edge of pulse, shifts six most recent clocked-in bits to set attenuation state. In parallel mode, if latch enable is logic high, changes to pins 19 to 24 occur directly. If latch enable is logic low, the attenuator does not change states until the signal is raised.	16	PUP2	Sets device power-up attenuation state. See Table 7.
5	GND	Ground	17	PUP1	Sets device power-up attenuation state. See Table 7.
6	RF1	RF input/output to digital attenuator.	18	VDD	DC power supply
7	NC_GND	No connection. Can be grounded without affecting performance.	19	D5	TTL/CMOS DC control pin for parallel mode operation. D5 is MSB.
8	NC_GND	No connection. Can be grounded without affecting performance.	20	D4	TTL/CMOS DC control pin for parallel mode operation
9	NC_GND	No connection. Can be grounded without affecting performance.	21	D3	TTL/CMOS DC control pin for parallel mode operation
10	NC_GND	No connection. Can be grounded without affecting performance.	22	D2	TTL/CMOS DC control pin for parallel mode operation
11	NC_GND	No connection. Can be grounded without affecting performance.	23	D1	TTL/CMOS DC control pin for parallel mode operation
12	NC_GND	No connection. Can be grounded without affecting performance.	24	D0	TTL/CMOS DC control pin for parallel mode operation. D0 is LSB.

## Functional Description

The SKY12347-362LF is a six bit digital attenuator comprised of a GaAs attenuator and a silicon CMOS driver. The attenuation setting is controlled by an SPI. Attenuation is set by a stream of data that is clocked into the shift registers of the silicon chip by the clock signal. To set the attenuation state, a latch signal is sent to the appropriate pin to send the correct bias voltages to the GaAs attenuator.

More than one attenuator can be cascaded together and the data may be passed through one device to the other using the SDO signal (pin 15). The DC bias voltage to the silicon CMOS chip is applied to pin 18 (VDD).

## Power-Up/Power-Down Timing

Serial input data (SDI pin) is shifted into the register on the rising edge of the clock (CLK pin), Least Significant Bit (LSB) first. The attenuator changes states on the rising edge of the latch enable (LE pin) signal, according to the most recent six bits of shifted data accepted since the previous falling edge of the latch enable signal. The serial data output is the serial input data delayed by six clock cycles.

Refer to the timing diagram in Figure 3 and timing parameter specifications in Table 2. Table 3 shows the transition states based on the LE and CLK signals.

Power-up sequence is as follows:

0. Connect ground
1. Apply V<sub>DD</sub>
2. Set all inputs (CLK, SDI, LE)

The power-down sequence is the reverse of above.

Figure 4 shows an example of how to set the attenuator to the 0.5 dB state. The progression of the bit states vs the clock signal is shown. The timing diagram shows that when the latch enable signal goes high, the voltages D0 to D5 set the attenuator to the 0.5 dB state.

## Electrical and Mechanical Specifications

The absolute maximum ratings of the SKY12347-362LF are provided in Table 4. Electrical specifications are provided in Tables 5 and 6.

Typical performance characteristics of the SKY12347-362LF are illustrated in Figures 5 through 11.

The state of the SKY12347-362LF is determined by the logic provided in Table 7.

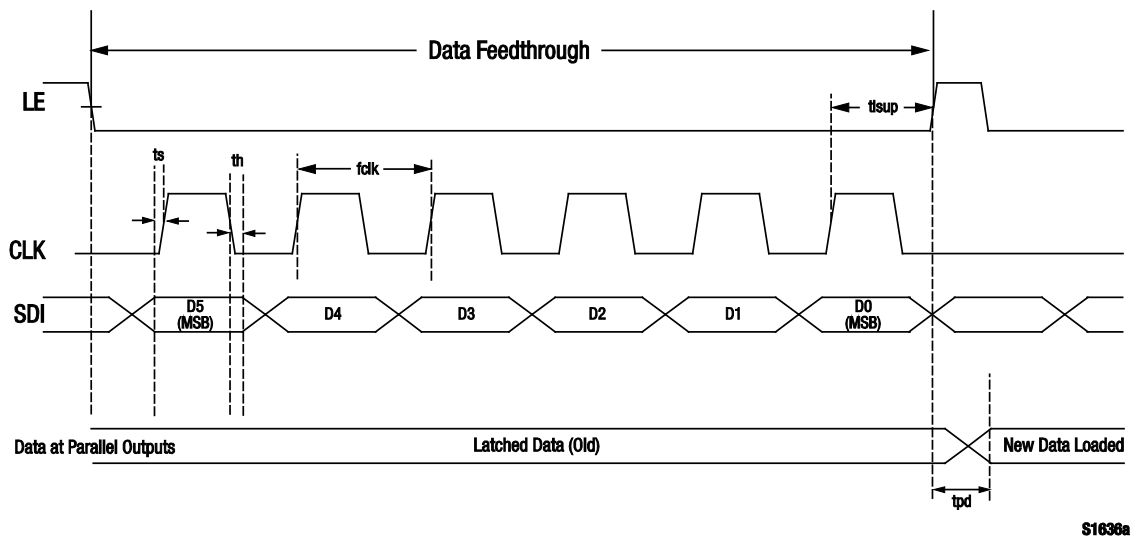


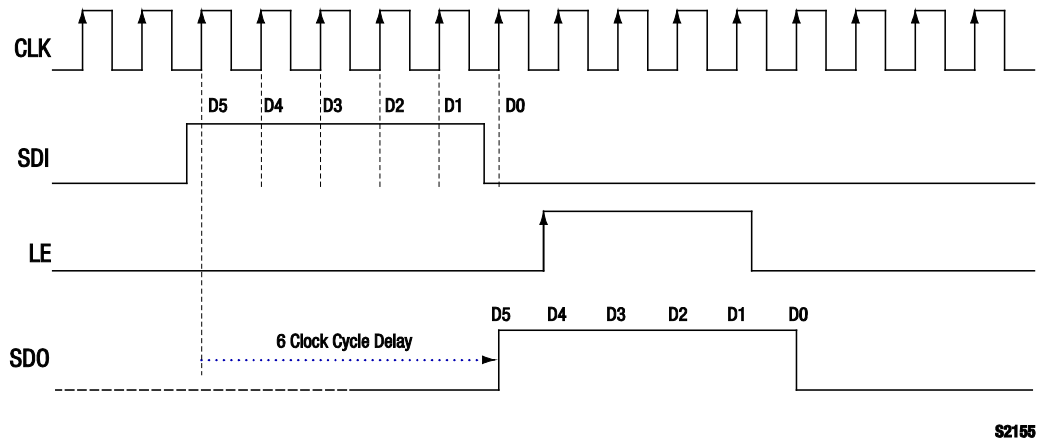
Figure 3. Power-Up/Power-Down Timing

Table 2. Power-Up/Power-Down Timing Parameters

Parameter	Symbol	VDD = 5 V			VDD = 3.3 V			Units
		Minimum	Typical	Maximum	Minimum	Typical	Maximum	
Serial input setup time	ts		5			5		ns
Hold time from serial input to shift clock	th		5			5		ns
Setup time from shift clock to latch enable	tlsup	40			100			ns
Propagation delay, latch enable to C0.5 through C8	tpd			30			70	ns
Setup time from reset to shift clock	—	20			50			ns
Clock frequency	fCLK			30			10	MHz

Table 3. Transition State Logic

LE (Pin 4)	CLK (Pin 2)	Function
X	→	Shift register clocked
→	X	Contents of shift register transferred to digital attenuator



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Figure 4. Example for Setting 0.5 dB State

**Table 4. SKY12347-362LF Absolute Maximum Ratings**

Parameter	Symbol	Minimum	Maximum	Units
Supply voltage	V <sub>DD</sub>	3.3	6.0	V
Control voltage	V <sub>CTL</sub>	0	V <sub>DD</sub>	V
RF input power	P <sub>IN</sub>		+30	dBm
Operating temperature	T <sub>OP</sub>	−40	+85	°C
Storage temperature	T <sub>STG</sub>	−40	+125	°C

**Note:** Exposure to maximum rating conditions for extended periods may reduce device reliability. There is no damage to device with only one parameter set at the limit and all other parameters set at or below their nominal value. Exceeding any of the limits listed here may result in permanent damage to the device.

**CAUTION:** Although this device is designed to be as robust as possible, Electrostatic Discharge (ESD) can damage this device. This device must be protected at all times from ESD. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD precautions should be used at all times.

**Table 5. SKY12347-362LF Electrical Specifications (Note 1) (1 of 2)**

(V<sub>DD</sub> = 5 V, V<sub>CTL</sub> = 5 V, T<sub>OP</sub> = +25 °C, P<sub>IN</sub> = 0 dBm, Characteristic Impedance [Z<sub>0</sub>] = 50 Ω, , Unless Otherwise Noted)

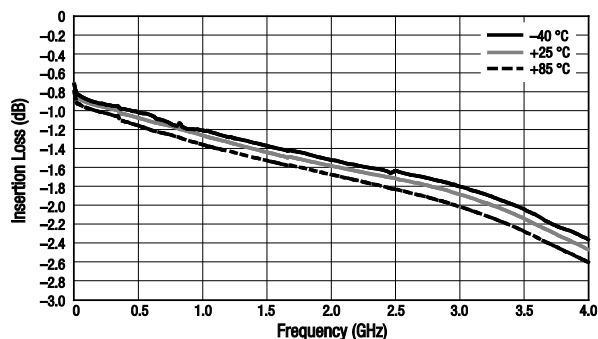
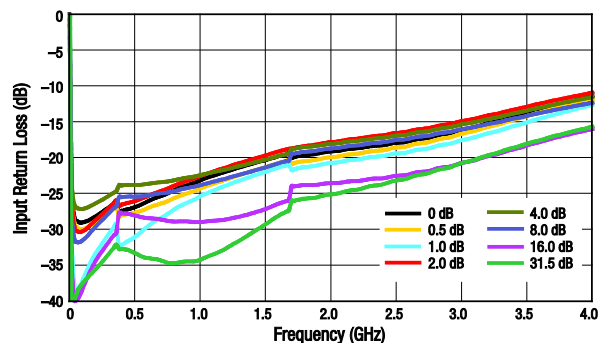
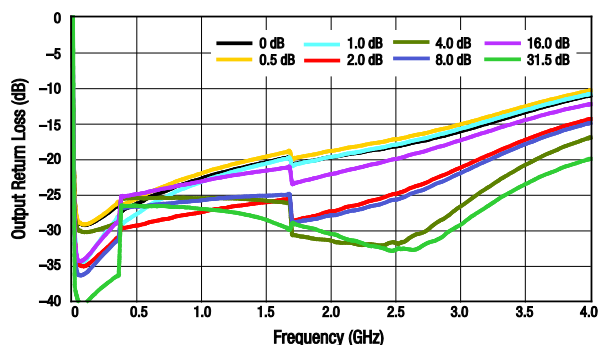
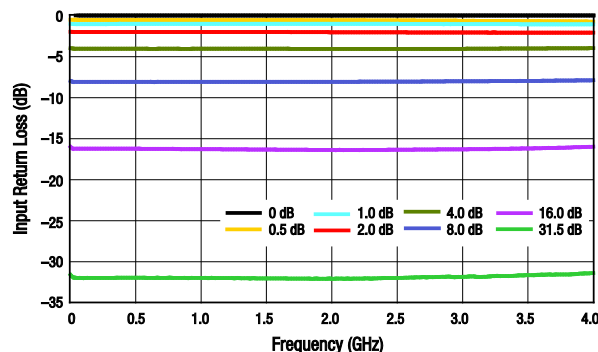
Parameter	Symbol	Test Condition	Min	Typical	Max	Units
<b>RF Specifications</b>						
Insertion loss	IL	DC to 0.8 GHz 0.8 to 3.0 GHz		1.2 2.0	1.3 2.2	dB dB
Attenuation range		DC to 3.0 GHz	0.5		31.5	dB
Return loss	RL	DC to 3.0 GHz		15		dB
Attenuation accuracy		All attenuation states DC to 0.8 GHz 0.8 to 3.0 GHz	±(0.1 + 5% of attenuation setting max) ±(0.3 + 3% of attenuation setting max)			dB dB
0.1 dB Input Compression Point	IP0.1dB	DC to 3.0 GHz		+30		dBm
3 <sup>rd</sup> Order Input Intercept Point	IIP3	DC to 3.0 GHz, P <sub>IN</sub> = +10 dBm/tone, ΔF = 1 MHz		+50		dBm
<b>DC Specifications</b>						
Control voltage: Low High	V <sub>CTL</sub>		0 3.0		0.8 V <sub>DD</sub>	V V
Supply voltage	V <sub>DD</sub>		3.3	5.0	5.5	V
Supply current	I <sub>DD</sub>			100		μA

**Table 5. SKY12347-362LF Electrical Specifications (Note 1) (2 of 2)****( $V_{DD} = 5\text{ V}$ ,  $V_{CTL} = 5\text{ V}$ ,  $T_{OP} = +25\text{ }^{\circ}\text{C}$ ,  $P_{IN} = 0\text{ dBm}$ , Characteristic Impedance [ $Z_0$ ] =  $50\text{ }\Omega$ , , Unless Otherwise Noted)**

Parameter	Symbol	Test Condition	Min	Typical	Max	Units
<b>Switching Speed Specifications</b>						
50% control to 90% attenuation		$V_{DD} = 3.3\text{ V}$ , Bit = 3.3 V		91		ns
		$V_{DD} = 5.0\text{ V}$ , Bit = 3.3 V		48		ns
		$V_{DD} = 5.0\text{ V}$ , Bit = 5.0 V		47		ns
50% control to 10% attenuation		$V_{DD} = 3.3\text{ V}$ , Bit = 3.3 V		19		ns
		$V_{DD} = 5.0\text{ V}$ , Bit = 3.3 V		28		ns
		$V_{DD} = 5.0\text{ V}$ , Bit = 5.0 V		28		ns
10% to 90% attenuation		$V_{DD} = 3.3\text{ V}$ , Bit = 3.3 V		47		ns
		$V_{DD} = 5.0\text{ V}$ , Bit = 3.3 V		24		ns
		$V_{DD} = 5.0\text{ V}$ , Bit = 5.0 V		26		ns
90% to 10% attenuation		$V_{DD} = 3.3\text{ V}$ , Bit = 3.3 V		35		ns
		$V_{DD} = 5.0\text{ V}$ , Bit = 3.3 V		18		ns
		$V_{DD} = 5.0\text{ V}$ , Bit = 5.0 V		18		ns

**Note 1:** Performance is guaranteed only under the conditions listed in this Table.

## Typical Performance Characteristics

**( $V_{DD} = 5\text{ V}$ ,  $V_{CTL} = 5\text{ V}$ ,  $T_{OP} = +25\text{ }^{\circ}\text{C}$ ,  $P_{IN} = 0\text{ dBm}$ , Characteristic Impedance [ $Z_0$ ] =  $50\text{ }\Omega$ , , Unless Otherwise Noted)****Figure 5. Insertion Loss vs Frequency****Figure 6. Input Return Loss vs Frequency****Figure 7. Output Return Loss vs Frequency****Figure 8. Normalized Attenuation vs Frequency**

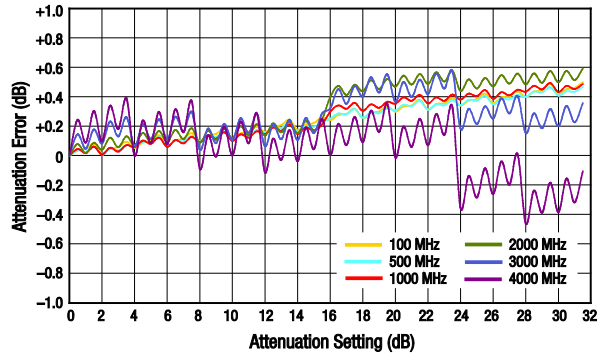


Figure 9. Attenuation Error vs Attenuation Setting

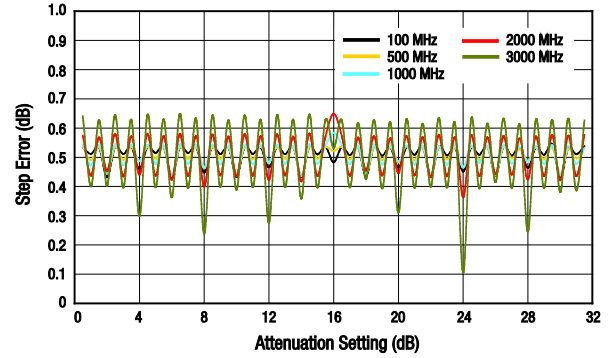


Figure 10. Step Error vs Attenuation Setting

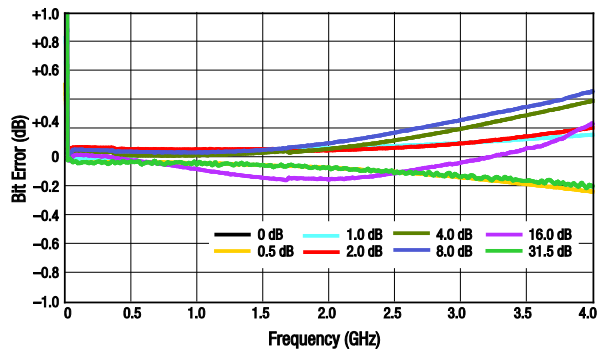


Figure 11. Major State Bit Error vs Frequency

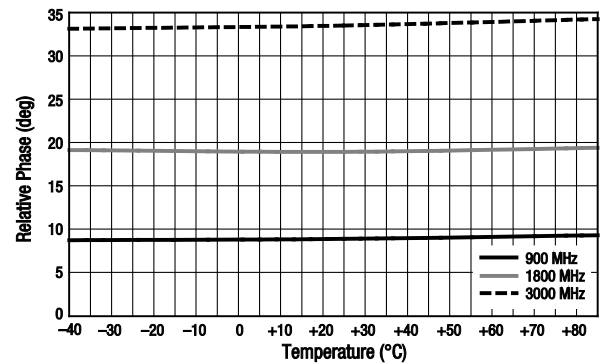


Figure 12. 31.5 dB State Relative Phase vs Temperature

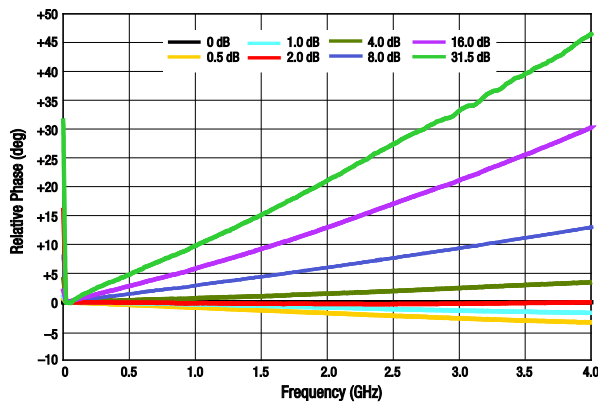


Figure 13. Relative Phase vs Frequency

**Table 6. SKY12347-362LF Parallel Mode Truth Table**

RF1/RF2 (Pins 6 & 13) Attenuation	D5 (Pin 19)	D4 (Pin 20)	D3 (Pin 21)	D2 (Pin 22)	D1 (Pin 23)	D0 (Pin 24)
Insertion loss	1	1	1	1	1	1
0.5 dB	1	1	1	1	1	0
1.0 dB	1	1	1	1	0	1
2.0 dB	1	1	1	0	1	1
4.0 dB	1	1	0	1	1	1
8.0 dB	1	0	1	1	1	1
16 dB	0	1	1	1	1	1
31.5 dB	0	0	0	0	0	0

**Note:** “1” = high control voltage: +3.0 to V<sub>DD</sub>.  
“0” = low control voltage: 0 to +0.8 V.

**Table 7. SKY12347-362LF Power-Up Truth Table**

Initial Attenuation State	LE (Pin 4)	PUP1 (Pin 17)	PUP2 (Pin 16)
31.5 dB	0	0	0
24.0 dB	0	1	0
16.0 dB	0	0	1
Insertion Loss	0	1	1
State is determined by signal logic at pins D0 to D5. See Table 6.	1	X	X

**Note:** “1” = Logic high  
“0” = Logic low  
“X” = don't care

## Evaluation Board Description

The SKY12347-362LF Evaluation Board is used to test the performance of the SKY12347-362LF digital attenuator. An assembly drawing for the Evaluation Board is shown in Figure 14 and an Evaluation Board schematic diagram is shown in Figure 15.

## Package Dimensions

The PCB layout footprint for the SKY12347-362LF is shown in Figure 16. Typical case markings are noted in Figure 17. Package dimensions for the 24-pin QFN are shown in Figure 18, and tape and reel dimensions are provided in Figure 19.

## Package and Handling Information

Instructions on the shipping container label regarding exposure to moisture after the container seal is broken must be followed. Otherwise, problems related to moisture absorption may occur when the part is subjected to high temperature during solder assembly.

THE SKY12347-362LF is rated to Moisture Sensitivity Level 1 (MSL1) at 260 °C. It can be used for lead or lead-free soldering. For additional information, refer to the Skyworks Application Note, *Solder Reflow Information*, document number 200164.

Care must be taken when attaching this product, whether it is done manually or in a production solder reflow environment. Production quantities of this product are shipped in a standard tape and reel format.



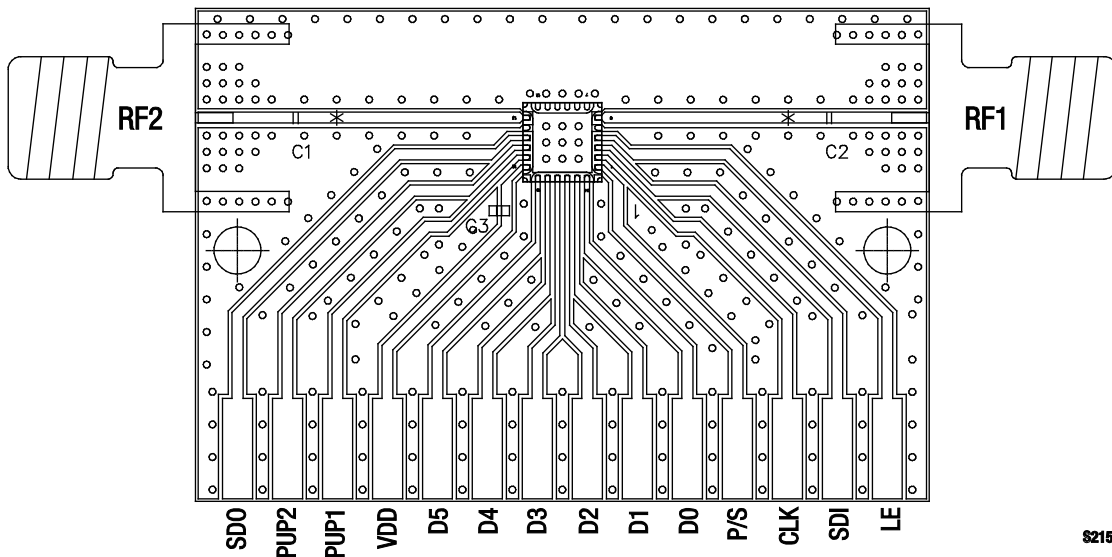


Figure 14. SKY12347-362LF Evaluation Board Assembly Diagram

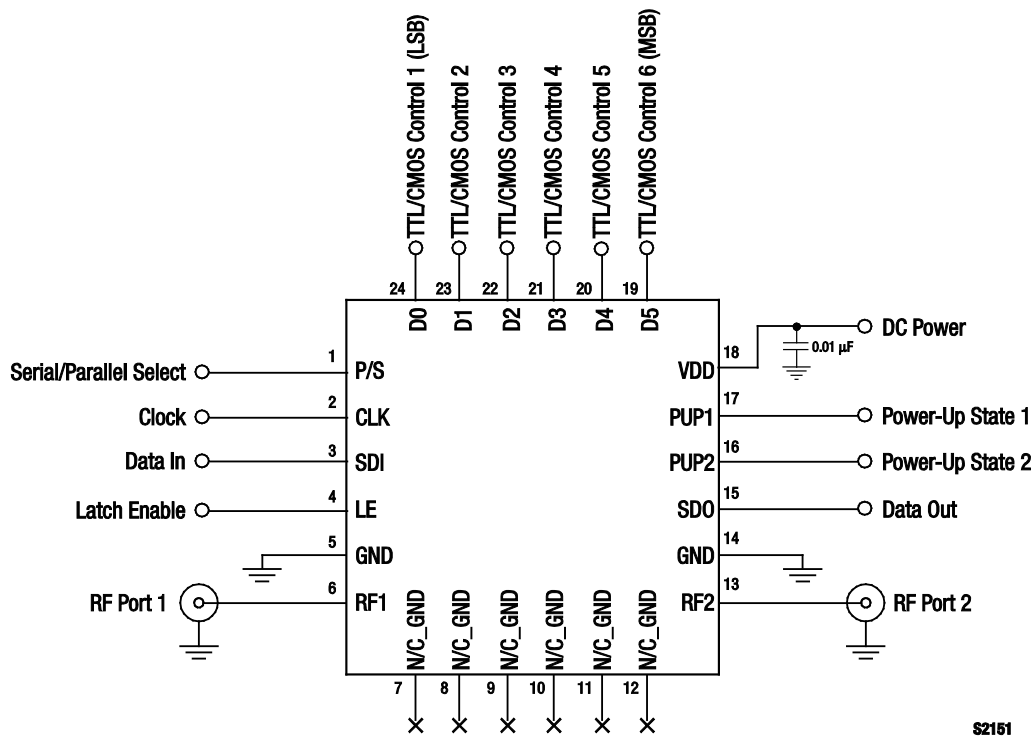
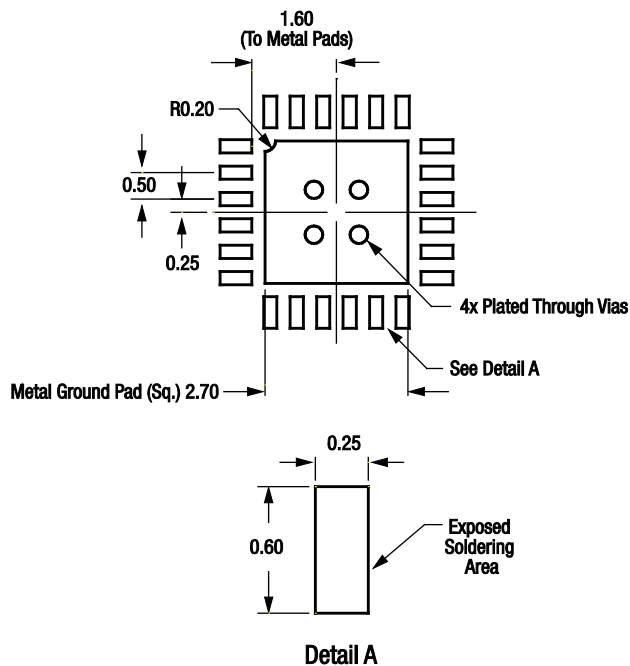


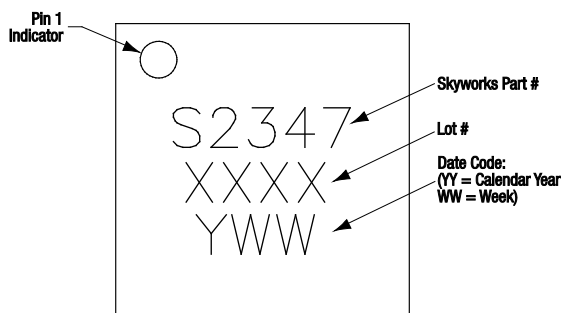
Figure 15. SKY12347-362LF Evaluation Board Schematic Diagram



All dimensions are in millimeters

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**Figure 16. SKY12347-362LF PCB Layout Footprint**



**Figure 17. Typical Part Markings**

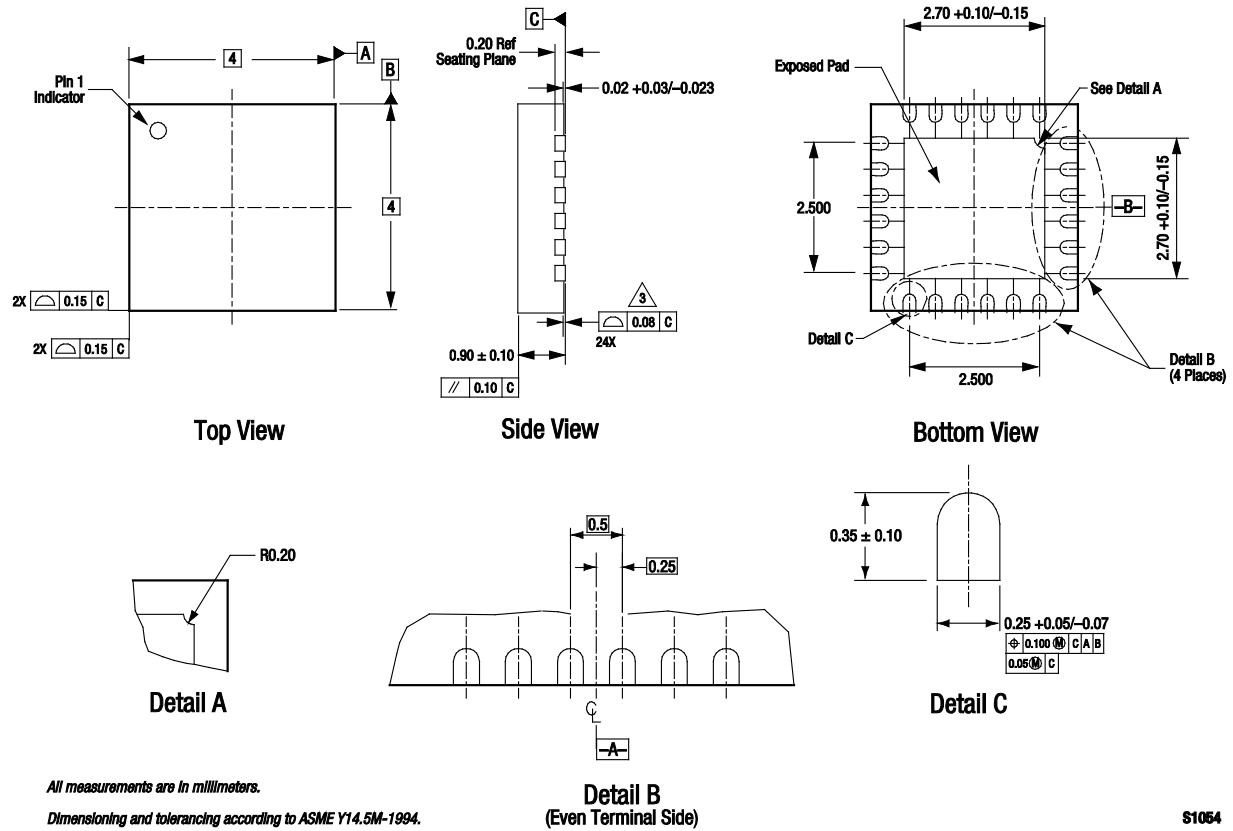
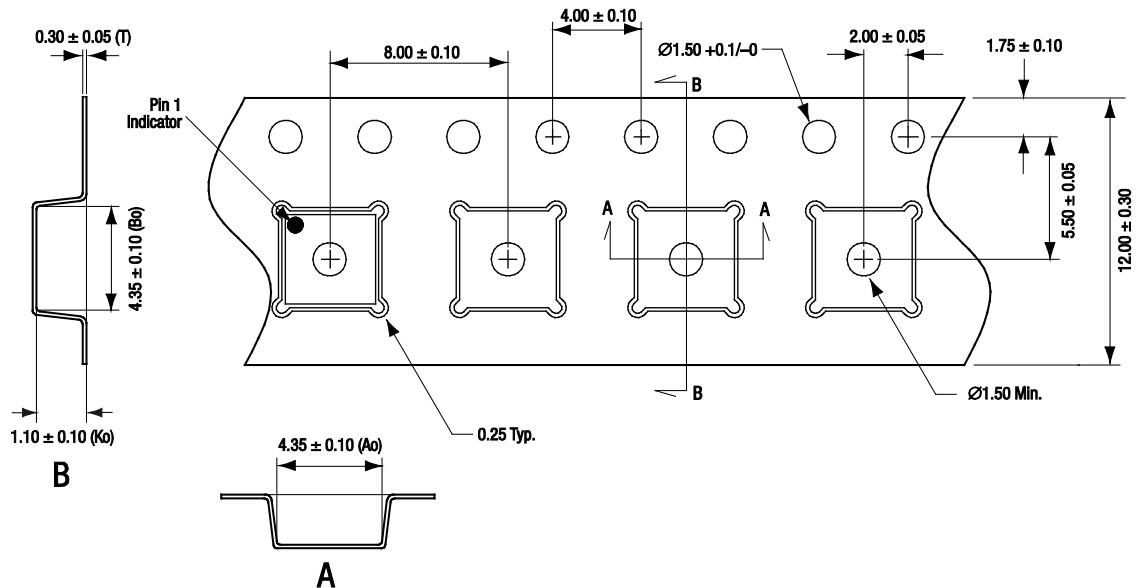


Figure 18. SKY12347-362LF 24-Pin QFN Package Dimensions



- Notes:**
1. Carrier tape material: black conductive polystyrene, non-bakeable
  2. Cover tape material: transparent conductive HSA
  3. Cover tape size: 9.2 mm width
  4. All measurements are in millimeters

Figure 19. SKY12347-362LF Tape and Reel Dimensions

## Ordering Information

Model Name	Manufacturing Part Number	Evaluation Board Part Numbers
SKY12347-362LF Digital Attenuator	SKY12347-362LF	SKY12347-362LF-EVB

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