

- **EPIC™ (Enhanced-Performance Implanted CMOS) Process**
- **Typical V_{OLP} (Output Ground Bounce)**
 < 0.8 V at V_{CC} , $T_A = 25^\circ\text{C}$
- **Typical V_{OHV} (Output V_{OH} Undershoot)**
 > 2 V at V_{CC} , $T_A = 25^\circ\text{C}$
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)**
- **Package Options Include Plastic Small-Outline (D, NS), Shrink Small-Outline (DB), Thin Very Small-Outline (DGV), and Thin Shrink Small-Outline (PW) Packages, Ceramic Flat (W) Packages, Chip Carriers (FK), and DIPs (J)**

description

The 'LV164A devices are 8-bit parallel-out serial shift registers designed for 2-V to 5.5-V V_{CC} operation.

These devices feature AND-gated serial (A and B) inputs and an asynchronous clear (CLR) input. The gated serial inputs permit complete control over incoming data as a low at either input inhibits entry of the new data and resets the first flip-flop to the low level at the next clock pulse. A high-level input enables the other input, which then determines the state of the first flip-flop. Data at the serial inputs can be changed while the clock is high or low, provided the minimum setup time requirements are met. Clocking occurs on the low-to-high-level transition of the clock (CLK) input.

The SN54LV164A is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LV164A is characterized for operation from -40°C to 85°C .

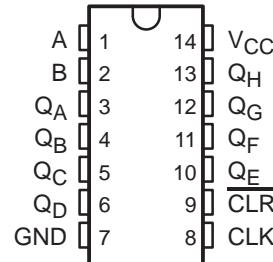
FUNCTION TABLE

INPUTS				OUTPUTS		
CLR	CLK	A	B	Q_A	$Q_B \dots Q_H$	
L	X	X	X	L	L	L
H	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	↑	H	H	H	Q_{An}	Q_{Gn}
H	↑	L	X	L	Q_{An}	Q_{Gn}
H	↑	X	L	L	Q_{An}	Q_{Gn}

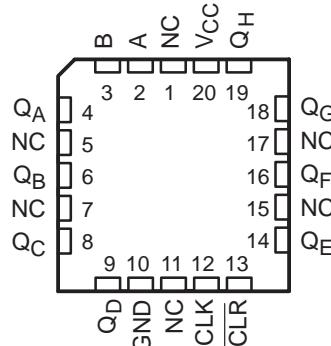
Q_{A0} , Q_{B0} , Q_{H0} = the level of Q_A , Q_B , or Q_H , respectively, before the indicated steady-state inputs conditions were established

Q_{An} , Q_{Gn} = the level of Q_A or Q_G before the most recent ↑ transition of the clock: indicates a 1-bit shift

SN54LV164A . . . J OR W PACKAGE
SN74LV164A . . . D, DB, DGV, NS, OR PW PACKAGE
(TOP VIEW)



SN54LV164A . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection



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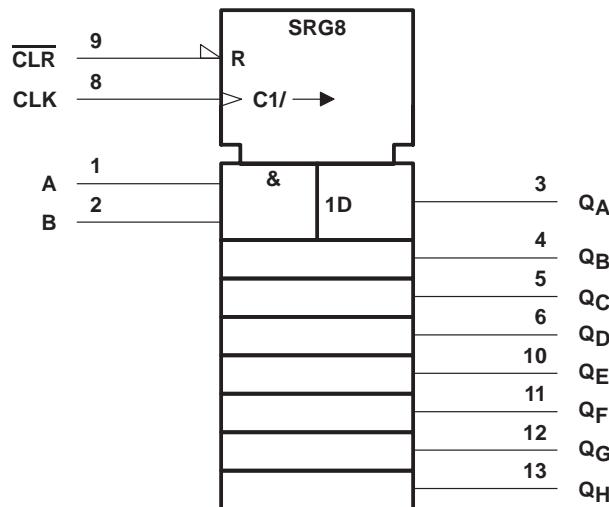
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SN54LV164A, SN74LV164A 8-BIT PARALLEL-OUT SERIAL SHIFT REGISTERS

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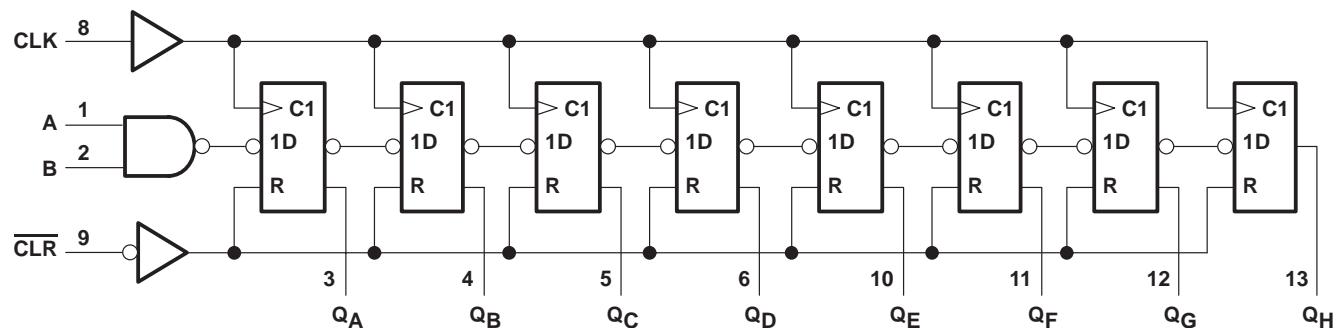
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

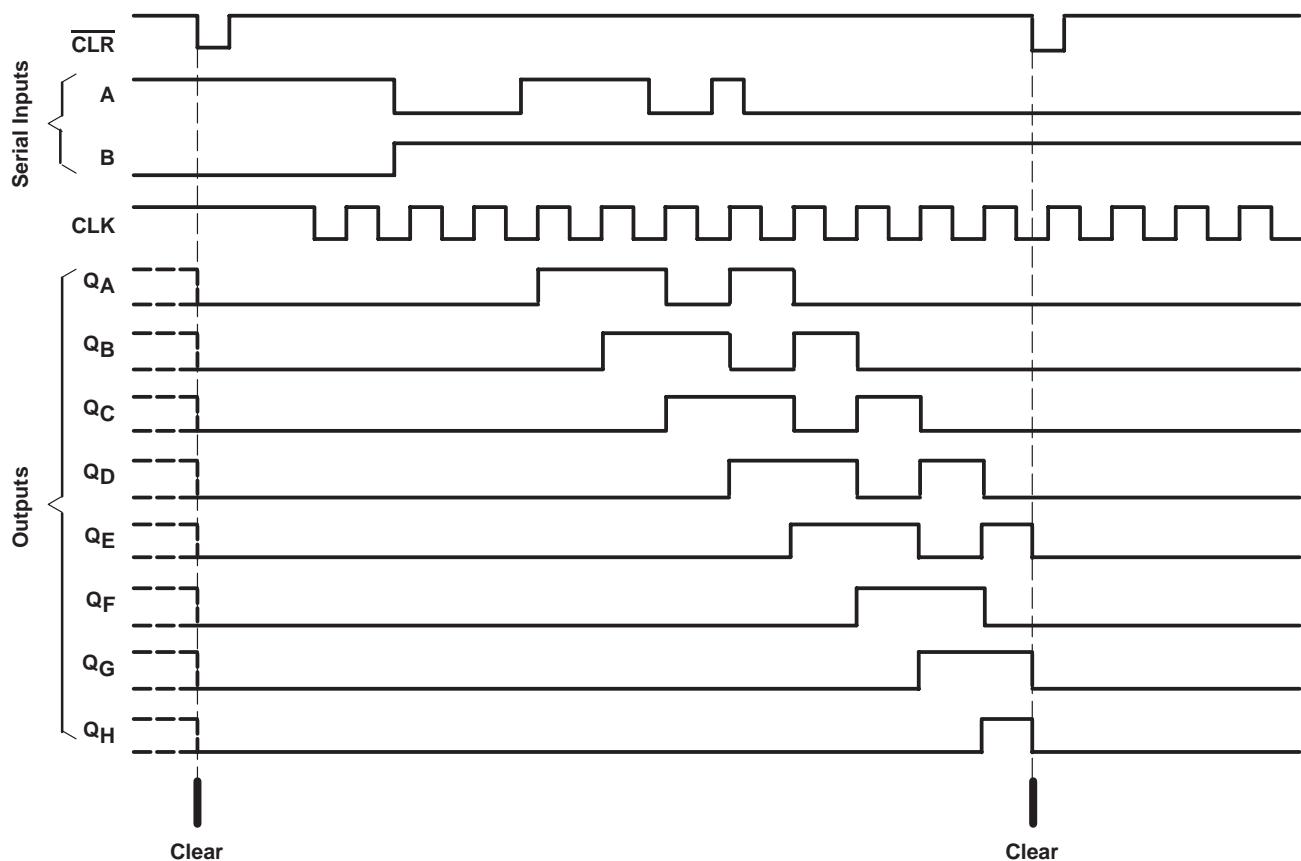
Pin numbers shown are for the D, DB, DGV, J, NS, PW, and W packages.

logic diagram (positive logic)



Pin numbers shown are for the D, DB, DGV, J, NS, PW, and W packages.

typical clear, shift, and clear sequences



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input voltage range, V_I (see Note 1)	-0.5 V to 7 V
Output voltage range, V_O (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	-20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 25 mA
Continuous current through V_{CC} or GND	± 50 mA
Package thermal impedance, θ_{JA} (see Note 3): D package	127°C/W
DB package	158°C/W
DGV package	182°C/W
NS package	127°C/W
PW package	170°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. This value is limited to 7 V maximum.
 3. The package thermal impedance is calculated in accordance with JESD 51.

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recommended operating conditions (see Note 4)

			SN54LV164A		SN74LV164A		UNIT	
			MIN	MAX	MIN	MAX		
V _{CC}	Supply voltage			2	5.5	2	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 2 V	1.5		1.5		V	
		V _{CC} = 2.3 V to 2.7 V	V _{CC} × 0.7		V _{CC} × 0.7			
		V _{CC} = 3 V to 3.6 V	V _{CC} × 0.7		V _{CC} × 0.7			
		V _{CC} = 4.5 V to 5.5 V	V _{CC} × 0.7		V _{CC} × 0.7			
V _{IL}	Low-level input voltage	V _{CC} = 2 V		0.5		0.5	V	
		V _{CC} = 2.3 V to 2.7 V		V _{CC} × 0.3		V _{CC} × 0.3		
		V _{CC} = 3 V to 3.6 V		V _{CC} × 0.3		V _{CC} × 0.3		
		V _{CC} = 4.5 V to 5.5 V		V _{CC} × 0.3		V _{CC} × 0.3		
V _I	Input voltage			0	5.5	0	5.5	V
V _O	Output voltage			0	V _{CC}	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 2 V		-50		-50	μA	
		V _{CC} = 2.3 V to 2.7 V		-2		-2	mA	
		V _{CC} = 3 V to 3.6 V		-6		-6		
		V _{CC} = 4.5 V to 5.5 V		-12		-12		
I _{OL}	Low-level output current	V _{CC} = 2 V		50		50	μA	
		V _{CC} = 2.3 V to 2.7 V		2		2	mA	
		V _{CC} = 3 V to 3.6 V		6		6		
		V _{CC} = 4.5 V to 5.5 V		12		12		
Δt/Δv	Input transition rise or fall rate	V _{CC} = 2.3 V to 2.7 V		0	200	0	200	ns/V
		V _{CC} = 3 V to 3.6 V		0	100	0	100	
		V _{CC} = 4.5 V to 5.5 V		0	20	0	20	
T _A	Operating free-air temperature			-55	125	-40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	SN54LV164A			SN74LV164A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V _{OH}	I _{OH} = -50 μA	2 V to 5.5 V	V _{CC} - 0.1			V _{CC} - 0.1			V
	I _{OH} = -2 mA	2.3 V	2			2			
	I _{OH} = -6 mA	3 V	2.48			2.48			
	I _{OH} = -12 mA	4.5 V	3.8			3.8			
V _{OL}	I _{OL} = 50 μA	2 V to 5.5 V		0.1		0.1			V
	I _{OL} = 2 mA	2.3 V		0.4		0.4			
	I _{OL} = 6 mA	3 V		0.44		0.44			
	I _{OL} = 12 mA	4.5 V		0.55		0.55			
I _I	V _I = V _{CC} or GND	5.5 V		±1		±1			μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V		20		20			μA
I _{off}	V _I or V _O = 0 to 5.5 V	0 V		5		5			μA
C _i	V _I = V _{CC} or GND	3.3 V		2.2		2.2			pF

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timing requirements over recommended operating free-air temperature range, $V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$ (unless otherwise noted) (see Figure 1)

		$T_A = 25^\circ\text{C}$		SN54LV164A		SN74LV164A		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_W	Pulse duration	CLR low	6	6.5		6.5		ns
		CLK high or low	6.5	7.5		7.5		
t_{SU}	Setup time	Data before CLK↑	6.5	8.5		8.5		ns
		CLR inactive	3	3		3		
t_H	Hold time	Data after CLK↑	-0.5	0		0		ns

timing requirements over recommended operating free-air temperature range, $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ (unless otherwise noted) (see Figure 1)

		$T_A = 25^\circ\text{C}$		SN54LV164A		SN74LV164A		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_W	Pulse duration	CLR low	5	5		5		ns
		CLK high or low	5	5		5		
t_{SU}	Setup time	Data before CLK↑	5	6		6		ns
		CLR inactive	2.5	2.5		2.5		
t_H	Hold time	Data after CLK↑	0	0		0		ns

timing requirements over recommended operating free-air temperature range, $V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$ (unless otherwise noted) (see Figure 1)

		$T_A = 25^\circ\text{C}$		SN54LV164A		SN74LV164A		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_W	Pulse duration	CLR low	5	5		5		ns
		CLK high or low	5	5		5		
t_{SU}	Setup time	Data before CLK↑	4.5	4.5		4.5		ns
		CLR inactive	2.5	2.5		2.5		
t_H	Hold time	Data after CLK↑	1	1		1		ns

switching characteristics over recommended operating free-air temperature range, $V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV164A	SN74LV164A	UNIT
				MIN	TYP	MAX			
f_{max}			$C_L = 15 \text{ pF}^*$	55	105		50	50	MHz
				45	85		40	40	
t_{pd}^*	CLK	Q	$C_L = 15 \text{ pF}$	9.2	17.6		1	20	ns
				8.6	16		1	18	
t_{pd}	CLK	Q	$C_L = 50 \text{ pF}$	11.5	21.1		1	24	ns
				10.8	19.5		1	22	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

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**switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV164A	SN74LV164A	UNIT
				MIN	TYP	MAX	MIN	MAX	
f_{max}			$C_L = 15 \text{ pF}^*$	80	155		65	65	MHz
			$C_L = 50 \text{ pF}$	50	120		45	45	
t_{pd}^*	CLK	Q	$C_L = 15 \text{ pF}$		6.4	12.8	1	15	ns
t_{PHL}^*	\overline{CLR}				6	12.8	1	15	
t_{pd}	CLK	Q	$C_L = 50 \text{ pF}$		8.3	16.3	1	18.5	ns
	\overline{CLR}				7.9	16.3	1	18.5	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

**switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$ (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV164A	SN74LV164A	UNIT
				MIN	TYP	MAX	MIN	MAX	
f_{max}			$C_L = 15 \text{ pF}^*$	125	220		105	105	MHz
			$C_L = 50 \text{ pF}$	85	165		75	75	
t_{pd}^*	CLK	Q	$C_L = 15 \text{ pF}$		4.5	9	1	10.5	ns
t_{PHL}^*	\overline{CLR}				4.2	8.6	1	10	
t_{pd}	CLK	Q	$C_L = 50 \text{ pF}$		6	11	1	12.5	ns
	\overline{CLR}				5.8	10.6	1	12.5	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

noise characteristics, $V_{CC} = 3.3 \text{ V}$, $C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$ (see Note 5)

PARAMETER	SN74LV164A			UNIT
	MIN	TYP	MAX	
$V_{OL(P)}$ Quiet output, maximum dynamic V_{OL}		0.28	0.8	V
$V_{OL(V)}$ Quiet output, minimum dynamic V_{OL}		-0.22	-0.8	V
$V_{OH(V)}$ Quiet output, minimum dynamic V_{OH}		3.09		V
$V_{IH(D)}$ High-level dynamic input voltage		2.31		V
$V_{IL(D)}$ Low-level dynamic input voltage			0.99	V

NOTE 5: Characteristics are for surface-mount packages only.

operating characteristics, $T_A = 25^\circ\text{C}$

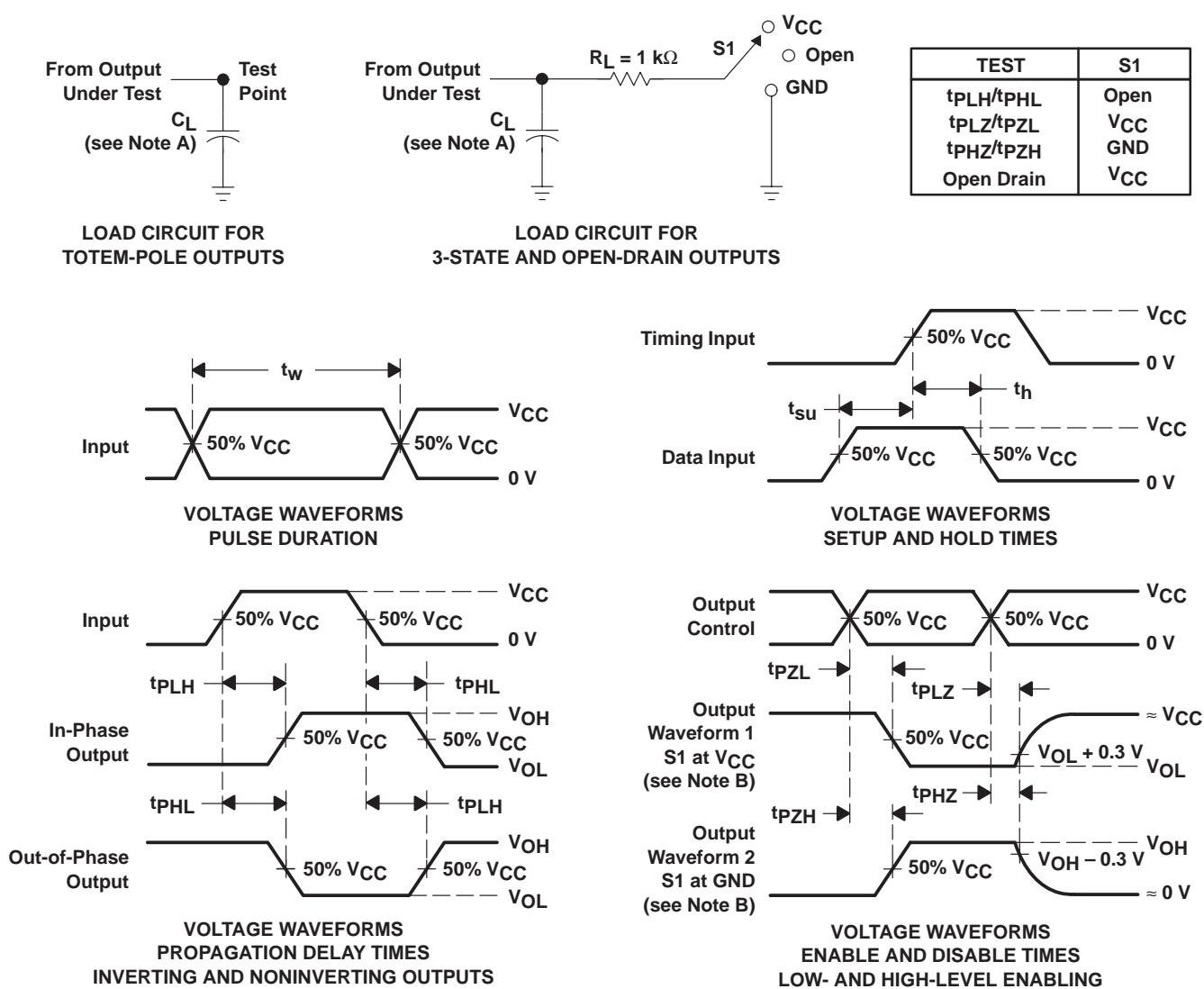
PARAMETER	TEST CONDITIONS	V_{CC}	TYP	UNIT
		3.3 V	48.1	pF
C_{pd} Power dissipation capacitance	$C_L = 50 \text{ pF}$, $f = 10 \text{ MHz}$	5 V	47.5	

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PARAMETER MEASUREMENT INFORMATION



NOTES:

- C_L includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 3 \text{ ns}$, $t_f \leq 3 \text{ ns}$.
- The outputs are measured one at a time with one input transition per measurement.
- t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- t_{PZL} and t_{PZH} are the same as t_{en} .
- t_{PHL} and t_{PLH} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

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