

AT91SAM9260-EK Evaluation Board

User Guide







Table of Contents

Section 1

Overview	1-1
1.1 Scope	1-1
1.2 Deliverables	1-1
1.3 AT91SAM9260-EK Evaluation Board	1-1

Section 2

Setting Up the AT91SAM9260-EK Board	2-1
2.1 Electrostatic Warning	2-1
2.2 Requirements	2-1
2.3 Layout	2-2
2.4 Powering Up the Board	2-3
2.5 Backup Power Supply	2-3
2.6 Getting Started	2-3
2.7 AT91SAM9260-EK Block Diagram	2-4

Section 3

Board Description	3-1
3.1 AT91SAM9260 Microcontroller	3-1
3.2 AT91SAM9260 Block Diagram	3-4
3.3 Microcontroller	3-5
3.4 Memory	3-5
3.5 Clock Circuitry	3-5
3.6 Reset Circuitry	3-5
3.7 Shutdown Controller	3-5
3.8 Power Supply Circuitry	3-5
3.9 Remote Communication	3-5
3.10 Audio Stereo Interface	3-6
3.11 User Interface	3-6
3.12 Debug Interface	3-6
3.13 Expansion Slot	3-6
3.14 PIO Usage	3-7

Section 4

Configuration	4-1
4.1 Jumpers	4-1
4.2 JTAG/ICE	4-2
4.3 Microcontroller Clock	4-2
4.4 Memory	4-2
4.5 Ethernet	4-3
4.6 Miscellaneous	4-3

Section 5

Schematics	5-1
5.1 Schematics	5-1

Section 6

Errata	6-1
6.1 VDD Backup Jumper Selector (J10)	6-1
6.2 JTAGSEL S2 Footprint Selector	6-1
6.3 TWI line pullups are too weak for Fast Mode operation.....	6-1

Section 7

Revision History	7-1
7.1 Revision History	7-1



Section 1

Overview

-
- | | | |
|------------|--|--|
| 1.1 | Scope | <p>The AT91SAM9260-EK evaluation kit enables the evaluation of and code development for applications running on an AT91SAM9260 device.</p> <p>This guide focuses on the AT91SAM9260-EK board as an evaluation platform.</p> <p>The board supports the AT91SAM9260 in an LFBGA217 package as well as in a PQFP208 package.</p> |
| <hr/> | | |
| 1.2 | Deliverables | <p>The AT91SAM9260-EK package contains the following items:</p> <ul style="list-style-type: none">■ an AT91SAM9260-EK board■ universal input AC/DC power supply with US and Europe plug adapter■ one A/B-type USB cable■ one serial RS232 cable■ one RJ45 crossed Ethernet cable■ one CD-ROM that allows the user to begin evaluating the AT91 ARM® Thumb® 32-bit microcontroller quickly. |
| <hr/> | | |
| 1.3 | AT91SAM9260-EK Evaluation Board | <p>The board is equipped with an AT91SAM9260 (217-ball LFBGA package) together with the following:</p> <ul style="list-style-type: none">■ 64 Mbytes of SDRAM memory■ 256 Mbytes of NANDFlash memory■ one Atmel serial DataFlash®■ one Atmel TWI serial EEPROM■ one USB device port interface■ two USB Host port interfaces■ one DBGU serial communication port■ one complete MODEM serial communication port |

- one additional serial communication port with RTS/CTS handshake control
- JTAG/ICE debug interface
- one PHY Ethernet 100-base TX with three status LEDs
- one Atmel AT73C213 Audio DAC
- one Power LED and one general-purpose LED
- two user input push buttons
- one Wakeup input push button
- one reset push button
- one DataFlash, SD/MMC card slot
- four expansion connectors (PIOA, PIOB, PIOC, IMAGE SENSOR)
- one BGA-like EBI expansion footprint connector
- one Lithium Coin Cell Battery Retainer for 12 mm cell size

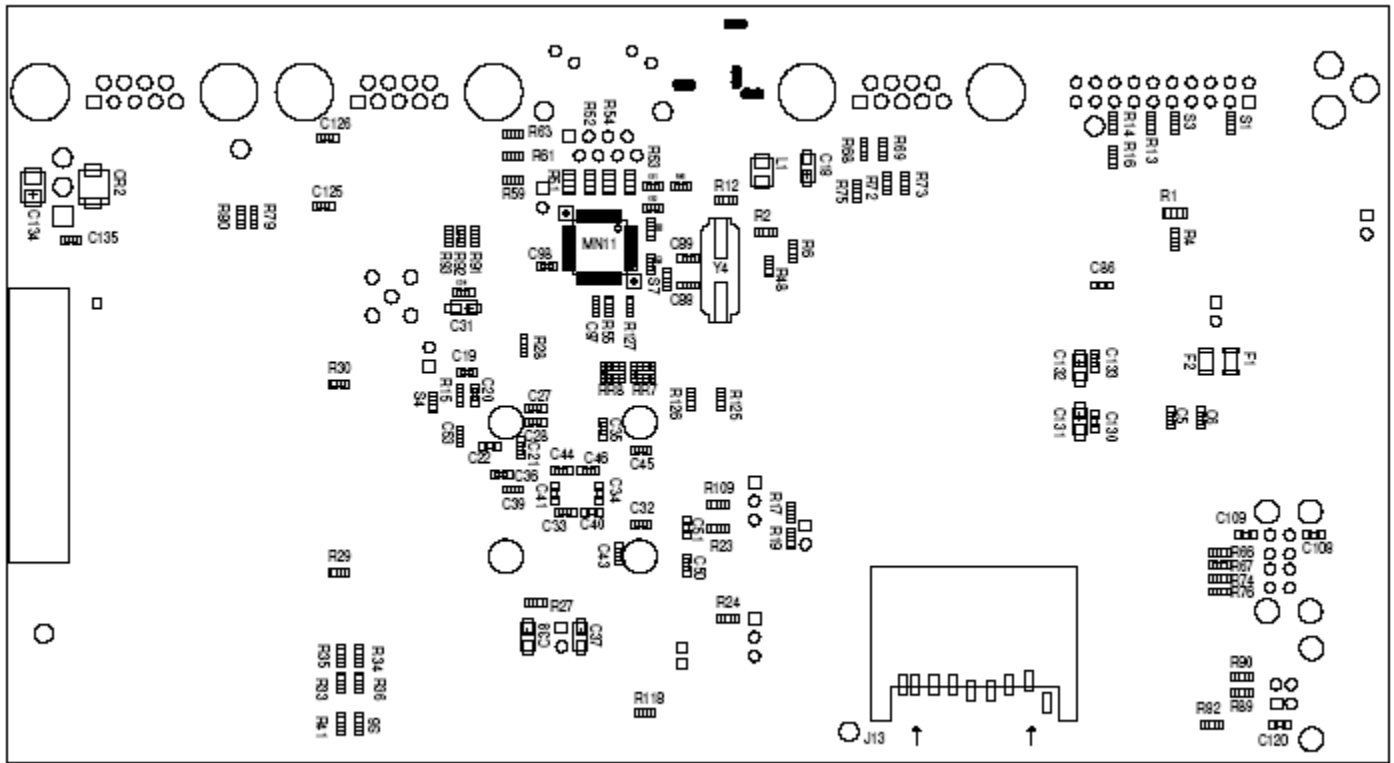


Section 2

Setting Up the AT91SAM9260-EK Board

-
- | | | |
|------------|------------------------------|---|
| 2.1 | Electrostatic Warning | The AT91SAM9260-EK evaluation board is shipped in protective anti-static packaging. The board must not be subjected to high electrostatic potentials. A grounding strap or similar protective device should be worn when handling the board. Avoid touching the component pins or any other metallic element. |
|------------|------------------------------|---|
-
- | | | |
|------------|---------------------|---|
| 2.2 | Requirements | <p>In order to set up the AT91SAM9260-EK evaluation board, the following items are needed:</p> <ul style="list-style-type: none">■ the AT91SAM9260-EK evaluation board itself.■ AC/DC power adapter (5V at 2A), 2.1 mm by 5.5 mm |
|------------|---------------------|---|
-

Figure 2-2. AT91SAM9260-EK Layout - Bottom View



- 2.4 Powering Up the Board** The AT91SAM9260-EK requires 5V DC ($\pm 5\%$). DC power is supplied to the board via the 2.1 mm by 5.5 mm socket J1. Coaxial plug center positive standard.
- 2.5 Backup Power Supply** The user has the possibility to plug a battery (3V Lithium Battery CR1225 or equivalent) in order to permanently power the backup part of the device. In this case, J10 configuration must be set in position 1, 2.
- Refer to [Section 4.1](#).
- 2.6 Getting Started** The AT91SAM9260-EK evaluation board is delivered with a CD-ROM containing all necessary information and step-by-step procedures for working with the most common development toolchains. Please refer to this CD-ROM, or to the AT91 web site, <http://www.atmel.com/products/AT91/>, for the most up-to-date information on getting started with the AT91SAM9260-EK.



Section 3

Board Description

- 3.1 AT91SAM9260 Microcontroller**
- Incorporates the ARM926EJ-S™ ARM® Thumb® Processor
 - DSP Instruction Extensions, ARM Jazelle® Technology for Java® Acceleration
 - 8-KByte Data Cache, 8-KByte Instruction Cache, Write Buffer
 - 200 MIPS at 180 MHz
 - Memory Management Unit
 - EmbeddedICE™, Debug Communication Channel Support
 - Additional Embedded Memories
 - One 32-KByte Internal ROM, Single-cycle Access At Maximum Matrix Speed
 - Two 4-KByte Internal SRAM, Single-cycle Access At Maximum Matrix Speed
 - External Bus Interface (EBI)
 - Supports SDRAM, Static Memory, ECC-enabled NANDFlash and CompactFlash®
 - USB 2.0 Full Speed (12 Mbits per second) Device Port
 - On-chip Transceiver, 2,432-byte Configurable Integrated DPRAM
 - USB 2.0 Full Speed (12 Mbits per second) Host Single Port in the 208-lead PQFP Package and Double Port in 217-ball LFBGA Package
 - Single or Dual On-chip Transceivers
 - Integrated FIFOs and Dedicated DMA Channels
 - Ethernet MAC 10/100 Base T
 - Media Independent Interface or Reduced Media Independent Interface
 - 28-byte FIFOs and Dedicated DMA Channels for Receive and Transmit
 - Image Sensor Interface
 - ITU-R BT. 601/656 External Interface, Programmable Frame Capture Rate
 - 12-bit Data Interface for Support of High Sensibility Sensors
 - SAV and EAV Synchronization, Preview Path with Scaler, YCbCr Format
 - Bus Matrix
 - Six 32-bit-layer Matrix
 - Boot Mode Select Option, Remap Command
 - Fully-featured System Controller, including
 - Reset Controller, Shutdown Controller
 - Four 32-bit Battery Backup Registers for a Total of 16 Bytes
 - Clock Generator and Power Management Controller
 - Advanced Interrupt Controller and Debug Unit
 - Periodic Interval Timer, Watchdog Timer and Real-time Timer
 - Reset Controller (RSTC)
 - Based on a Power-on Reset Cell, Reset Source Identification and Reset Output

Control

- Clock Generator (CKGR)
 - Selectable 32768Hz Low-power Oscillator or Internal Low Power RC Oscillator on Battery Backup Power Supply, Providing a Permanent Slow Clock
 - 3 to 20 MHz On-chip Oscillator, One up to 240 MHz PLL and One up to 130 MHz PLL
- Power Management Controller (PMC)
 - Very Slow Clock Operating Mode, Software Programmable Power Optimization Capabilities
 - Two Programmable External Clock Signals
- Advanced Interrupt Controller (AIC)
 - Individually Maskable, Eight-level Priority, Vectored Interrupt Sources
 - Three External Interrupt Sources and One Fast Interrupt Source, Spurious Interrupt Protected
- Debug Unit (DBGU)
 - 2-wire UART and Support for Debug Communication Channel, Programmable ICE Access Prevention
- Periodic Interval Timer (PIT)
 - 20-bit Interval Timer plus 12-bit Interval Counter
- Watchdog Timer (WDT)
 - Key-protected, Programmable Only Once, Windowed 16-bit Counter Running at Slow Clock
- Real-time Timer (RTT)
 - 32-bit Free-running Backup Counter Running at Slow Clock with 16-bit Prescaler
- One 4-channel 10-bit Analog-to-Digital Converter
- Three 32-bit Parallel Input/Output Controllers (PIOA, PIOB, PIOC)
 - 96 Programmable I/O Lines Multiplexed with up to Two Peripheral I/Os
 - Input Change Interrupt Capability on Each I/O Line
 - Individually Programmable Open-drain, Pull-up Resistor and Synchronous Output
 - High-current Drive I/O Lines, Up to 16 mA Each
- Peripheral DMA Controller Channels (PDC)
- One Two-slot MultiMedia Card Interface (MCI)
 - SDCard/SDIO and MultiMediaCard™ Compliant
 - Automatic Protocol Control and Fast Automatic Data Transfers with PDC
- One Synchronous Serial Controller (SSC)
 - Independent Clock and Frame Sync Signals for Each Receiver and Transmitter
 - I²S Analog Interface Support, Time Division Multiplex Support
 - High-speed Continuous Data Stream Capabilities with 32-bit Data Transfer
- Four Universal Synchronous/Asynchronous Receiver Transmitters (USART)
 - Individual Baud Rate Generator, IrDA® Infrared Modulation/Demodulation, Manchester Encoding/Decoding
 - Support for ISO7816 T0/T1 Smart Card, Hardware Handshaking, RS485 Support
 - Full Modem Signal Control on USART0
- Two 2-wire UARTs
- Two Master/Slave Serial Peripheral Interfaces (SPI)
 - 8- to 16-bit Programmable Data Length, Four External Peripheral Chip Selects
 - Synchronous Communications
- Two Three-channel 16-bit Timer/Counters (TC)
 - Three External Clock Inputs, Two Multi-purpose I/O Pins per Channel
 - Double PWM Generation, Capture/Waveform Mode, Up/Down Capability

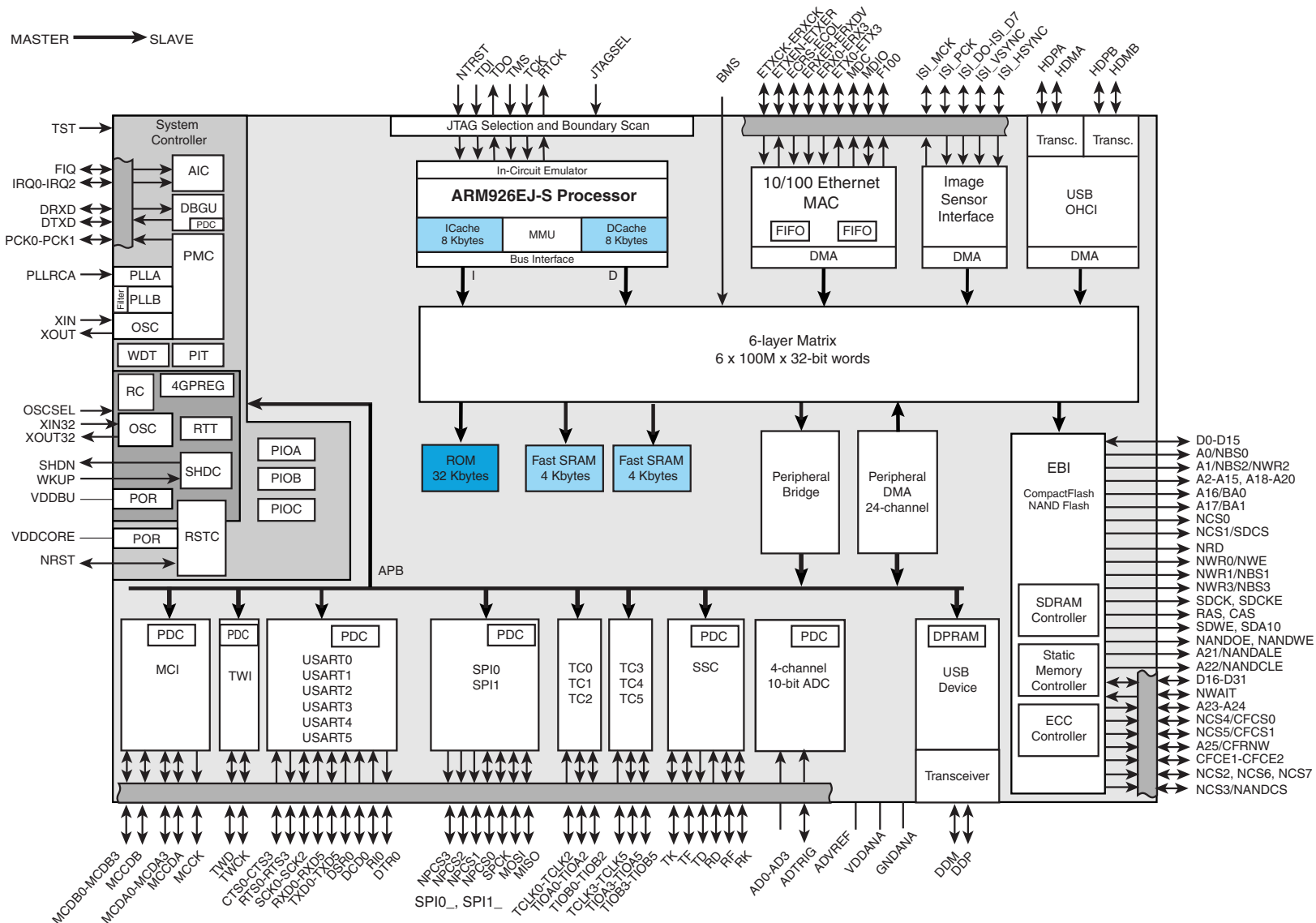


- High-Drive Capability on Outputs TIOA0, TIOA1, TIOA2
- One Two-wire Interface (TWI)
 - Master, Multi-master and Slave Mode Operation
 - General Call Supported in Slave Mode
 - Connection to PDC Channel To Optimize Data Transfers in Master Mode Only
- IEEE® 1149.1 JTAG Boundary Scan on All Digital Pins
- Required Power Supplies:
 - 1.65V to 1.95V for VDDDBU, VDDCORE, VDDOSC and VDDPLL
 - 3.0V to 3.6V for VDDIOP0, VDDIOP1 (Peripheral I/Os) and VDDANA (Analog to Digital Converter)
 - Programmable 1.65V to 1.95V or 3.0V to 3.6V for VDDIOM (Memory I/Os)
- Available in a 208-lead PQFP and 217-ball LFBGA Package

3.2

AT91SAM9260
Block Diagram

Figure 3-1. AT91SAM9260 Block Diagram



3.3	Microcontroller	■ One LFBGA 217-ball fitted on board ■ One LQFP 208-lead footprint To try the microcontroller in the LQFP package, the user has to unsolder MN4 and solder the PQFP208 microcontroller on the MN6 footprint.
3.4	Memory	■ 32 Kbytes of Internal ROM ■ Two 4-KByte Internal SRAM ■ Atmel serial DataFlash ■ 64 Mbytes of SDRAM memory (32-bit bus width) ■ 256 Mbytes of NANDFlash memory (8-bit bus width) ■ TWI serial EEPROM
3.5	Clock Circuitry	■ 18.432 MHz standard crystal for the embedded oscillator ■ Selectable 32768Hz Low-power external standard crystal Oscillator or Internal Low Power RC Oscillator
3.6	Reset Circuitry	■ Internal reset controller with bi-directional reset pin ■ External reset pushbutton
3.7	Shutdown Controller	■ Programmable shutdown and Wake-Up ■ Wake-up push button
3.8	Power Supply Circuitry	■ On-board 1.8V High Efficiency step-down charge pump regulator with shutdown control ■ On-board 3.3V linear regulator with shutdown control
3.9	Remote Communication	■ One serial interface (DBGU COM Port) via RS-232 DB9 male socket ■ One complete modem serial interface (COM Port 0) via RS-232 DB9 male socket ■ One additional serial interface (COM Port 1) with RTS/CTS handshake control via RS-232 DB9 male socket ■ USB V2.0 full-speed compliant, 12 Mbits per second (UDP) ■ Two⁽¹⁾ USB Host ports V2.0 full-speed compliant, 12 Mbits per second (UHP) ■ One Ethernet 100-base TX with three status LEDs

-
- | | | |
|-------------|-------------------------------|--|
| 3.10 | Audio Stereo Interface | <ul style="list-style-type: none">■ One Atmel stereo audio DAC (AT73C213)■ One 32 Ohm/20 mW Stereo Headset output (J4) with master volume and mute controls |
|-------------|-------------------------------|--|
-
- | | | |
|-------------|-----------------------|--|
| 3.11 | User Interface | <ul style="list-style-type: none">■ Two user input pushbuttons⁽²⁾■ One user green LED■ One yellow power LED (can be also software controlled) |
|-------------|-----------------------|--|
-
- | | | |
|-------------|------------------------|---|
| 3.12 | Debug Interface | <ul style="list-style-type: none">■ 20-pin JTAG/ICE interface connector■ DBGU COM port |
|-------------|------------------------|---|
-
- | | | |
|-------------|-----------------------|--|
| 3.13 | Expansion Slot | <ul style="list-style-type: none">■ One DataFlash, SD/MMC card slot■ All I/Os of the AT91SAM9260 are routed to peripheral extension connectors■ All I/Os of the AT91SAM9260 Image Sensor Interface are routed to peripheral extension connectors■ All EBI Signals of the AT91SAM9260 are routed to extension footprint connectors (J25) <p>This allows the developer to check the integrity of the components and to extend the features of the board by adding external hardware components or boards.</p> <p>Notes: 1. Only one available with the 208-lead PQFP package.
 2. Not available with the 208-lead PQFP package.</p> |
|-------------|-----------------------|--|
-
- 3-6
- 
- AT91SAM9260-EK Evaluation Board User Guide
- 6234C-ATARM-22-Mar-07

3.14 PIO Usage

Table 3-1. PIO Controller A

I/O Line	Peripheral A	Peripheral B	Comments	Function
PA0	SPI0_MISO	MCDB0		SPI DATAFLASH, SPI/MCI SD/MMC/DATAFLASH Slot
PA1	SPI0_MOSI	MCCDB		(PA0..PA5)
PA2	SPI0_SPCK			
PA3	SPI0_NPCS0	MCDB3		
PA4	RTS2	MCDB2		
PA5	CTS2	MCDB1		
PA6	MCDA0			User LED
PA7	MCCDA			ETHERNET DM9161A MII/RMII (IRQ)
PA8	MCCK			MCI SD/MMC/DATAFLASH Slot
PA9	MCDA1			Power LED
PA10	MCDA2	ETX2		ETHERNET DM9161A MII Interface (PA10..PA11)
PA11	MCDA3	ETX3		
PA12	ETX0			ETHERNET DM9161A RMII Interface (PA12..PA19)
PA13	ETX1			
PA14	ERX0			
PA15	ERX1			
PA16	ETXEN			
PA17	ERXDV			
PA18	ERXER			
PA19	ETXCK			
PA20	EMDC			ETHERNET DM9161A MII/RMII Interface (PA20..PA21)
PA21	EMDIO			
PA22	ADTRG	ETXER		ETHERNET DM9161A MII Interface
PA23	TWD	ETX2		SERIAL EEPROM (SDA)
PA24	TWCK	ETX3		SERIAL EEPROM (SCL)
PA25	TCLK0	ERX2		ETHERNET DM9161A MII Interface (PA25..PA29)
PA26	TIOA0	ERX3	High-Drive	
PA27	TIOA1	ERXCK	High-Drive	
PA28	TIOA2	ECRS	High-Drive	
PA29	SCK1	ECOL		
PA30	SCK2	RXD4		(BP3) User's interface Push Button
PA31	SCK0	TXD4		(BP4) User's interface Push Button

Table 3-2. PIO B Controller

I/O Line	Peripheral A	Peripheral B	Comments	Function
PB0	SPI1_MISO	TIOA3		Audio DAC AT73C213 (MISO)
PB1	SPI1_MOSI	TIOB3		Audio DAC AT73C213 (MOSI)
PB2	SPI1_SPCK	TIOA4		Audio DAC AT73C213 (SPCK)
PB3	SPI1_NPCS0	TIOA5		Audio DAC AT73C213 (Chip Select)
PB4	TXD0			COM PORT 0 (TXD)
PB5	RXD0			COM PORT 0 (RXD)
PB6	TXD1	TCLK1		COM PORT 1 (TXD)
PB7	RXD1	TCLK2		COM PORT 1 (RXD)
PB8	TXD2			
PB9	RXD2			
PB10	TXD3	ISI_D8		(J28) IMAGE SENSOR CONNECTOR (PB10..PB13)
PB11	RXD3	ISI_D9		
PB12	TXD5	ISI_D10		
PB13	RXD5	ISI_D11		
PB14	DRXD			SERIAL DEBUG PORT(RXD)
PB15	DTXD			SERIAL DEBUG PORT(TXD)
PB16	TK0	TCLK3		Audio DAC AT73C213 (BCLK)
PB17	TF0	TCLK4		Audio DAC AT73C213 (LRFS)
PB18	TD0	TIOB4		Audio DAC AT73C213 (SDIN)
PB19	RD0	TIOB5		(J28) IMAGE SENSOR CONNECTOR (CTRL2)
PB20	RK0	ISI_D0		(J28) IMAGE SENSOR CONNECTOR (PB20..PB31)
PB21	RF0	ISI_D1		
PB22	DSR0	ISI_D2		Warning: Shared with COM PORT 0 (PB22..PB27)
PB23	DCD0	ISI_D3		
PB24	DTR0	ISI_D4		
PB25	RI0	ISI_D5		
PB26	RTS0	ISI_D6		
PB27	CTS0	ISI_D7		
PB28	RTS1	ISI_PCK		Warning: Shared with COM PORT 1 (PB28..PB29)
PB29	CTS1	ISI_VSYNC		
PB30	PCK0	ISI_HSYNC		
PB31	PCK1	ISI_MCK		

Table 3-3. PIO C Controller

I/O Line	Peripheral A	Peripheral B	Comments	Function
PC0	AD0	SCK3		
PC1	AD1	PCK0		Audio DAC AT73C213 (MCLK)
PC2	AD2	PCK1		
PC3	AD3	SPI1_NPCS3		
PC4	A23	SPI1_NPCS2		(J28) IMAGE SENSOR CONNECTOR (CTRL1)
PC5	A24	SPI1_NPCS1		USB_CNx (VBUS DETECT)
PC6	TIOB2	CFCE1		
PC7	TIOB1	CFCE2		
PC8	NCS4/CFCS0	RTS3		
PC9	NCS5/CFCS1	TIOB0		
PC10	A25/CFRNW	CTS3		
PC11	NCS2	SPI0_NPCS1		SPI DATAFLASH memory (Chip Select)
PC12	IRQ0	NCS7		
PC13	FIQ	NCS6		NandFlash (RDYBSY)
PC14	NCS3/NANDCS	IRQ2		NandFlash (NANDCS)
PC15	NWAIT	IRQ1		
PC16	D16	SPI0_NPCS2		EBI Data Bus (PC16..PC31)
PC17	D17	SPI0_NPCS3		
PC18	D18	SPI1_NPCS1		
PC19	D19	SPI1_NPCS2		
PC20	D20	SPI1_NPCS3		
PC21	D21	EF100		
PC22	D22	TCLK5		
PC23	D23			
PC24	D24			
PC25	D25			
PC26	D26			
PC27	D27			
PC28	D28			
PC29	D29			
PC30	D30			
PC31	D31			



Section 4

Configuration

4.1 Jumpers

Table 4-1. Jumpers Configuration

Designation	Default Setting	Feature
JP2	Closed	3.3V Jumper ⁽¹⁾
JP3	Closed	Forces power on. To use the software shutdown control, J3 must be opened. 3V battery backup must be present and J10 jumper set in position 1-2
JP6	Closed	VDDPLL Jumper ⁽¹⁾
JP7	Opened	Enables boot on the internal ROM
	Closed	Enables boot on the NCS0
JP9	2 - 3	Slow Clock OSCSEL 1-2: Internal RC Oscillator 2-3: External Crystal Oscillator
JP10	2 - 3	VDDBU Jumper select ⁽¹⁾ 1-2: Lithium 3V Battery 2-3: 1.8V from VDDCORE
JP12	Closed	VDDCORE Jumper ⁽¹⁾
JP15	Closed	Enables Ethernet Auto MDIX control

Note: 1. These jumpers are provided for power consumption measurement use. By default, they are closed. To use this feature, the user has to open the strap and insert an ammeter.

4.2 JTAG/ICE

Table 4-2. JTAG/ICE Configuration

Designation	Default Setting	Feature
S1	Opened	Disables the ICE NTRST input
S2	Opened	Selects ICE mode or JTAG mode (See Errata)
S3	Opened	Disables TCK <-> RTCK local loop. If S3 is closed, R13 must be unsoldered.
R13	Soldered	Enables the ICE RTCK return. S3 must be opened
R14	Soldered	Enables the ICE NRST input

4.3 Microcontroller Clock

Table 4-3. Microcontroller Clock Configuration

Designation	Default Setting	Feature
R18/R20	Soldered	Enables the use of 18.432MHz crystal. If external clock used, R18/R20 must be unsoldered and S4 closed.
S4	Opened	
J9		Slow Clock Setting. See Table 4-1 .

4.4 Memory

Table 4-4. Memory Configuration

Designation	Default Setting	Feature
SDRAM		
R31	Soldered	Enables MN7 Chip select access
R32	Soldered	Enables MN8 Chip select access
NANDFlash (MN6x)		
R36	Soldered	Enables the use of NANDFlash (MN6x)
R34	Soldered	Enables the use of Ready Busy signal
S6	Opened	Disables write protect
SERIAL DATAFLASH (MN9)		
R40	Soldered	Enable the use of the Serial DataFlash (MN9)
S5	Opened	Disables the write protect.
TWI SERIAL EEPROM (MN10)		
R46	Soldered	Enables SCL access
R47	Soldered	Enables SDA access

4.5 Ethernet

RMII is the factory default mode.

To evaluate the MII mode, the user has to unsolder R49, R50, R127 and close S7 and S8.

When the RMII mode is used, the user can use the specific MII signals as PIO, but the following resistors must be unsoldered (R119 to R126).

4.6 Miscellaneous

Refer to the TOP level schematic for the PIO usage.

Table 4-5.

Designation	Default Setting	Feature
R82	Soldered	USB DEVICE: Enables the use of the USBCNX signal
R72	Soldered	DBGU COM Port: Enables the use of DTXD output signal
R73	Soldered	Enables the use of DRXD input
		RS232 COM Port 0: Enable the use of outputs signal
R94	Soldered	RTS0
R95		TXD0
R96		DTR0
		RS232 COM Port 0: Enable the use of inputs signal
R98	Soldered	DCD0
R101		DSR0
R103		RXD0
R104		CTS0
R105		RI0
R106		Enables all MAX3241E outputs buffer
		RS232 COM Port 1: Enable the use of outputs signal
R83	Soldered	TXD1
R85		RTS1
		RS232 COM Port 1: Enable the use of inputs signal
R86	Soldered	RXD1
R88		CTS1
TP1	N.A	GND Test point
TP2	N.A	GND Test point.
TP3	N.A	GND Test point.
TP4	N.A	GND Test point.
TP5	N.A	Reserved: do not use
TP6	N.A	Reserved: do not use



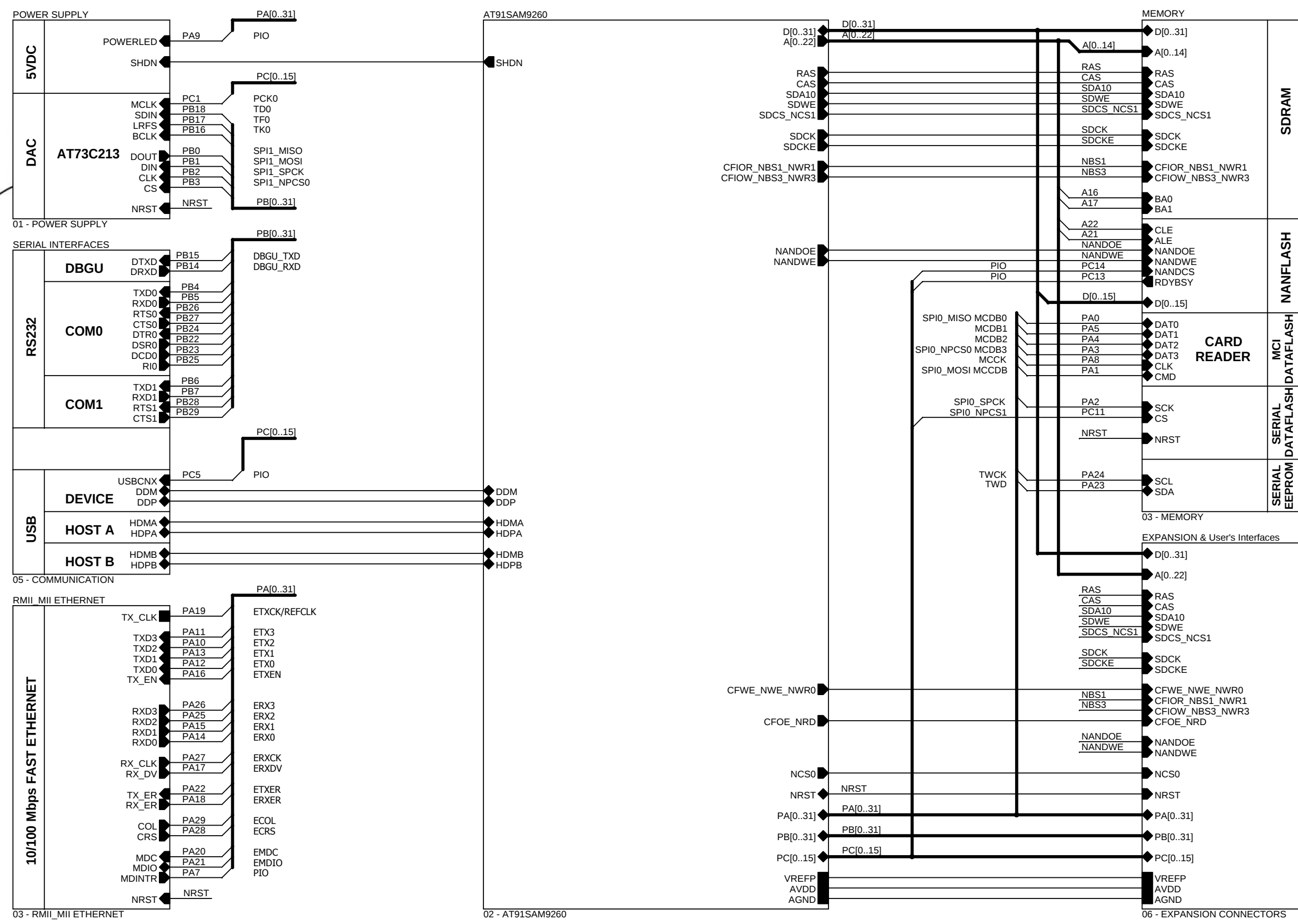
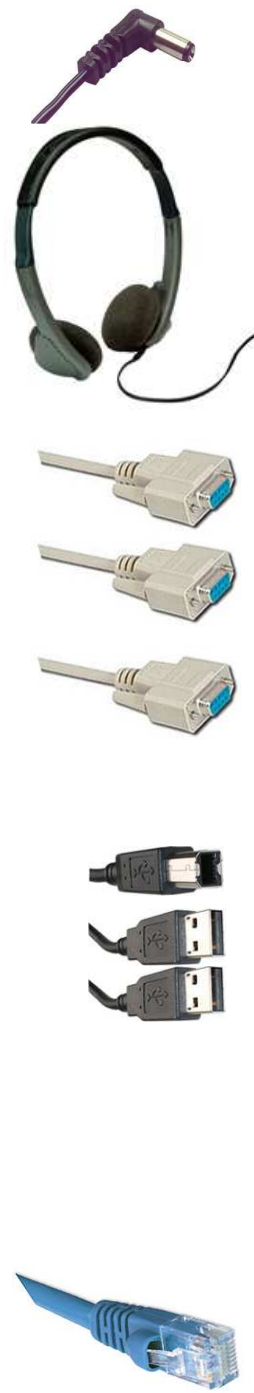
Section 5

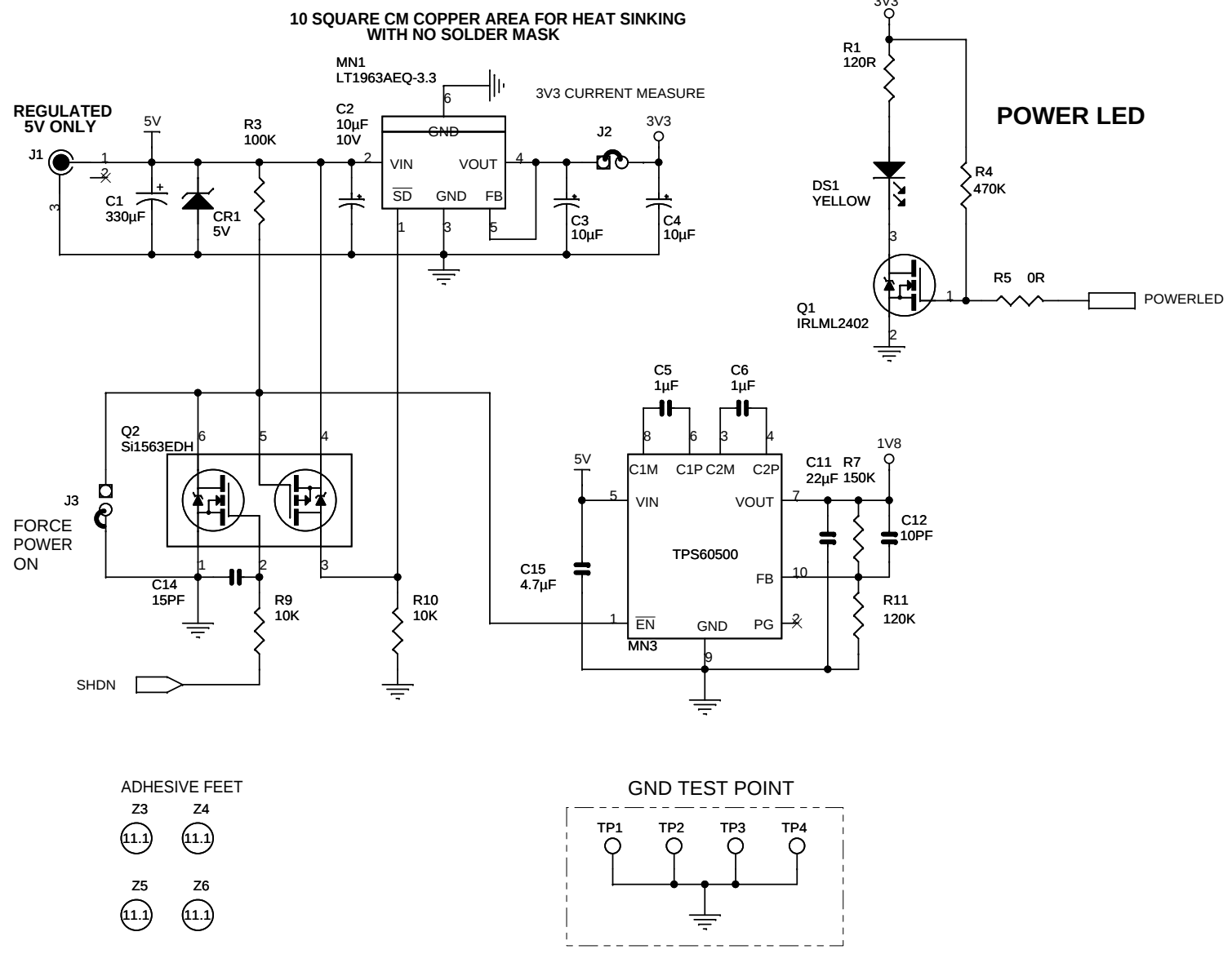
Schematics

5.1 Schematics

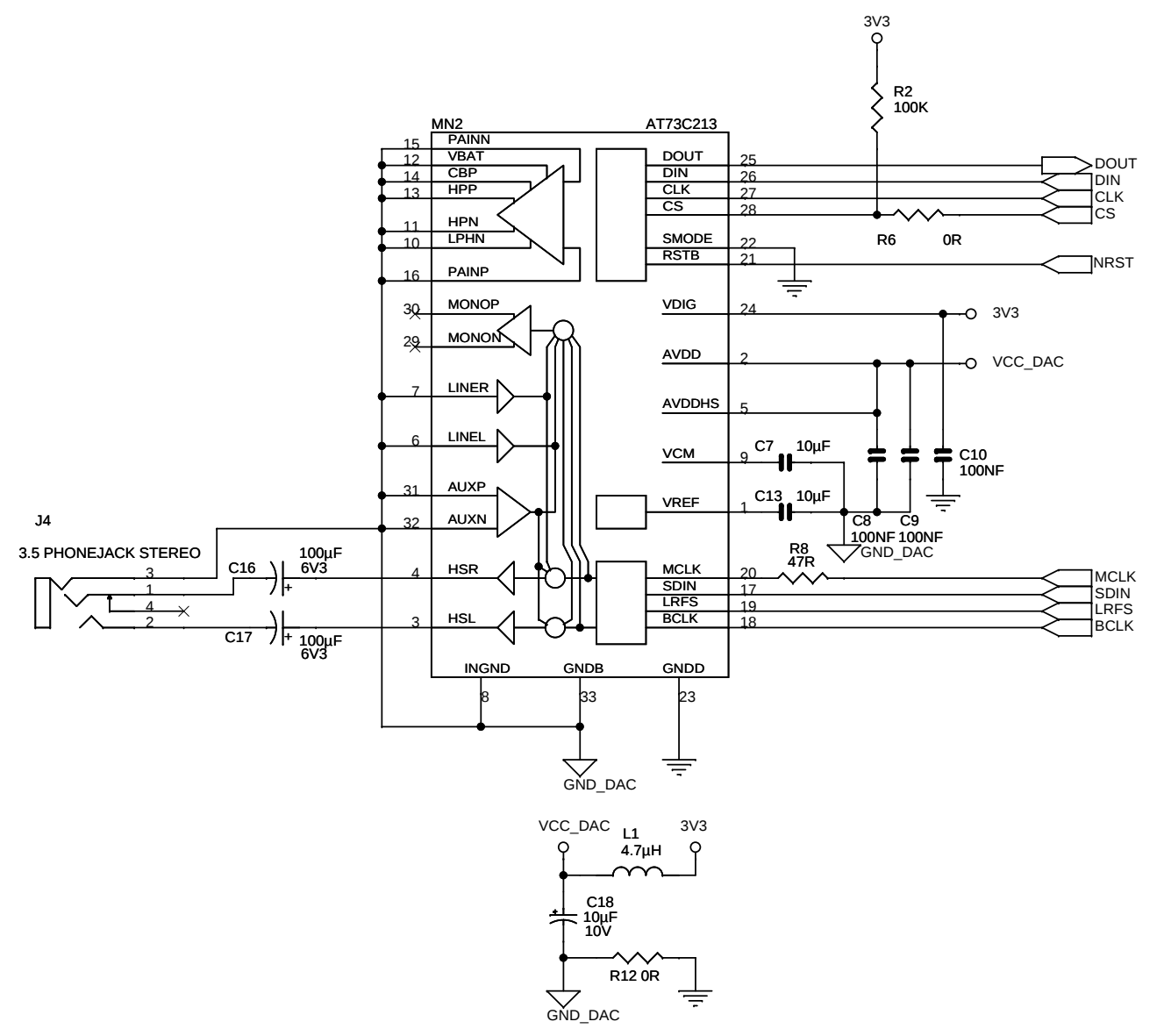
This section contains the following schematics:

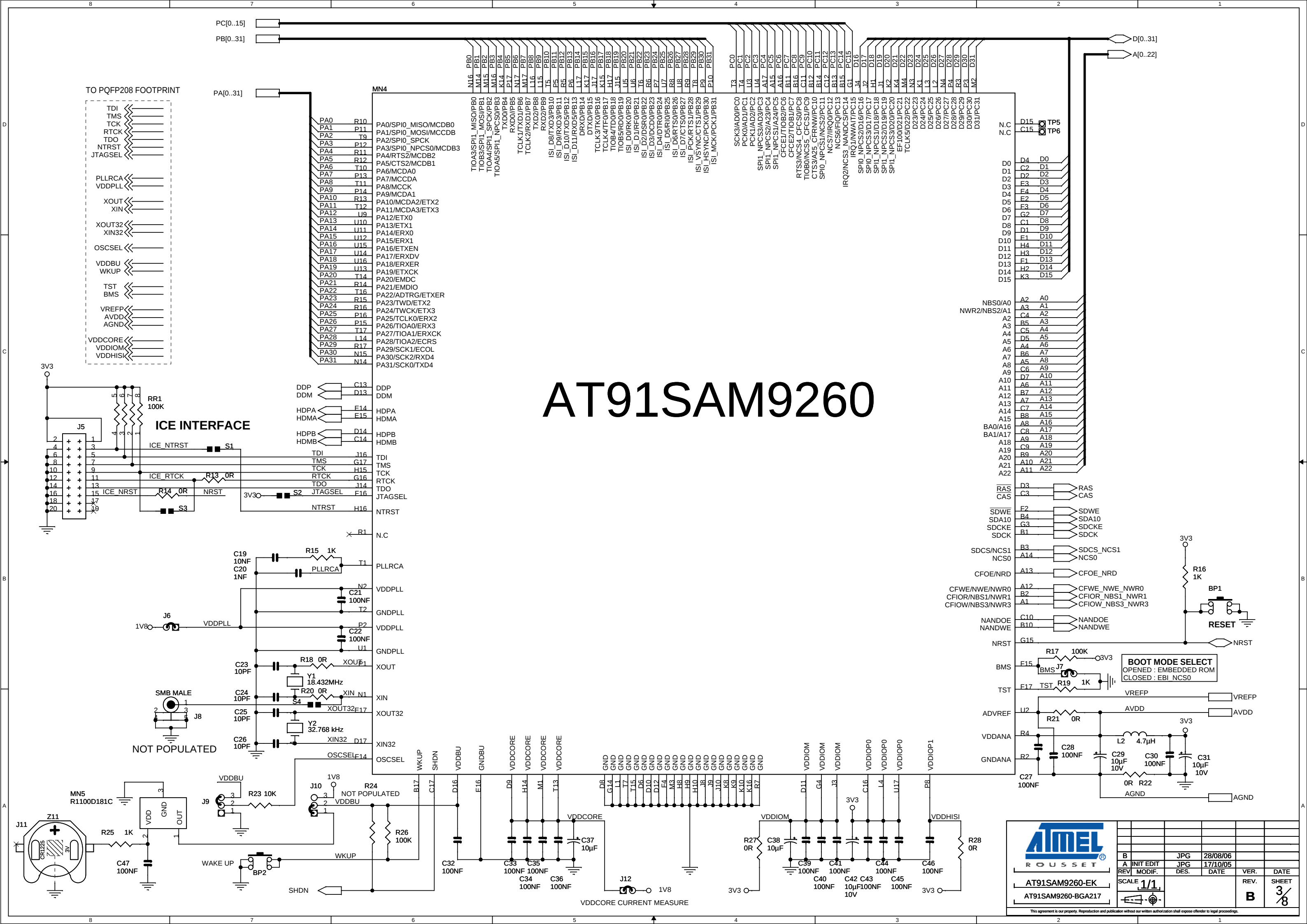
- Board Layout - Top View
- Power supply and audio
- 217-ball BGA AT91SAM9260 Microcontroller
- 208-pin LQFP AT91SAM9260 Microcontroller
- Memory
- Ethernet
- Serial Interface
- Expansion and User Interface



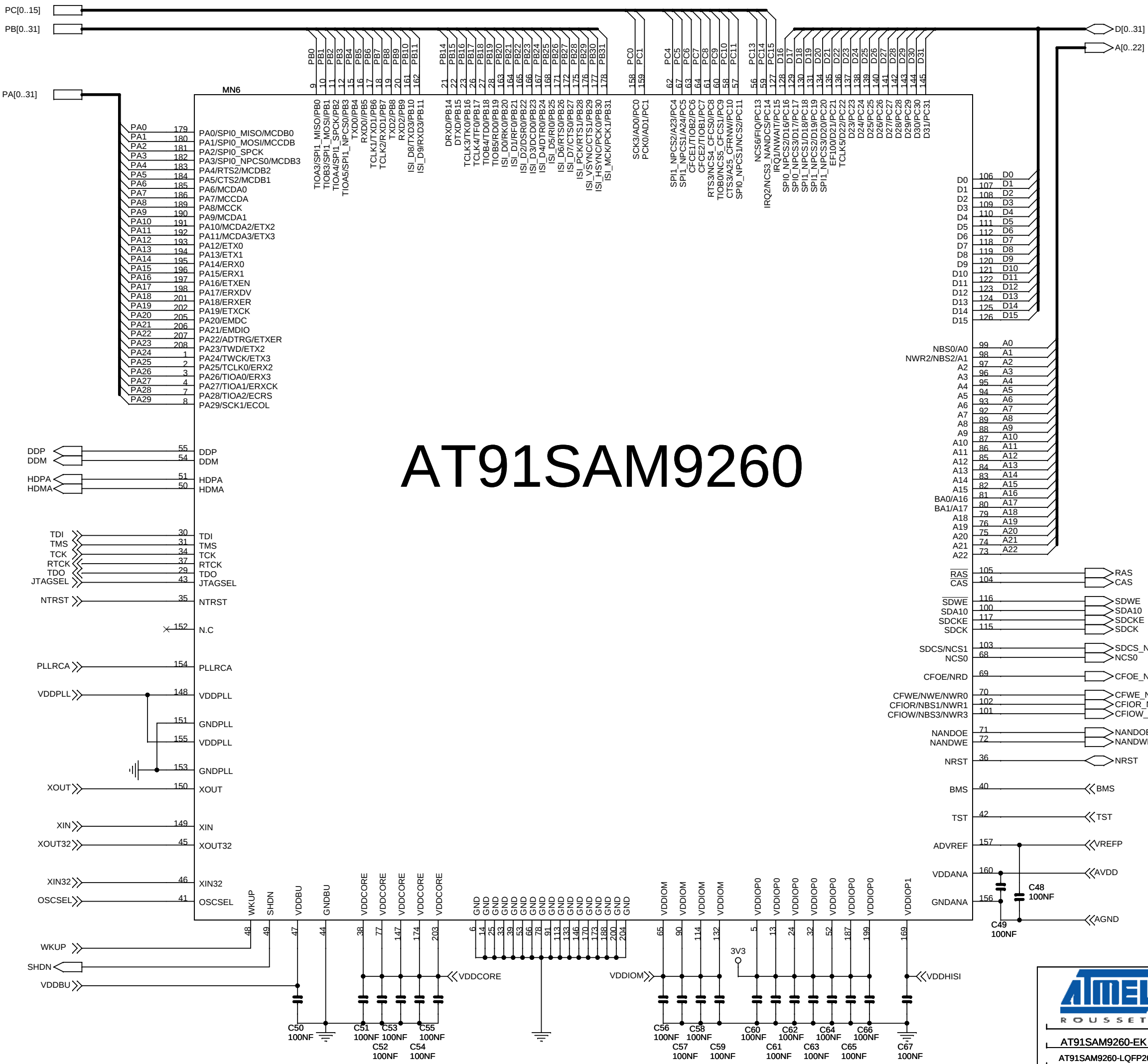


AUDIO DAC INTERFACE



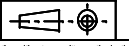


AT91SAM9260

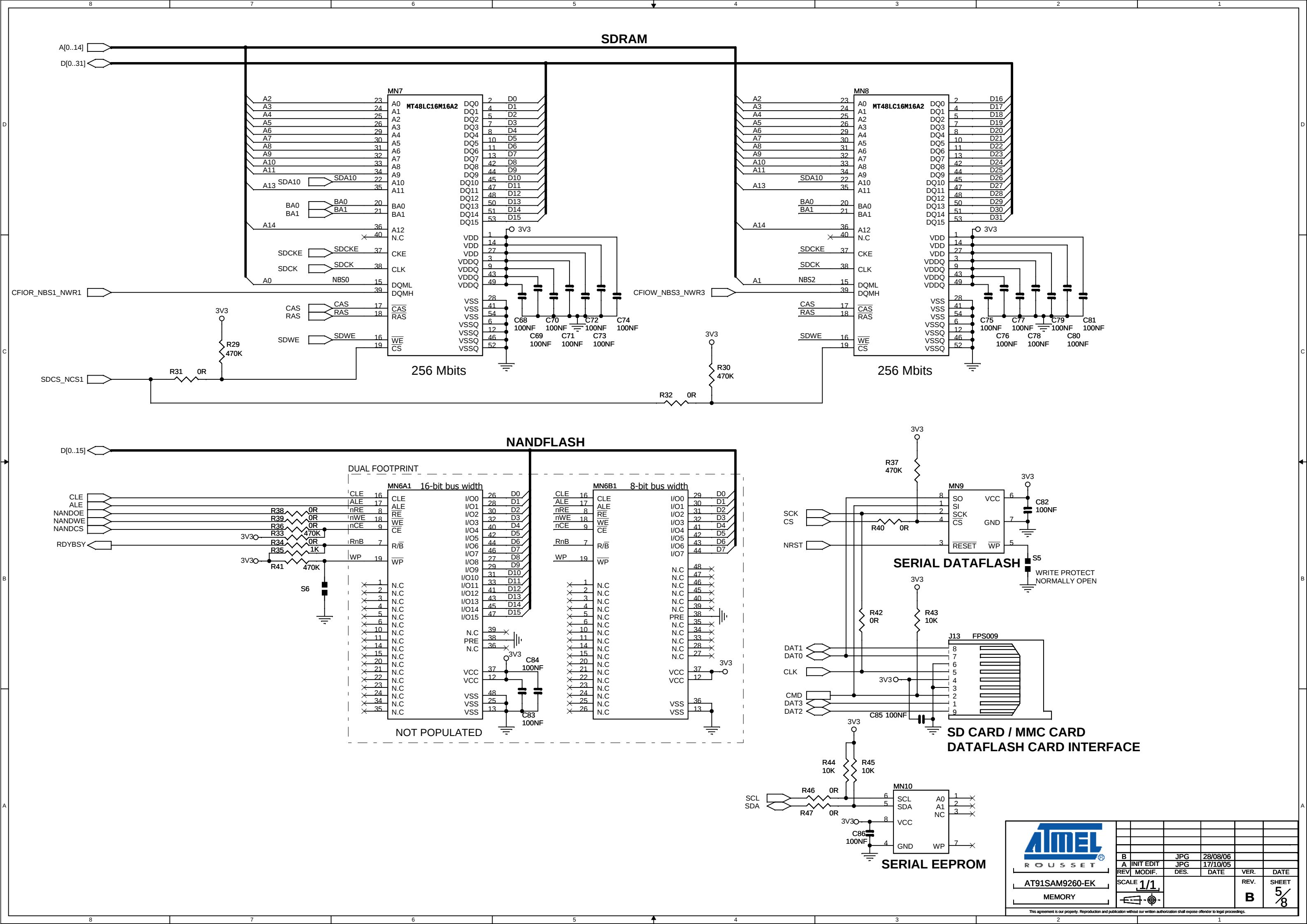


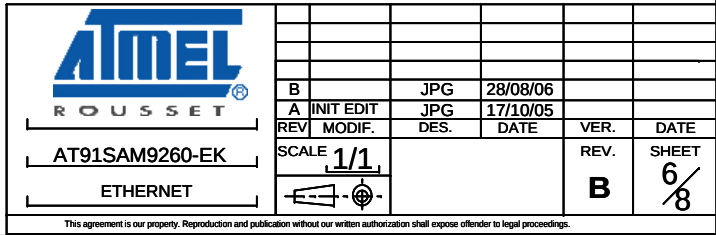


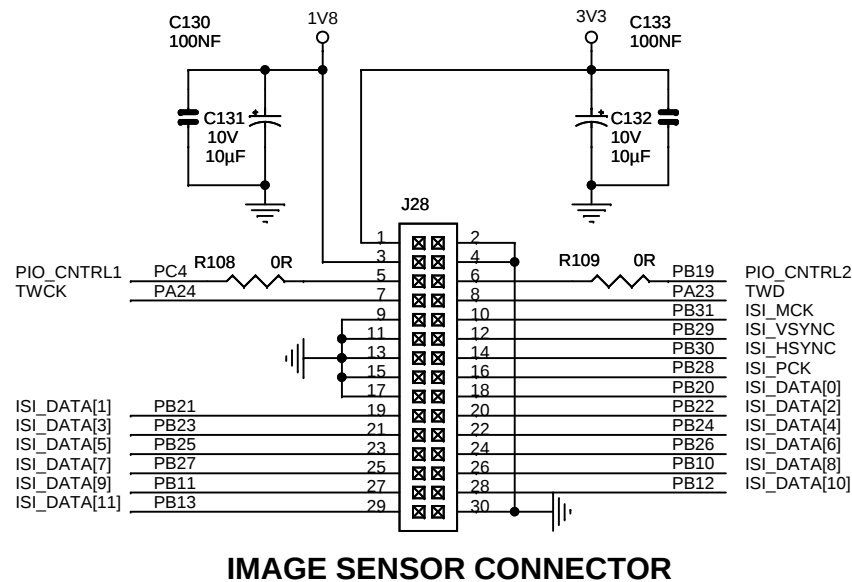
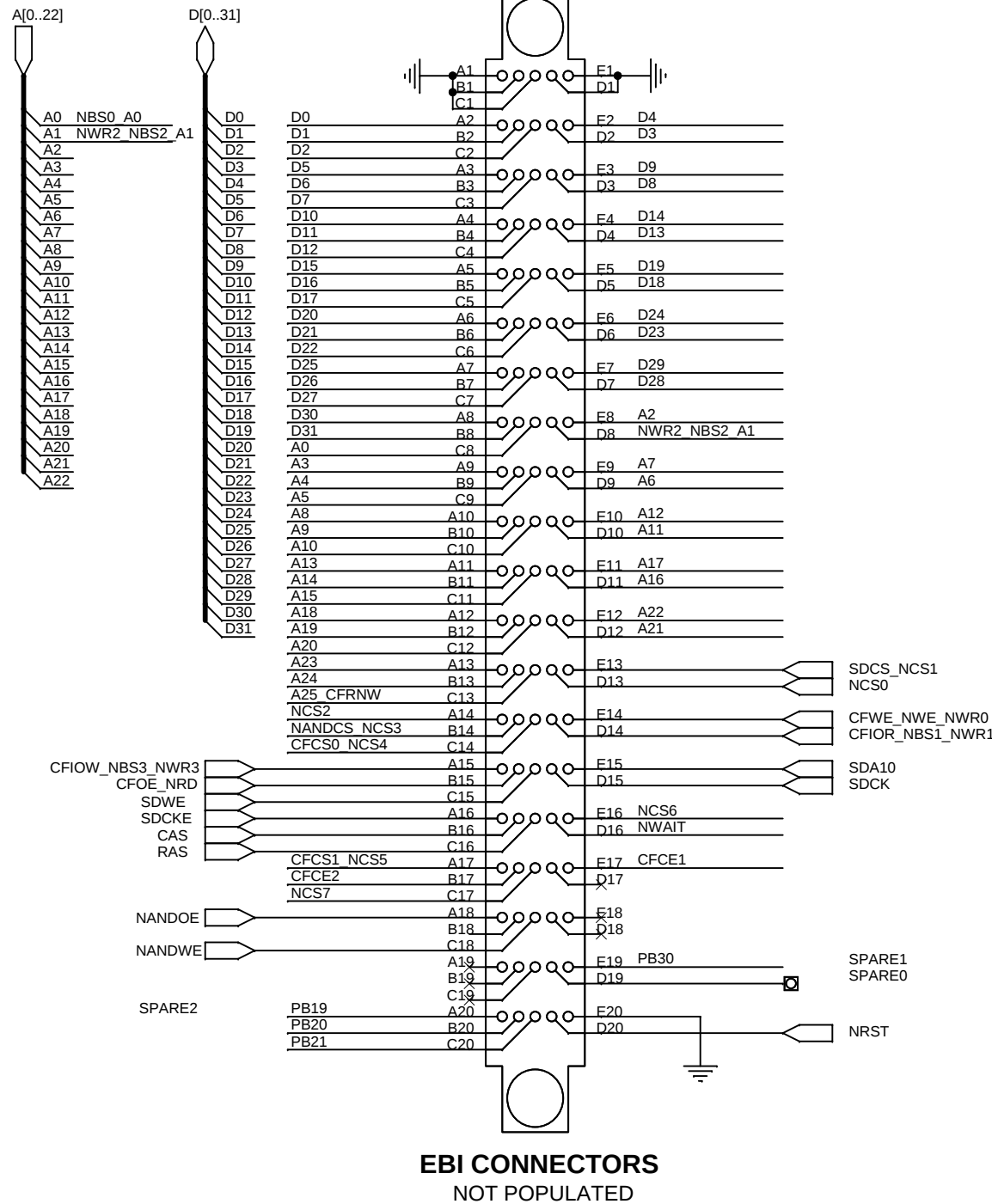
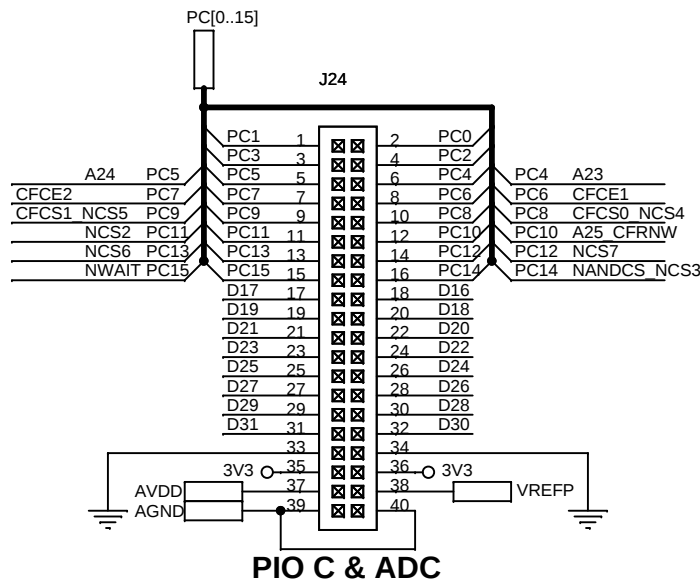
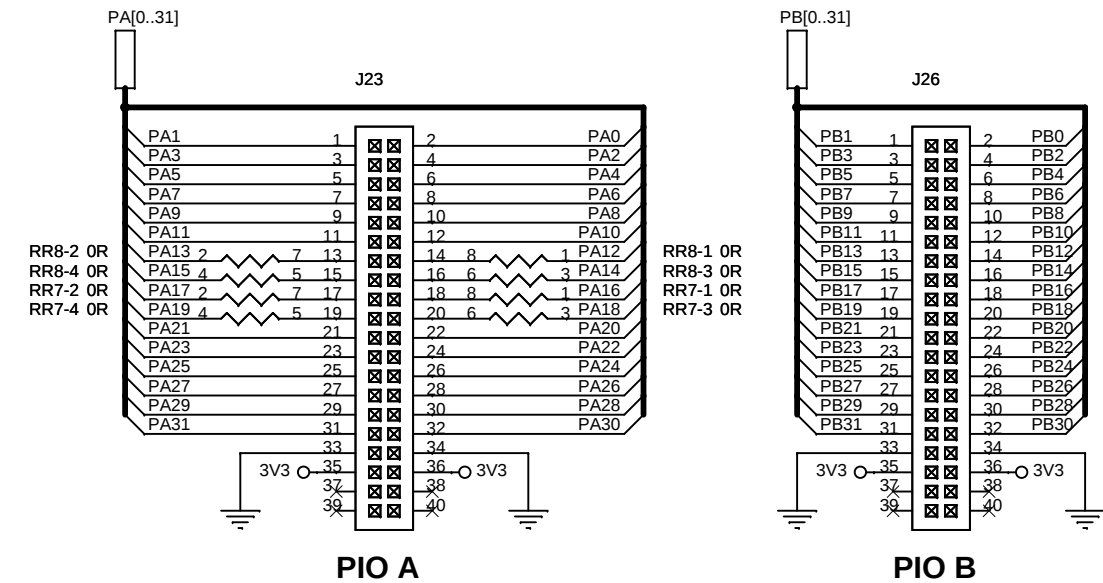
AT91SAM9260-EK
AT91SAM9260-LQFP208

B		JPG	28/08/06		
A	INIT EDIT	JPG	17/10/05		
REV	MODIF.	DES.	DATE	VER.	DATE
SCALE 1/1				REV.	4/8
				B	

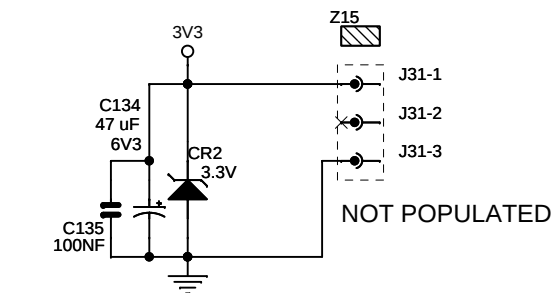
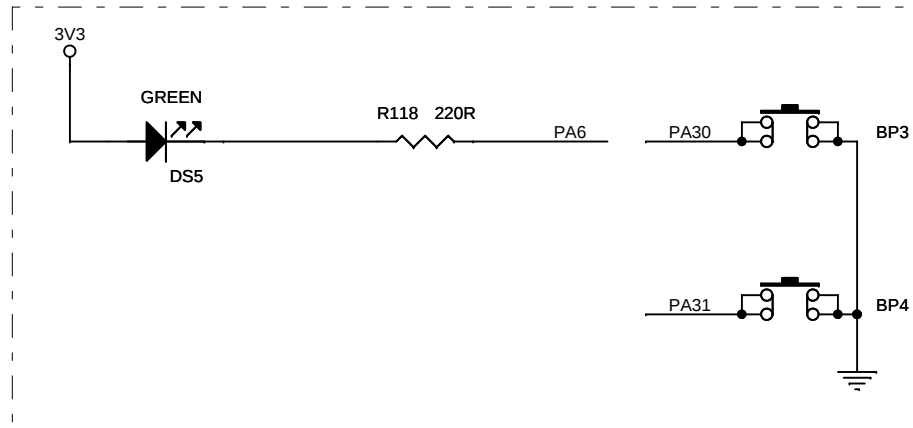
This agreement is our property. Reproduction and publication without our written authorization shall expose offender to legal proceedings.







USER INTERFACE



ATMEL ROUSSET							
AT91SAM9260-EK		REV.	MODIF.	DES.	DATE	VER.	DATE
EXPANSION & UI		SCALE	1/1			REV.	SHEET
						B	8/8



Section 6

Errata

-
- | | | |
|------------|---|---|
| 6.1 | VDD Backup Jumper Selector (J10) | <p>The silkscreen is wrong. The markings for BB and 1V8 are inverted.</p> <p>The marking should be:</p> <ul style="list-style-type: none">■ On J10 pin 1 (square pin): BB.■ On J10 pin 3: 1V8. |
| <hr/> | | |
| 6.2 | JTAGSEL S2 Footprint Selector | <p>The S2 footprint must never be shorted to select a JTAG mode, otherwise the chip can be damaged.</p> <p>By default, the JTAGSEL input pin integrates a pull-down resistor (ICE mode). To select the JTAG mode, connect the JTAGSEL input pin at VDDBU power.</p> |
| <hr/> | | |
| 6.3 | TWI line pullups for Fast Mode operation | <p>In order to use the TWI in Fast Mode (up to 400 Kbits/s), the default 10 KΩ resistors R44 and R45 should be replaced by smaller values (e.g., 2.2 KΩ).</p> <p>Note that there is no need to change the pull-up resistors if the TWI is used in Standard Mode (up to 100 Kbits/s).</p> |
| <hr/> | | |
| 6.4 | AT73C213 clocking | <p>In the present schematics (block diagram p.10 and sheet 1/8, p.26), the MCLK and BCLK sources implementation does not guarantee a correct phase relation as specified in the AT73C213 datasheet.</p> <p>Problem Fix/Workaround:</p> <p>In his own design, the user must make sure the BCLK and MCLK clocks generation implements the timing specified in the AT73C213 datasheet.</p> |
-



Section 7

Revision History

7.1 Revision History

Table 7-1.

Document	Comments	Change Request Ref.
6234A	First issue.	
6234B	New Figure 2-3, "AT91SAM9260-EK Block Diagram" . Inserted Section 3.14, "PIO Usage" . Added new schematics in Section 5 . Added new Section 6, Errata .	3315
6234C	Added errata Section 6.3, "TWI line pullups for Fast Mode operation" .	4086
	Added errata Section 6.4, "AT73C213 clocking"	4227



Atmel Corporation

2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 487-2600

Regional Headquarters

Atmel Europe

Le Krebs
8, rue Jean-Pierre Timbaud
BP 309
78054 Saint-Quentin-en-Yvelines
Cedex
France
Tel: (33) 1-30-60-70-00
Fax: (33) 1-30-60-71-11

Asia

Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimshatsui
East Kowloon
Hong Kong
Tel: (852) 2721-9778
Fax: (852) 2722-1369

Japan

9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
Tel: (81) 3-3523-3551
Fax: (81) 3-3523-7581

Atmel Operations

Memory

2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 436-4314

Microcontrollers

2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 436-4314

La Chantrerie
BP 70602
44306 Nantes Cedex 3, France
Tel: (33) 2-40-18-18-18
Fax: (33) 2-40-18-19-60

ASIC/ASSP/Smart Cards

Zone Industrielle
13106 Rousset Cedex, France
Tel: (33) 4-42-53-60-00
Fax: (33) 4-42-53-60-01

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906, USA
Tel: 1(719) 576-3300
Fax: 1(719) 540-1759

Scottish Enterprise Technology Park
Maxwell Building
East Kilbride G75 0QR, Scotland
Tel: (44) 1355-803-000
Fax: (44) 1355-242-743

RF/Automotive

Theresienstrasse 2
Postfach 3535
74025 Heilbronn, Germany
Tel: (49) 71-31-67-0
Fax: (49) 71-31-67-2340

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906, USA
Tel: 1(719) 576-3300
Fax: 1(719) 540-1759

Biometrics/Imaging/Hi-Rel MPU/ High Speed Converters/RF Datacom

Avenue de Rochepleine
BP 123
38521 Saint-Egreve Cedex, France
Tel: (33) 4-76-58-30-00
Fax: (33) 4-76-58-34-80



Literature Requests

www.atmel.com/literature

Disclaimer: The information in this document is provided in connection with Atmel products. No license, express or implied, by estoppel or otherwise, to any intellectual property right is granted by this document or in connection with the sale of Atmel products. **EXCEPT AS SET FORTH IN ATMEL'S TERMS AND CONDITIONS OF SALE LOCATED ON ATMEL'S WEB SITE, ATMEL ASSUMES NO LIABILITY WHATSOEVER AND DISCLAIMS ANY EXPRESS, IMPLIED OR STATUTORY WARRANTY RELATING TO ITS PRODUCTS INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTY OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT. IN NO EVENT SHALL ATMEL BE LIABLE FOR ANY DIRECT, INDIRECT, CONSEQUENTIAL, PUNITIVE, SPECIAL OR INCIDENTAL DAMAGES (INCLUDING, WITHOUT LIMITATION, DAMAGES FOR LOSS OF PROFITS, BUSINESS INTERRUPTION, OR LOSS OF INFORMATION) ARISING OUT OF THE USE OR INABILITY TO USE THIS DOCUMENT, EVEN IF ATMEL HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.** Atmel makes no representations or warranties with respect to the accuracy or completeness of the contents of this document and reserves the right to make changes to specifications and product descriptions at any time without notice. Atmel does not make any commitment to update the information contained herein. Unless specifically provided otherwise, Atmel products are not suitable for, and shall not be used in, automotive applications. Atmel's products are not intended, authorized, or warranted for use as components in applications intended to support or sustain life.

© 2007 Atmel Corporation. All rights reserved. Atmel®, logo and combinations thereof, Everywhere You Are®, DataFlash® and others are registered trademarks or trademarks of Atmel Corporation or its subsidiaries. ARM®, the ARM Powered® and others are the registered trademarks or trademarks of ARM Ltd. Other terms and product names may be trademarks of others.



Printed on recycled paper.

6234C-ATARM-22-Mar-07