



16-Bit, Ultra-Low Power, Voltage-Output Digital-to-Analog Converters

FEATURES

- 16-Bit Resolution
- 2.7 V to 5.5 V Single-Supply Operation
- Very Low Power: 15 μ W for 3 V Power
- High Accuracy, INL: 1 LSB
- Low Noise: 10 nV/ $\sqrt{\text{Hz}}$
- Fast Settling: 1.0 μ S
- Fast SPI™ Interface, up to 50 MHz
- Reset to Zero-Code
- Schmitt-Trigger Inputs for Direct Optocoupler Interface
- Industry-Standard Pin Configuration

APPLICATIONS

- Portable Equipment
- Automatic Test Equipment
- Industrial Process Control
- Data Acquisition Systems
- Optical Networking

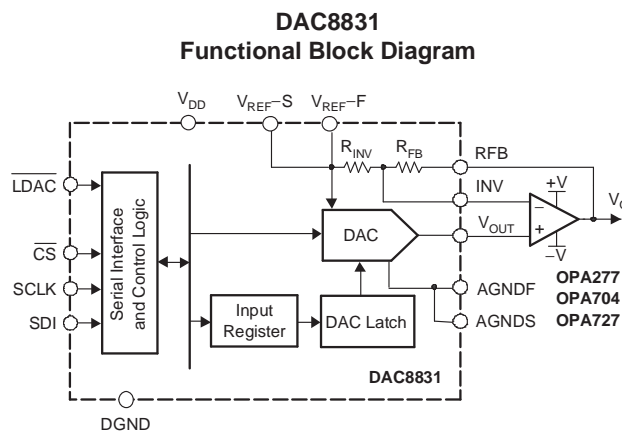
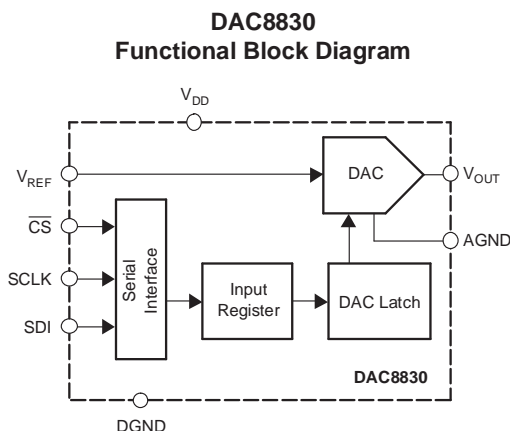
DESCRIPTION

The DAC8830 and DAC8831 are single, 16-bit, serial-input, voltage-output digital-to-analog converters (DACs) operating from a single 3 V to 5 V power supply. These converters provide excellent linearity (1 LSB INL), low glitch, low noise, and fast settling (1.0 μ S to 1/2 LSB of full-scale output) over the specified temperature range of -40°C to $+85^{\circ}\text{C}$. The output is unbuffered, which reduces the power consumption and the error introduced by the buffer.

These parts feature a standard high-speed (clock up to 50 MHz), 3 V or 5 V SPI serial interface to communicate with a DSP or microprocessor.

The DAC8830 output is 0 V to V_{REF} . However, the DAC8831 provides bipolar output ($\pm V_{\text{REF}}$) when working with an external buffer. The DAC8830 and DAC8831 are both reset to zero code after power up. For optimum performance, a set of Kelvin connections to external reference and analog ground input are provided on the DAC8831.

The DAC8830 is available in an SO-8 package, and the DAC8831 in an SO-14 package. Both have industry standard pinouts (see Table 3, the cross-reference table in the Application Information section for details). The DAC8831 is also available in a QFN-14 package.



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION⁽¹⁾

PRODUCT	MINIMUM RELATIVE ACCURACY (LSB)	DIFFERENTIAL NONLINEARITY (LSB)	POWER- ON RESET VALUE	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	PACKAGE- LEAD	PACKAGE DESIGNATOR	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
DAC8830ID	±4	±1	Zero Code	−40°C to +85°C	8830I	SO-8	D	DAC8830ID	Tubes, 75
								DAC8830IDR	Tape and Reel, 2500
DAC8830IBD	±2	±1	Zero Code	−40°C to +85°C	8830I	SO-8	D	DAC8830IBD	Tubes, 75
								DAC8830IBDR	Tape and Reel, 2500
DAC8830ICD	±1	±1	Zero Code	−40°C to +85°C	8830I	SO-8	D	DAC8830ICD	Tubes, 75
								DAC8830ICDR	Tape and Reel, 2500
DAC8831ID	±4	±1	Zero Code	−40°C to +85°C	8831I	SO-14	D	DAC8831ID	Tube, 50
								DAC8831IDR	Tape and Reel, 2500
DAC8831IBD	±2	±1	Zero Code	−40°C to +85°C	8831I	SO-14	D	DAC8831IBD	Tube, 50
								DAC8831IBDR	Tape and Reel, 2500
DAC8831ICD	±1	±1	Zero Code	−40°C to +85°C	8831I	SO-14	D	DAC8831ICD	Tube, 50
								DAC8831ICDR	Tape and Reel, 2500
DAC8831IRGY	±4	±1	Zero Code	−40°C to +85°C	8831I	QFN-14	RGY	DAC8831IRGYT	Tape and Reel, 250
								DAC8831IRGYR	Tape and Reel, 1000
DAC8831IBRGY	±2	±1	Zero Code	−40°C to +85°C	8831I	QFN-14	RGY	DAC8831IBRGYT	Tape and Reel, 250
								DAC8831IBRGYR	Tape and Reel, 1000
DAC8831ICRGY	±1	±1	Zero Code	−40°C to +85°C	8831I	QFN-14	RGY	DAC8831ICRGYT	Tape and Reel, 250
								DAC8831ICRGYR	Tape and Reel, 1000

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this data sheet, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		DAC8830, DAC8831	UNIT
V_{DD} to AGND		−0.3 to +7	V
Digital input voltage to DGND		−0.3 to $V_{DD} + 0.3$	V
V_{OUT} to AGND		−0.3 to $V_{DD} + 0.3$	V
AGND, AGNDF, AGNDS to DGND		−0.3 to +0.3	V
Operating temperature range		−40 to +85	°C
Storage temperature range		−65 to +150	°C
Junction temperature range (T_J max)		+150	°C
Power dissipation		$(T_J \text{ max} - T_A) / \theta_{JA}$	W
Thermal impedance, θ_{JA}	QFN-14	54.9	°C/W
	SO-8	136.9	°C/W
	SO-14	66.6	°C/W

(1) Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

All specifications at $T_A = T_{MIN}$ to T_{MAX} , $V_{DD} = +3\text{ V}$ or $V_{DD} = +5\text{ V}$, $V_{REF} = +2.5\text{ V}$ unless otherwise noted.

PARAMETER		CONDITIONS	DAC8830, DAC8831			UNIT
			MIN	TYP	MAX	
STATIC PERFORMANCE						
Resolution			16			bits
Linearity error	DAC8830ICD, DAC8831ICD, DAC8831ICRGY		±0.5 ±1			LSB
	DAC8830IBD, DAC8831IBD, DAC8831IBRGY		±0.5 ±2			
	DAC8830ID, DAC8831ID, DAC8831IRGY		±0.5 ±4			
Differential linearity error		All grades	±0.5 ±1			LSB
Gain error		T _A = +25°C	±1 ±5			LSB
		T _A = −40°C to +85°C	±7			
Gain drift			±0.1			ppm/°C
Zero code error		T _A = +25°C	±0.25 ±1			LSB
		T _A = −40°C to +85°C	±2			
Zero code drift			±0.05			ppm/°C
OUTPUT CHARACTERISTICS						
Voltage output ⁽¹⁾	All devices	Unipolar operation	0 +V _{REF}			V
	DAC8831 only	Bipolar operation	−V _{REF} +V _{REF}			V
Output impedance			6.25			kΩ
Settling time		To 1/2 LSB of FS, C _L = 10 pF	1			μs
Slew rate ⁽²⁾		C _L = 10 pF	25			V/μs
Digital-to-analog glitch		1 LSB change around major carry	35			nV-s
Digital feedthrough ⁽³⁾			0.2			nV-s
Output noise	DAC8830	T _A = +25°C	10			nV/√Hz
	DAC8831		18			
Power-supply rejection		V _{DD} varies ±10%	±1			LSB
Bipolar resistor matching	DAC8831 only	R _{FB} / R _{INV}	1			Ω/Ω
		Ratio error	±0.0015 ±0.0076			%
Bipolar zero error	DAC8831 only	T _A = +25°C	±0.25 ±5			LSB
		T _A = −40°C to +85°C	±7			
Bipolar zero drift		DAC8831 only	±0.2			ppm/°C

(1) The DAC8830 output is unipolar (0 V to $+V_{REF}$). The DAC8831 output is bipolar ($\pm V_{REF}$) when it connects to an external buffer (see the [Bipolar Output Operation](#) section for details).

(2) Slew rate is measured from 10% to 90% of transition when the output changes from 0 to full-scale.

(3) Digital feedthrough is defined as the impulse injected into the analog output from the digital input. It is measured when the DAC output does not change; \overline{CS} is held high, while SCLK and DIN signals are toggled.

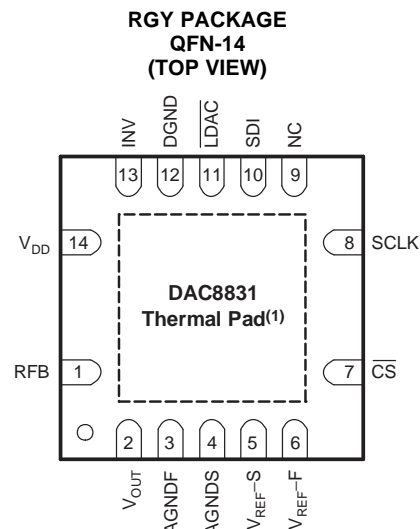
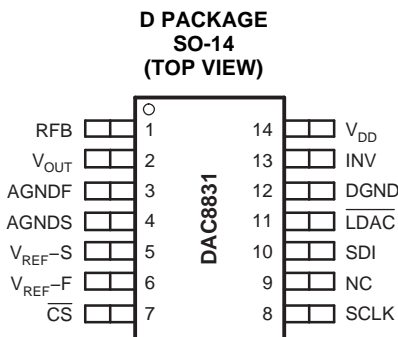
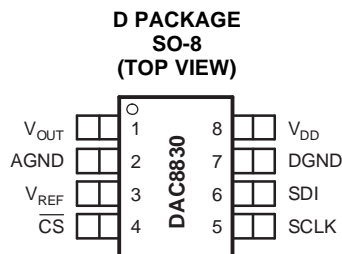
ELECTRICAL CHARACTERISTICS (continued)

All specifications at $T_A = T_{MIN}$ to T_{MAX} , $V_{DD} = +3\text{ V}$ or $V_{DD} = +5\text{ V}$, $V_{REF} = +2.5\text{ V}$ unless otherwise noted.

PARAMETER		CONDITIONS	DAC8830, DAC8831			UNIT
			MIN	TYP	MAX	
REFERENCE INPUT						
Reference input voltage range			1.25		V _{DD}	V
Reference input impedance ⁽⁴⁾		Unipolar mode	9			kΩ
		Bipolar mode, DAC8831	7.5			
Reference –3dB bandwidth, BW		Code = FFFFh		1.3		MHz
Reference feedthrough		Code = 0000h, V _{REF} = 1 V _{PP} at 100 kHz		1		mV
Signal-to-noise ratio, SNR				92		dB
Reference input capacitance		Code = 0000h		75		pF
		Code = FFFFh		120		
DIGITAL INPUTS						
V _{IL}	Input low voltage	V _{DD} = 2.7 V			0.6	V
		V _{DD} = 5 V			0.8	
V _{IH}	Input high voltage	V _{DD} = 2.7 V	2.1			V
		V _{DD} = 5 V	2.4			
Input current					±1	μA
Input capacitance					10	pF
Hysteresis voltage				0.4		V
POWER SUPPLY						
V _{DD}	Power-supply voltage		2.7		5.5	V
I _{DD}	Power-supply current	V _{DD} = 3 V		5	20	μA
		V _{DD} = 5 V		5	20	
Power		V _{DD} = 3 V		15	60	μW
		V _{DD} = 5 V		25	100	
TEMPERATURE RANGE						
Specified performance			–40		+85	°C

(4) Reference input resistance is code-dependent, minimum at 8555h.

PIN CONFIGURATIONS (NOT TO SCALE)



NOTE: (1) Exposed thermal pad in the QFN package must be connected to analog ground.

TERMINAL FUNCTIONS

TERMINAL NO.	NAME	DESCRIPTION
DAC8830		
1	V _{OUT}	Analog output of DAC
2	AGND	Analog ground
3	V _{REF}	Voltage reference input
4	\overline{CS}	Chip select input (active low). Data are not clocked into SDI unless \overline{CS} is low
5	SCLK	Serial clock input
6	SDI	Serial data input. Data are latched into input register on the rising edge of SCLK.
7	DGND	Digital ground
8	V _{DD}	Analog power supply, +3 V to +5 V
DAC8831		
1	RFB	Feedback resistor. Connect to the output of external operational amplifier in bipolar mode.
2	V _{OUT}	Analog output of DAC
3	AGNDF	Analog ground (Force)
4	AGNDS	Analog ground (Sense)
5	V _{REF-S}	Voltage reference input (Sense). Connect to external voltage reference
6	V _{REF-F}	Voltage reference input (Force). Connect to external voltage reference
7	\overline{CS}	Chip select input (active low). Data are not clocked into SDI unless \overline{CS} is low.
8	SCLK	Serial clock input.
9	NC	No internal connection
10	SDI	Serial data input. Data are latched into input register on the rising edge of SCLK.
11	\overline{LDAC}	Load DAC control input. Active low. When \overline{LDAC} is Low, the DAC latch is simultaneously updated with the content of the input register.
12	DGND	Digital ground
13	INV	Junction point of internal scaling resistors. Connect to external operational amplifier inverting input in bipolar mode.
14	V _{DD}	Analog power supply, +3 V to +5 V.

Case1: $\overline{\text{LDAC}}$ tied to LOW

Timing diagram for Case 1 shows the relationship between $\overline{\text{CS}}$, SCLK, SDI, and $\overline{\text{LDAC}}$. $\overline{\text{LDAC}}$ is tied to LOW. The diagram illustrates the sequence of operations: $\overline{\text{CS}}$ is pulled down, followed by a delay t_{Delay} , then a lead time t_{Lead} . SCLK is then enabled for a duration t_{sck} with a setup time t_{wsck} before the first data bit (BIT 15, MSB) is shifted out. The data is shifted out in 16-bit words (BIT 15, BIT 14, BIT 13...1, BIT 0). The setup time t_{su} and hold time t_{ho} for the data are indicated. After the last data bit, there is a delay t_{Lag} before the DAC is updated. The update time t_{DCLK} is shown, followed by a delay t_{td} before the DAC output is updated. A legend indicates that hatched areas represent "Don't Care".

Case2: $\overline{\text{LDAC}}$ Active

Timing diagram for Case 2 shows the relationship between $\overline{\text{CS}}$, SCLK, SDI, and $\overline{\text{LDAC}}$. $\overline{\text{LDAC}}$ is active. The diagram illustrates the sequence of operations: $\overline{\text{CS}}$ is pulled down, followed by a delay t_{Delay} , then a lead time t_{Lead} . SCLK is then enabled for a duration t_{sck} with a setup time t_{wsck} before the first data bit (BIT 15, MSB) is shifted out. The data is shifted out in 16-bit words (BIT 15, BIT 14, BIT 13...1, BIT 0). The setup time t_{su} and hold time t_{ho} for the data are indicated. After the last data bit, there is a delay t_{Lag} before the DAC is updated. The update time t_{DCLK} is shown, followed by a delay t_{td} before the DAC output is updated. A legend indicates that hatched areas represent "Don't Care".

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Product Folder Link(s): [DAC8830](#) [DAC8831](#)

TIMING CHARACTERISTICS: $V_{DD} = +5\text{ V}^{(1)(2)}$

At -40°C to $+85^{\circ}\text{C}$, unless otherwise noted.

PARAMETER		MIN	MAX	UNIT
t_{sck}	SCLK period	20		ns
t_{wsck}	SCLK high or low time	10		ns
t_{Delay}	Delay from SCLK high to $\overline{\text{CS}}$ low	10		ns
t_{Lead}	$\overline{\text{CS}}$ enable lead time	10		ns
t_{Lag}	$\overline{\text{CS}}$ enable lag time	10		ns
t_{DSCLK}	Delay from $\overline{\text{CS}}$ high to SCLK high	10		ns
t_{td}	$\overline{\text{CS}}$ high between active period	30		ns
t_{su}	Data setup time (input)	10		ns
t_{ho}	Data hold time (input)	0		ns
t_{WLDAC}	$\overline{\text{LDAC}}$ width	30		ns
t_{DLDAC}	Delay from $\overline{\text{CS}}$ high to $\overline{\text{LDAC}}$ low	30		ns
	V_{DD} high to $\overline{\text{CS}}$ low (power-up delay)	10		μs

(1) Assured by design. Not production tested.

(2) Sample tested during the initial release and after any redesign or process changes that may affect this parameter.

TIMING CHARACTERISTICS: $V_{DD} = +3\text{ V}^{(1)(2)}$

At -40°C to $+85^{\circ}\text{C}$, unless otherwise noted.

PARAMETER		MIN	MAX	UNIT
t_{sck}	SCLK period	20		ns
t_{wsck}	SCLK high or low time	10		ns
t_{Delay}	Delay from SCLK high to $\overline{\text{CS}}$ low	10		ns
t_{Lead}	$\overline{\text{CS}}$ enable lead time	10		ns
t_{Lag}	$\overline{\text{CS}}$ enable lag time	10		ns
t_{DSCLK}	Delay from $\overline{\text{CS}}$ high to SCLK high	10		ns
t_{td}	$\overline{\text{CS}}$ high between active period	30		ns
t_{su}	Data setup time (input)	10		ns
t_{ho}	Data hold time (input)	0		ns
t_{WLDAC}	$\overline{\text{LDAC}}$ width	30		ns
t_{DLDAC}	Delay from $\overline{\text{CS}}$ high to $\overline{\text{LDAC}}$ low	30		ns
	V_{DD} high to $\overline{\text{CS}}$ low (power-up delay)	10		μs

(1) Assured by design. Not production tested.

(2) Sample tested during the initial release and after any redesign or process changes that may affect this parameter.

TYPICAL CHARACTERISTICS: $V_{DD} = +5\text{ V}$

At $T_A = +25^\circ\text{C}$ and $V_{REF} = +2.5\text{ V}$, unless otherwise noted.

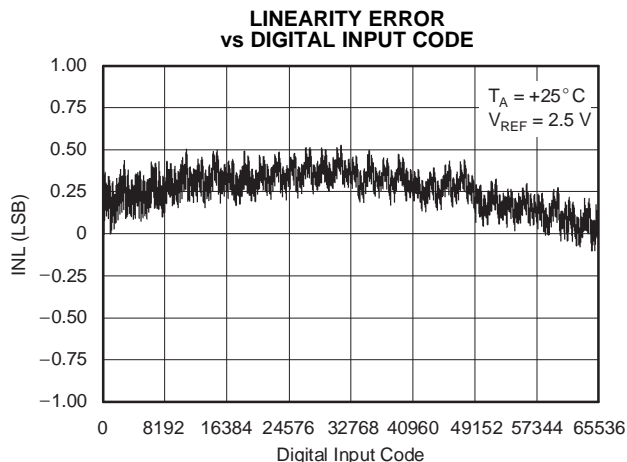


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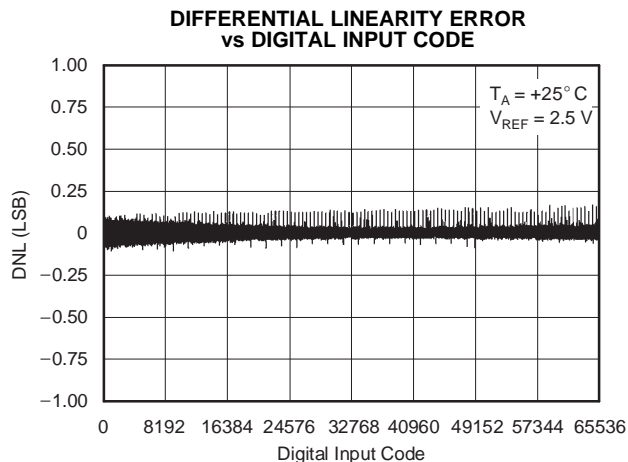


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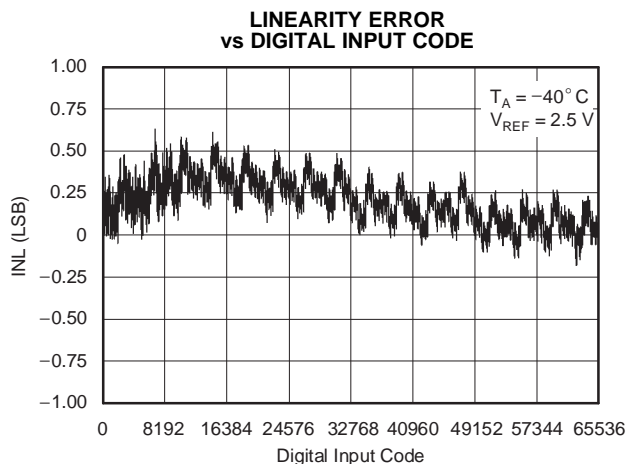


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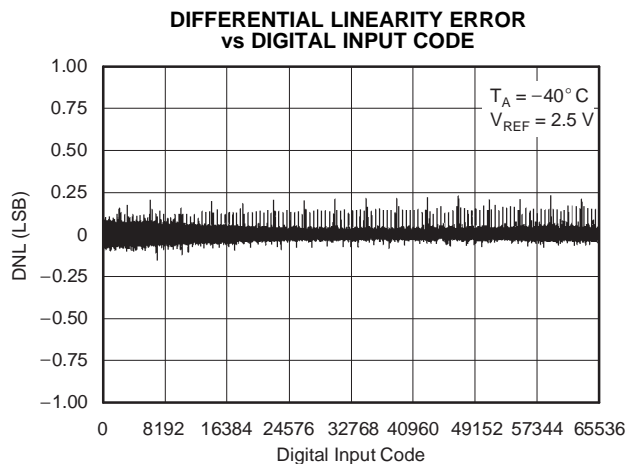


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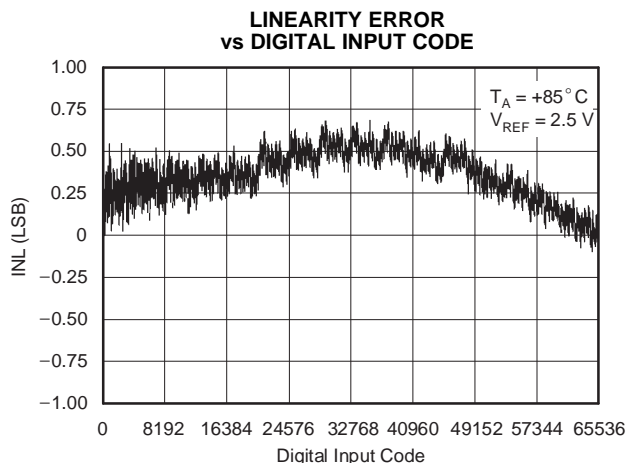


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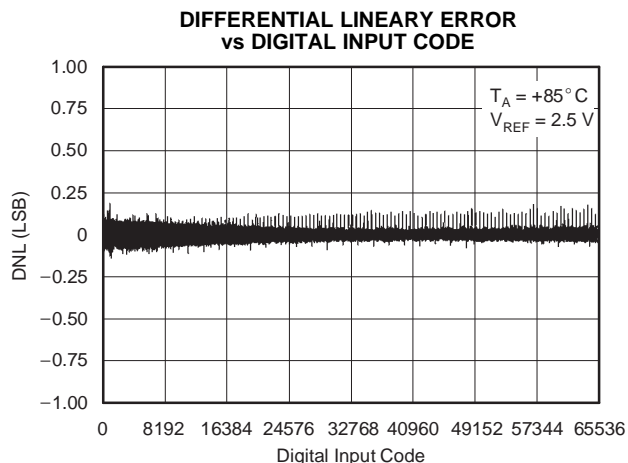


Figure 8.

TYPICAL CHARACTERISTICS: $V_{DD} = +5\text{ V}$ (continued)

At $T_A = +25^\circ\text{C}$ and $V_{REF} = +2.5\text{ V}$, unless otherwise noted.

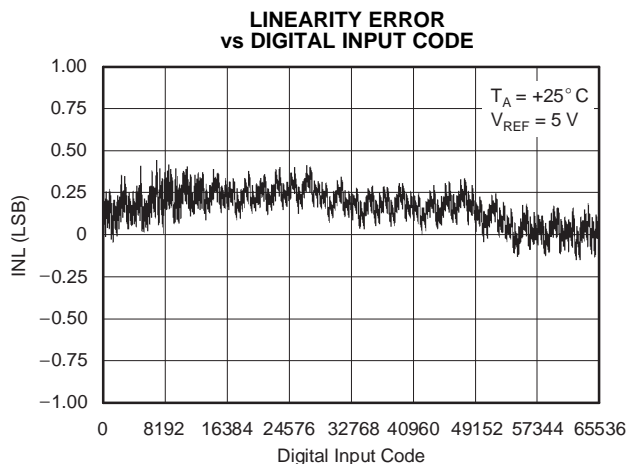


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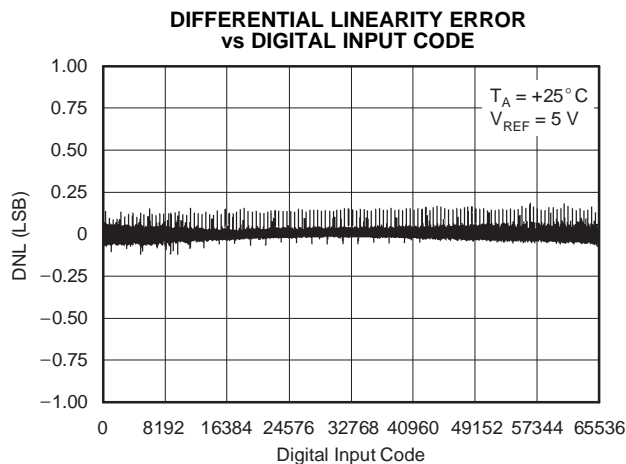


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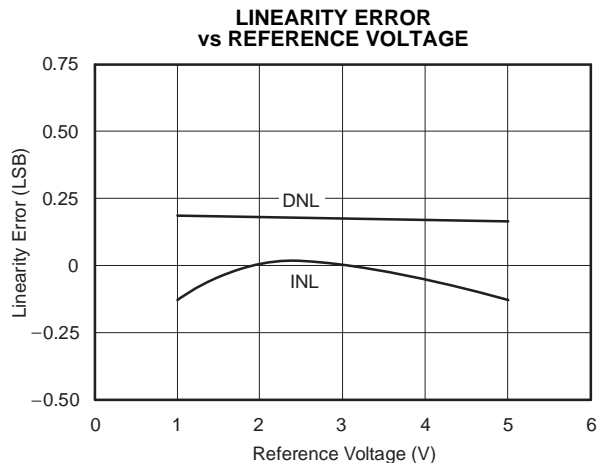


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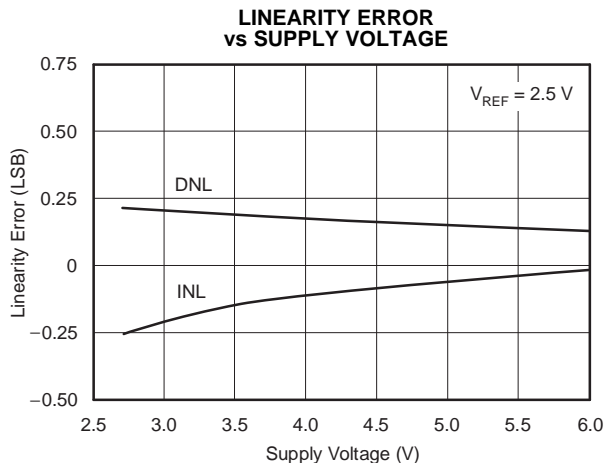


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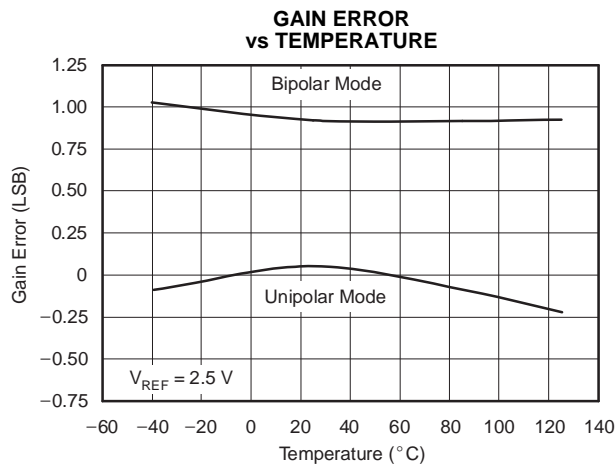


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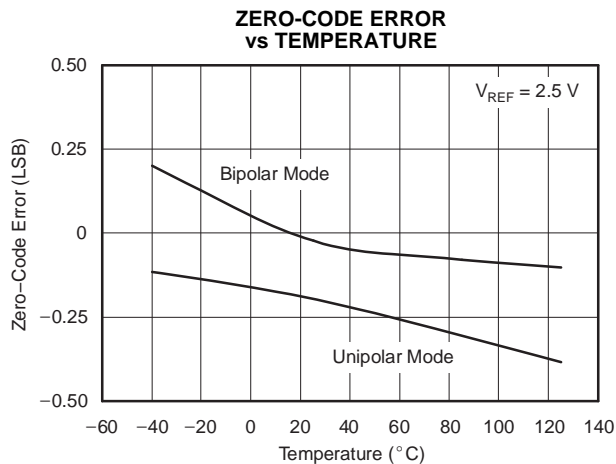


Figure 14.

TYPICAL CHARACTERISTICS: $V_{DD} = +5\text{ V}$ (continued)

At $T_A = +25^\circ\text{C}$ and $V_{REF} = +2.5\text{ V}$, unless otherwise noted.

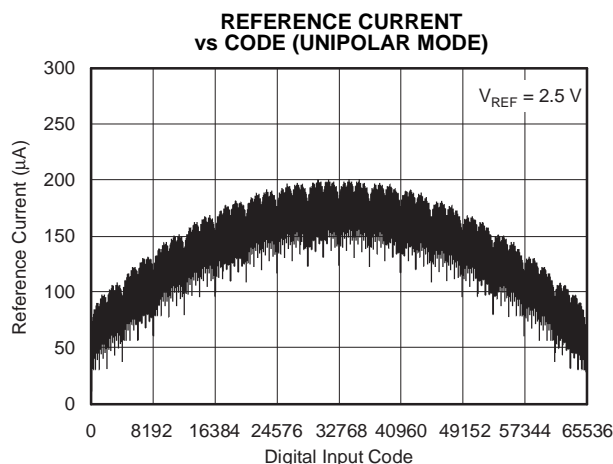


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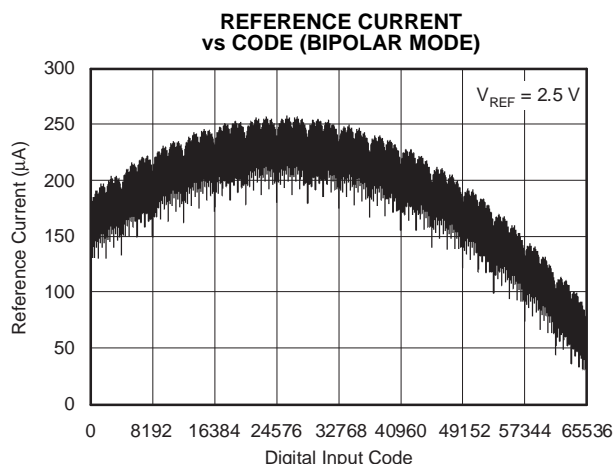


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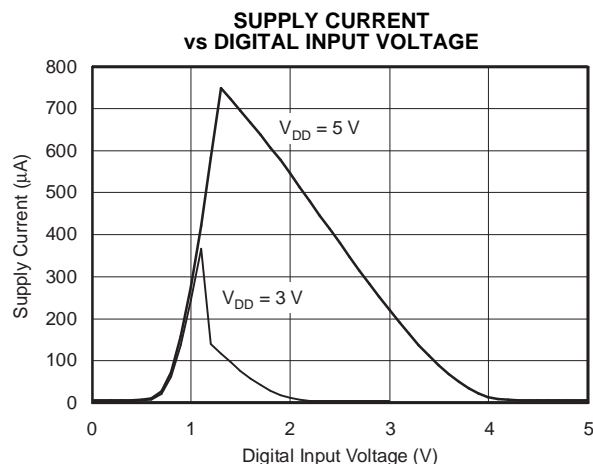


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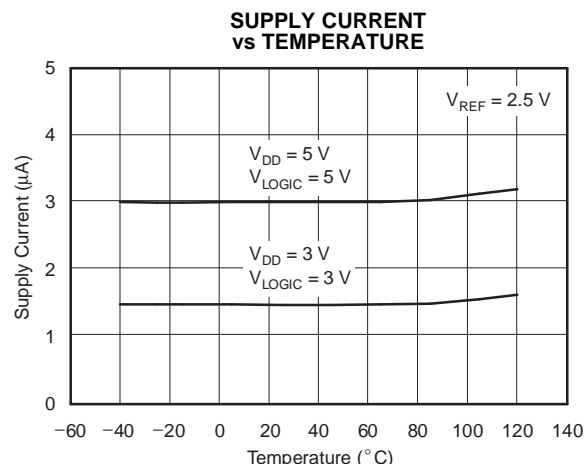


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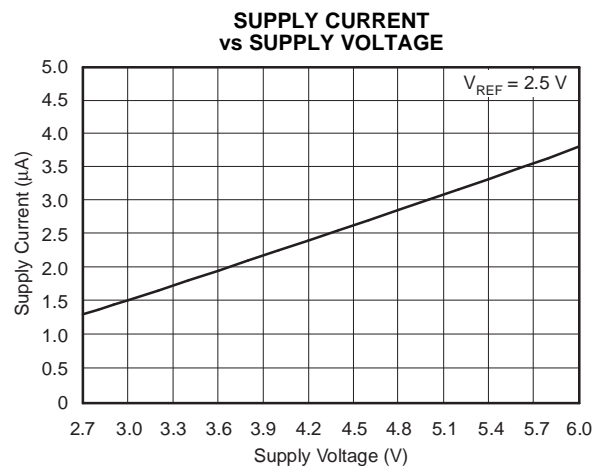


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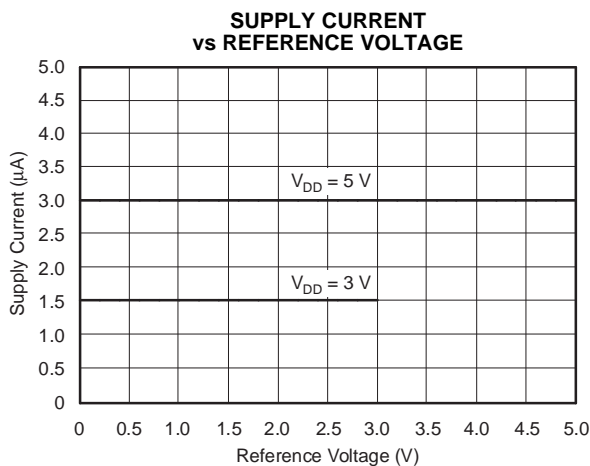


Figure 20.

TYPICAL CHARACTERISTICS: $V_{DD} = +5\text{ V}$ (continued)

At $T_A = +25^\circ\text{C}$ and $V_{REF} = +2.5\text{ V}$, unless otherwise noted.

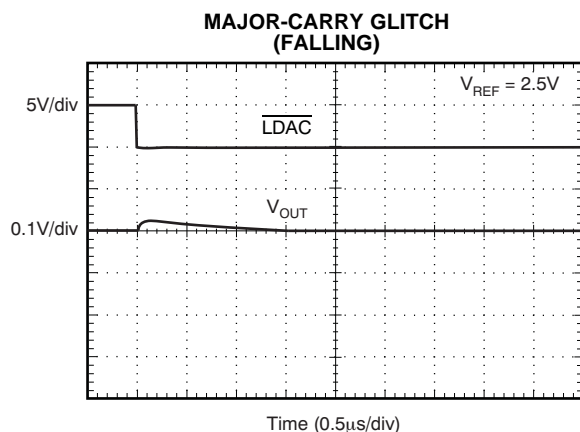


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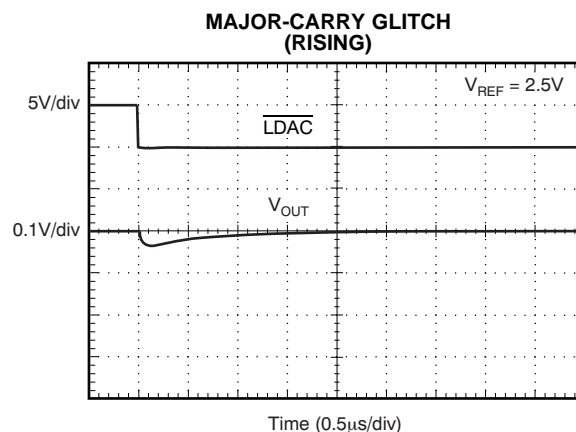


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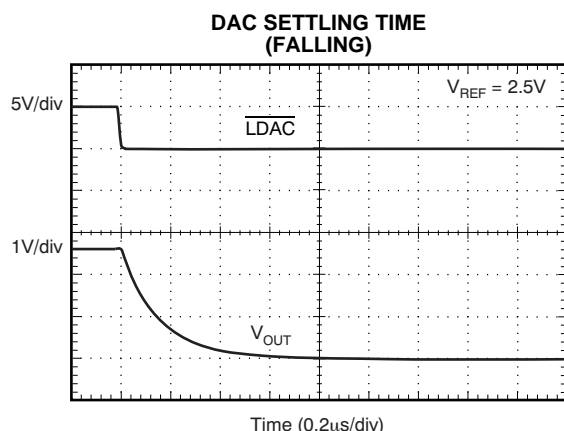


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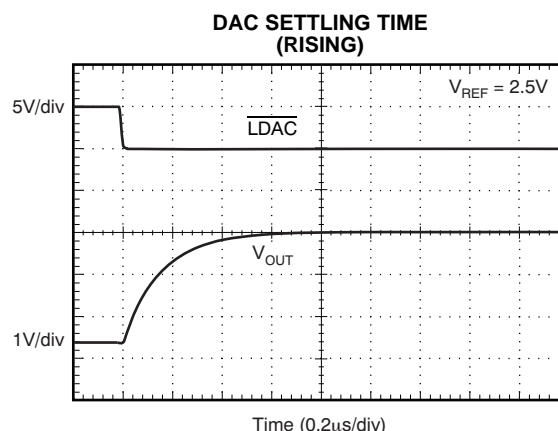


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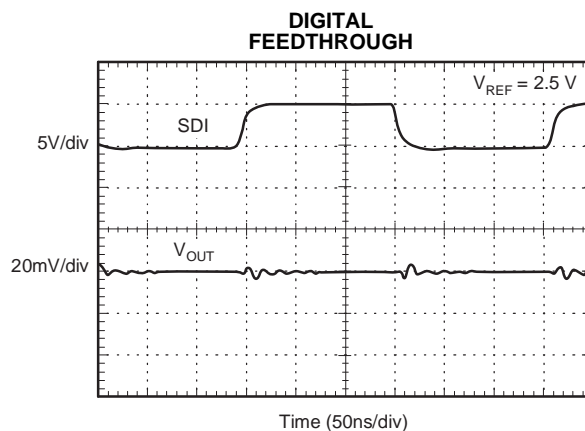


Figure 25.

TYPICAL CHARACTERISTICS: $V_{DD} = +3\text{ V}$

At $T_A = +25^\circ\text{C}$ and $V_{REF} = +2.5\text{ V}$, unless otherwise noted.

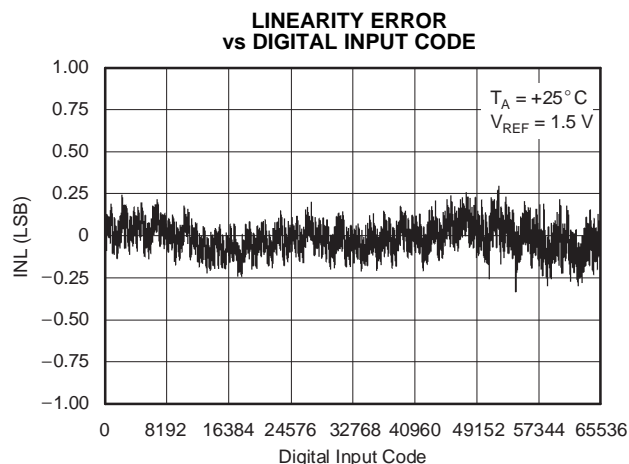


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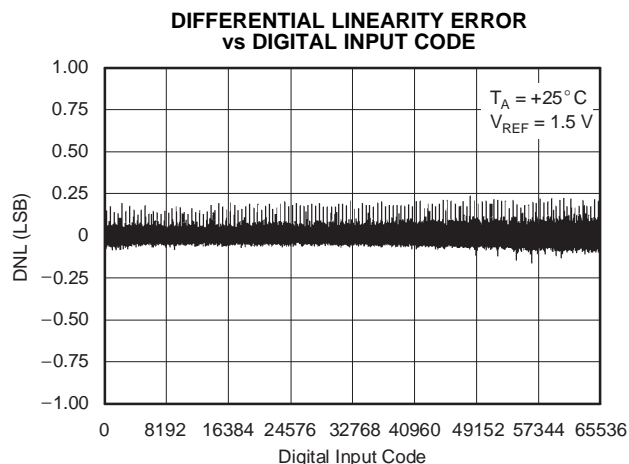


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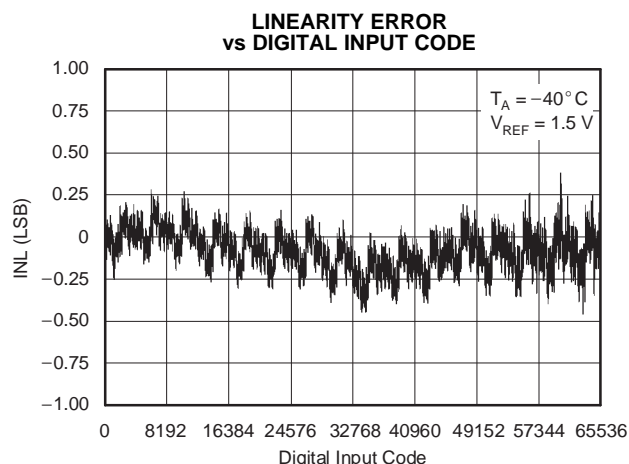


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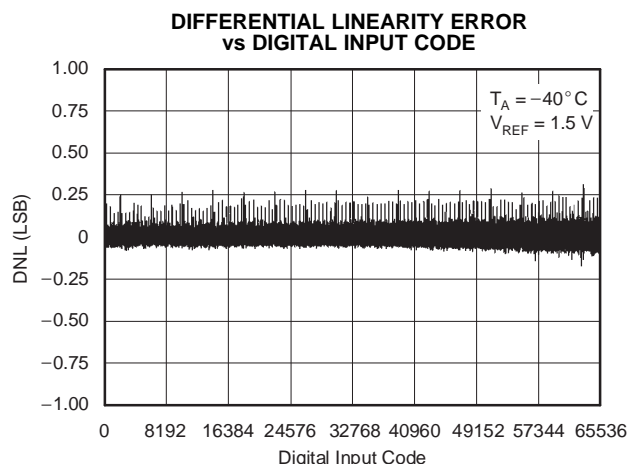


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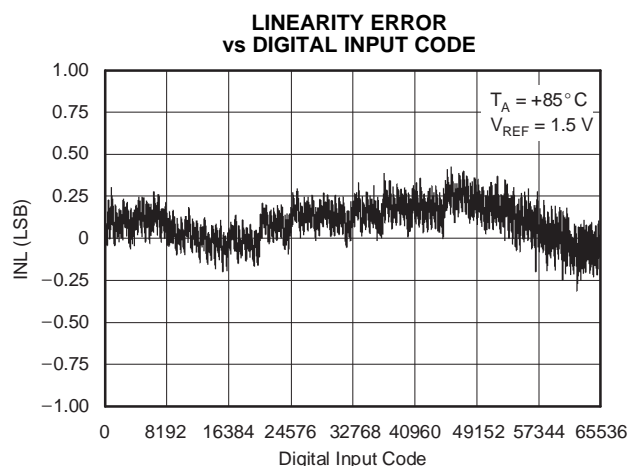


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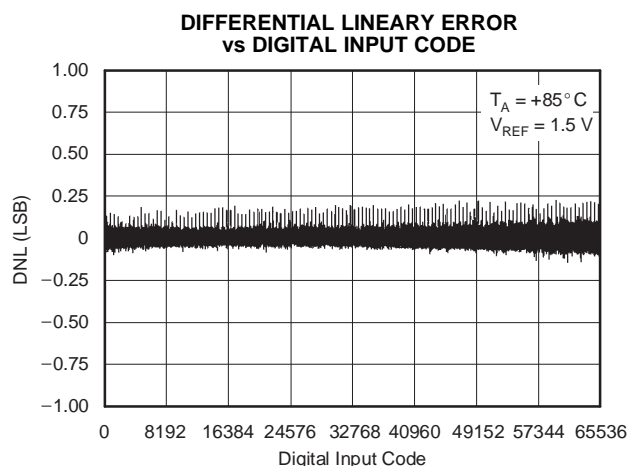


Figure 31.

TYPICAL CHARACTERISTICS: $V_{DD} = +3\text{ V}$ (continued)

At $T_A = +25^\circ\text{C}$ and $V_{REF} = +2.5\text{ V}$, unless otherwise noted.

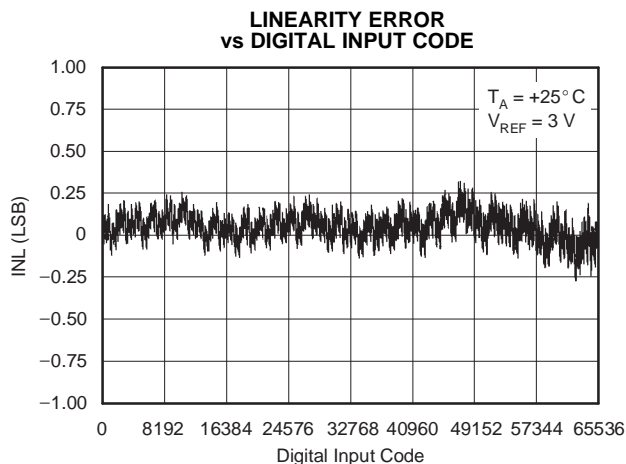


Figure 32.

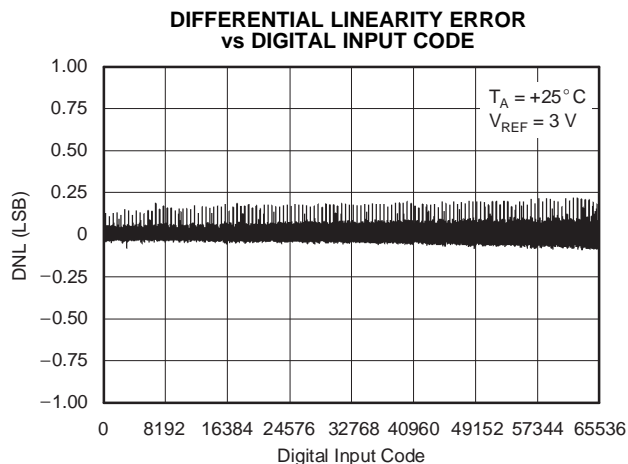


Figure 33.

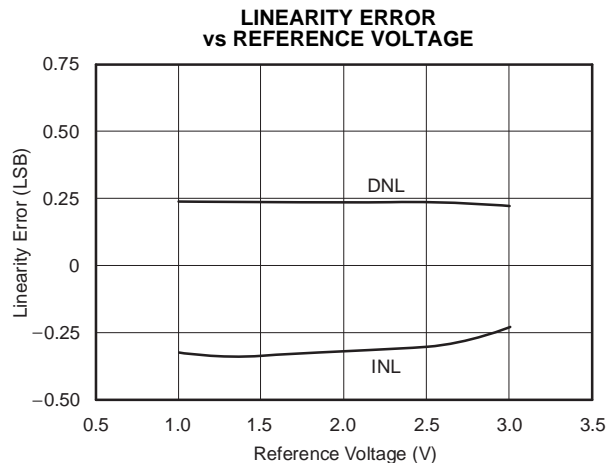


Figure 34.

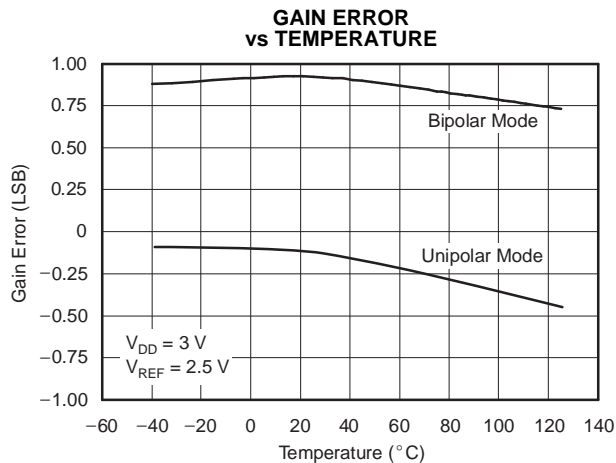


Figure 35.

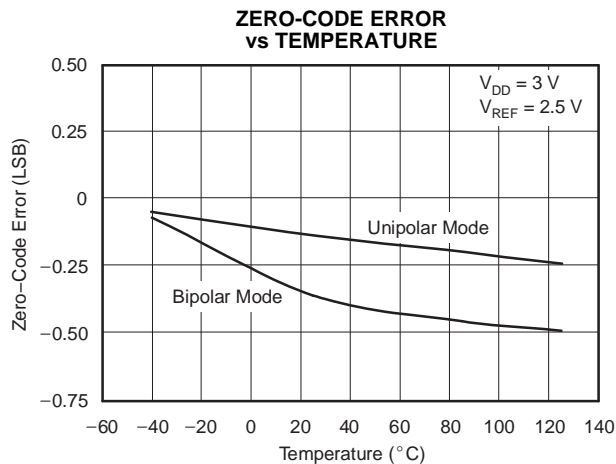


Figure 36.

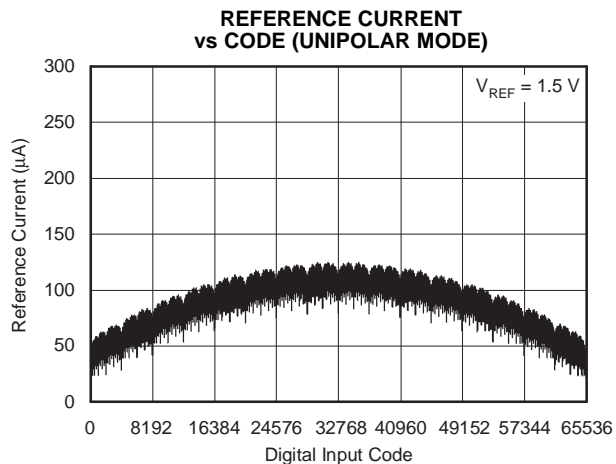


Figure 37.

TYPICAL CHARACTERISTICS: $V_{DD} = +3\text{ V}$ (continued)

At $T_A = +25^\circ\text{C}$ and $V_{REF} = +2.5\text{ V}$, unless otherwise noted.

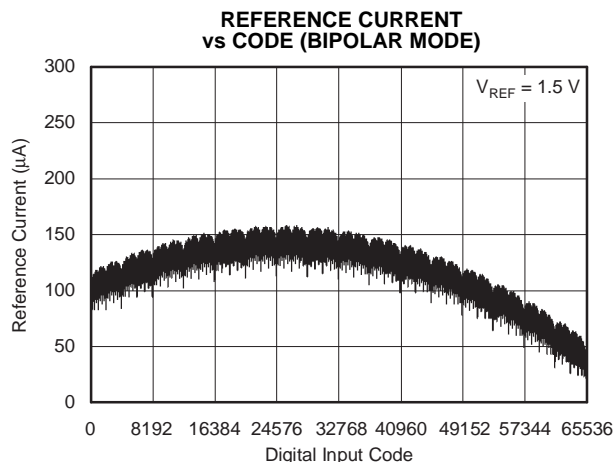


Figure 38.

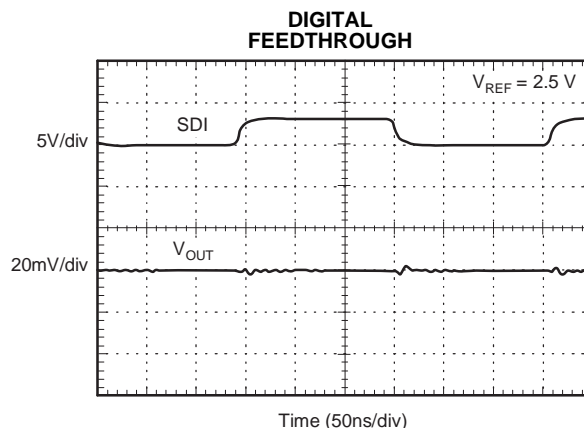


Figure 39.

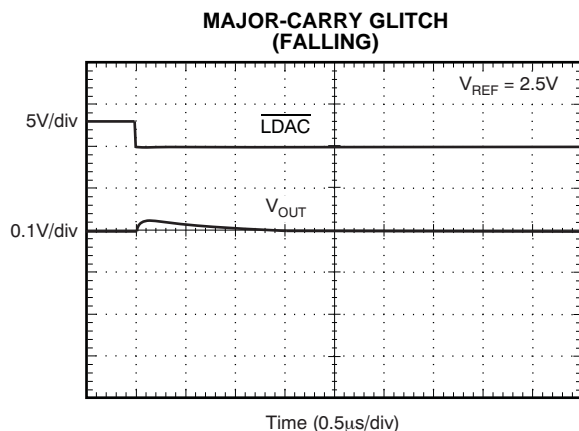


Figure 40.

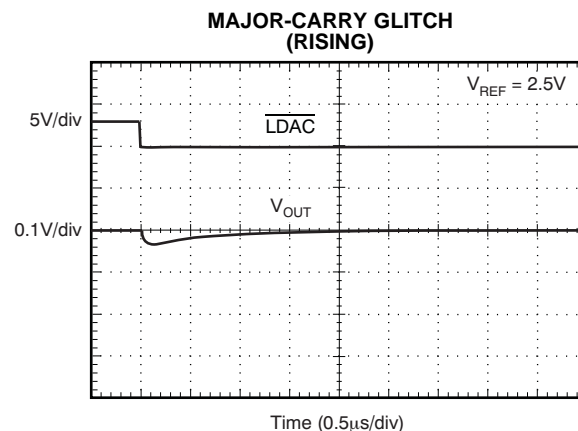


Figure 41.

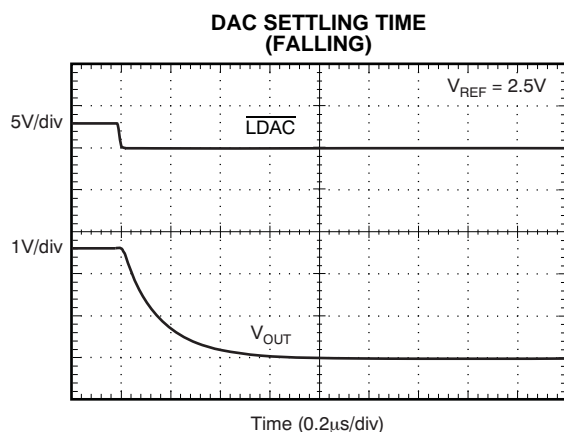


Figure 42.

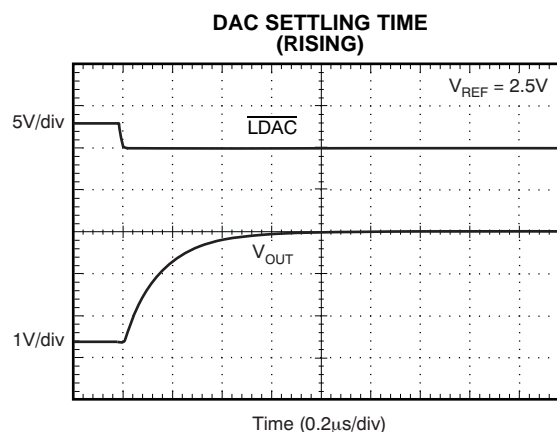


Figure 43.

THEORY OF OPERATION

GENERAL DESCRIPTION

The DAC8830 and DAC8831 are single, 16-bit, serial-input, voltage-output DACs. They operate from a single

supply ranging from 2.7 V to 5 V, and typically consume 5 μ A. Data are written to these devices in a 16-bit word format, via an SPI serial interface. To ensure a known power-up state, these parts are designed with a power-on reset function. The DAC8830 and DAC8831 are reset to zero code. In unipolar mode, the DAC8830 and DAC8831 are reset to 0 V, and in bipolar mode, the DAC8831 is reset to $-V_{REF}$. Kelvin sense connections for the reference and analog ground are included on the DAC8831.

DIGITAL-TO-ANALOG SECTIONS

The DAC architecture for both devices consists of two matched DAC sections and is segmented. A simplified circuit diagram is shown in Figure 44. The four MSBs of the 16-bit data word are decoded to drive 15 switches, E1 to E15. Each of these switches connects one of 15 matched resistors to either AGND or V_{REF} . The remaining 12 bits of the data word drive switches S0 to S11 of a 12-bit voltage mode R-2R ladder network.

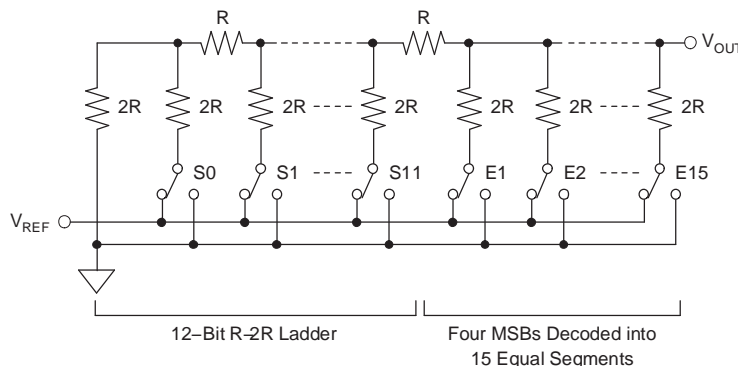


Figure 44. DAC Architecture

OUTPUT RANGE

The output of the DAC is

$$V_{OUT} = (V_{REF} \times \text{Code})/65536.$$

Where *Code* is the decimal data word loaded to the DAC latch.

POWER-ON RESET

Both devices have a power-on reset function to ensure the output is at a known state upon power-up. In the DAC8830 and DAC8831, at power-up, the DAC latch and Input Registers contain all 0s until new data are loaded from the input serial shift register. Therefore, after power-up, the output from pin V_{OUT} of the DAC8830 is 0 V. The output from pin V_{OUT} of the DAC8831 is 0 V in unipolar mode and $-V_{REF}$ in bipolar mode.

However, the serial register of the DAC8830 and DAC8831 is not cleared on power-up, so its contents are undefined. When loading data initially to the device, 16 bits or more should be loaded to prevent erroneous data appearing on the output. If more than 16 bits are loaded, the last 16 are kept; if less than 16 are loaded, bits will remain from the previous word. If the device must be interfaced with data shorter than 16 bits, the data should be padded with 0s at the LSBs.

Serial Interface

The digital interface is a standard 3-wire connection compatible with SPI, QSPI™, Microwire™, and TI DSP interfaces, which can operate at speeds up to 50 M-bits/sec. The data transfer is framed by \overline{CS} , the chip select signal. The DAC works as a bus slave. The bus master generates the synchronize clock, SCLK, and initiates the transmission. When \overline{CS} is high, the DAC is not accessed, and the clock SCLK and serial input data SDI are ignored. The bus master accesses the DAC by driving pin \overline{CS} low. Immediately following the high-to-low transition of \overline{CS} , the serial input data on pin SDI is shifted out from the bus master synchronously on the falling edge of SCLK, and latched on the rising edge of SCLK into the input shift register, MSB first. The low-to-high transition of \overline{CS} transfers the contents of the input shift register to the input register. All data registers are 16-bit. It takes 16 clocks of SCLK to transfer one data word to the parts. To complete a whole data word, \overline{CS} must go high immediately after 16 SCLKs are clocked in. If more than 16 SCLKs are applied during the low state of \overline{CS} , the last 16 bits are transferred to the input register on the rising edge of \overline{CS} . However, if \overline{CS} is not kept low during the entire 16 SCLK cycles, data is corrupted. In this case, reload the DAC with a new 16-bit word.

In the DAC8830, the contents of the input register are transferred into the DAC latch immediately when the input register is loaded, and the DAC output is updated at the same time.

The DAC8831 has an \overline{LDAC} pin allowing the DAC latch to be updated asynchronously by bringing \overline{LDAC} low after \overline{CS} goes high. In this case, \overline{LDAC} must be maintained high while \overline{CS} is low. If \overline{LDAC} is tied permanently low, the DAC latch is updated immediately after the input register is loaded (caused by the low-to-high transition of \overline{CS}).

APPLICATION INFORMATION

Unipolar Output Operation

These DACs are capable of driving unbuffered loads of 60 kΩ. Unbuffered operation results in low supply current (typically 5 μA) and a low offset error. The DAC8830 provides a unipolar output swing ranging from 0 V to V_{REF} . The DAC8831 can be configured to output both unipolar and bipolar voltages. Figure 45 and Figure 46 show a typical unipolar output voltage circuit for each device, respectively. The code table for this mode of operation is shown in Table 1.

Table 1. Unipolar Code

DAC LATCH CONTENTS		ANALOG OUTPUT
MSB	LSB	
1111	1111 1111 1111	$V_{REF} \times (65,535/65,536)$
1000	0000 0000 0000	$V_{REF} \times (32,768/65,536) = 1/2 V_{REF}$
0000	0000 0000 0001	$V_{REF} \times (1/65,536)$
0000	0000 0000 0000	0 V

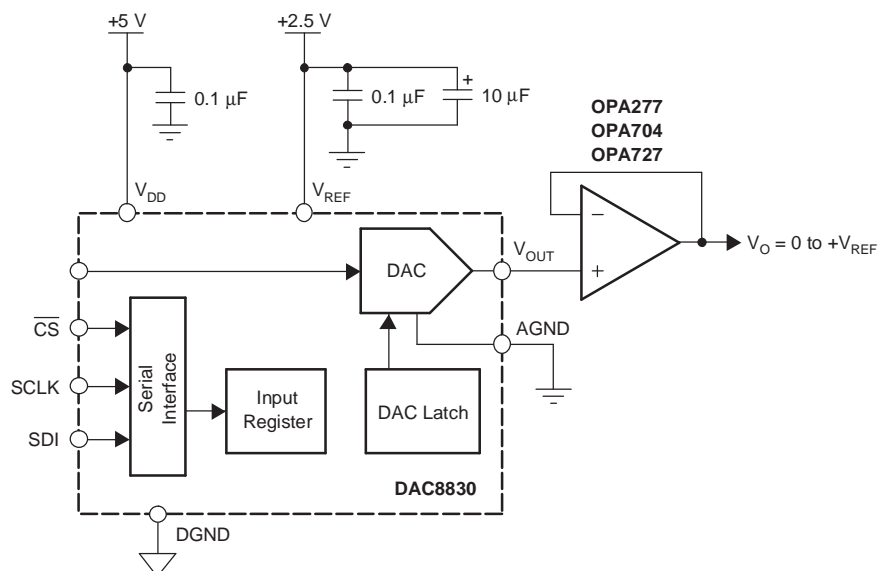


Figure 45. Unipolar Output Mode of DAC8830

Product Folder Link(s): [DAC8830](#) [DAC8831](#)

Bipolar Output Operation

With the aid of an external operational amplifier, the DAC8831 may be configured to provide a bipolar voltage output. A typical circuit of such an operation is shown in Figure 47. The matched bipolar offset resistors R_{FB} and R_{INV} are connected to an external operational amplifier to achieve this bipolar output swing; typically, $R_{FB} = R_{INV} = 28\text{ k}\Omega$.

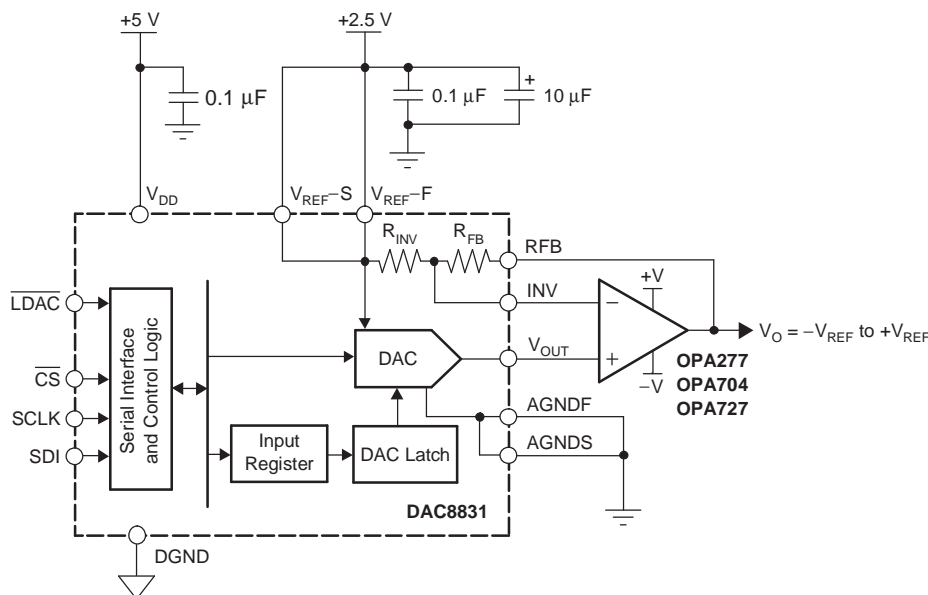


Figure 47. Bipolar Output Mode of DAC8831

Table 2 shows the transfer function for this output operating mode. The DAC8831 also provides a set of Kelvin connections to the analog ground and external reference inputs.

Table 2. Bipolar Code

DAC LATCH CONTENTS		ANALOG OUTPUT
MSB	LSB	
1111 1111 1111 1111		$+V_{REF} \times (32,767/32,768)$
1000 0000 0000 0001		$+V_{REF} \times (1/32,768)$
1000 0000 0000 0000		0 V
0111 1111 1111 1111		$-V_{REF} \times (1/32,768)$
0000 0000 0000 0000		$-V_{REF} \times (32,768/32,768) = -V_{REF}$

Assuming a perfect reference, the worst-case output voltage may be calculated from the following equation:

Bipolar Mode Worst-Case Output

$$V_{OUT_BIP} = \frac{\left[(V_{OUT_UNI} + V_{OS}) (2 + RD) - V_{REF}(1 + RD) \right]}{1 + \left(\frac{2 + RD}{A} \right)}$$

Where:

V_{OS} = External operational amplifier input offset voltage

$RD = R_{FB}$ and R_{IN} resistor matching error

A = Operational amplifier open-loop gain

Output Amplifier Selection

For bipolar mode, a precision amplifier should be used, supplied from a dual power supply. This provides the $\pm V_{REF}$ output.

In a single-supply application, selection of a suitable operational amplifier may be more difficult because the output swing of the amplifier does not usually include the negative rail; in this case, AGND. This output swing can result in some degradation of the specified performance unless the application does not use codes near 0.

The selected operational amplifier needs to have low-offset voltage (the DAC LSB is 38 μ V with a 2.5 V reference), eliminating the need for output offset trims. Input bias current should also be low because the bias current multiplied by the DAC output impedance (approximately 6.25 k Ω) adds to the zero-code error.

Rail-to-rail input and output performance are required. For fast settling, the slew rate of the operational amplifier should not impede the settling time of the DAC. Output impedance of the DAC is constant and code-independent, but in order to minimize gain errors the input impedance of the output amplifier should be as high as possible. The amplifier should also have a 3 dB bandwidth of 1 MHz or greater. The amplifier adds another time constant to the system, thus increasing the settling time of the output. A higher 3 dB amplifier bandwidth results in a shorter effective settling time of the combined DAC and amplifier.

Reference and Ground

Since the input impedance is code-dependent, the reference pin should be driven from a low impedance source. The DAC8830 and DAC8831 operate with a voltage reference ranging from 1.25 V to V_{DD} . References below 1.25 V result in reduced accuracy.

The DAC full-scale output voltage is determined by the reference. [Table 1](#) and [Table 2](#) outline the analog output voltage for particular digital codes.

For optimum performance, Kelvin sense connections are provided on the DAC8831. If the application does not require separate force and sense lines, they should be tied together close to the package to minimize voltage drops between the package leads and the internal die.

Power Supply and Reference Bypassing

For accurate high-resolution performance, it is recommended that the reference and supply pins be bypassed with a 10 μ F tantalum capacitor in parallel with a 0.1 μ F ceramic capacitor.

CROSS-REFERENCE

The DAC8830 and DAC8831 have an industry-standard pinout configuration (see [Table 3](#)).

Table 3. Cross-Reference

MODEL	INL (LSB)	DNL (LSB)	POWER-ON RESET TO	TEMPERATURE RANGE	PACKAGE DESCRIPTION	PACKAGE OPTION	CROSS REFERENCE
DAC8830ICD	±1	±1	Zero Code	–40°C to +85°C	8-Lead Small Outline IC	SO-8	AD5541CR, MAX541AESA
DAC8830IBD	±2	±1	Zero Code	–40°C to +85°C	8-Lead Small Outline IC	SO-8	AD5541BR, MAX541BESA
DAC8830ID	±4	±1	Zero Code	–40°C to +85°C	8-Lead Small Outline IC	SO-8	AD5541AR, MAX541CESA
N/A	±1	±1	Zero Code	–40°C to +85°C	8-Lead Plastic DIP	PDIP-8	MAX541AEPA
N/A	±2	±1	Zero Code	–40°C to +85°C	8-Lead Plastic DIP	PDIP-8	MAX541BEPA
N/A	±4	±1	Zero Code	–40°C to +85°C	8-Lead Plastic DIP	PDIP-8	MAX541CEPA
N/A	±1	±1	Zero Code	0°C to +70°C	8-Lead Small Outline IC	SO-8	AD5541LR
N/A	±2	±1.5	Zero Code	0°C to +70°C	8-Lead Small Outline IC	SO-8	AD5541JR
N/A	±1	±1	Zero Code	0°C to +70°C	8-Lead Plastic DIP	PDIP-8	MAX541AEPA
N/A	±2	±1	Zero Code	0°C to +70°C	8-Lead Plastic DIP	PDIP-8	MAX541BEPA
N/A	±4	±1	Zero Code	0°C to +70°C	8-Lead Plastic DIP	PDIP-8	MAX541CEPA
DAC8831ICD	±1	±1	Zero Code	–40°C to +85°C	14-Lead Small Outline IC	SO-14	AD5542CR, MAX542AESD
DAC8831IBD	±2	±1	Zero Code	–40°C to +85°C	14-Lead Small Outline IC	SO-14	AD5542BR, MAX542BESD
DAC8831ID	±4	±1	Zero Code	–40°C to +85°C	14-Lead Small Outline IC	SO-14	AD5542AR, MAX542CESD
DAC8831ICRGY	±1	±1	Zero Code	–40°C to +85°C	14-Lead QFN	QFN-14	N/A
DAC8831IBRGY	±2	±1	Zero Code	–40°C to +85°C	14-Lead QFN	QFN-14	N/A
DAC8831IRGY	±4	±1	Zero Code	–40°C to +85°C	14-Lead QFN	QFN-14	N/A
N/A	±1	±1	Zero Code	–40°C to +85°C	14-Lead Plastic DIP	PDIP-14	MAX542ACPD
N/A	±2	±1	Zero Code	–40°C to +85°C	14-Lead Plastic DIP	PDIP-14	MAX542BCPD
N/A	±4	±1	Zero Code	–40°C to +85°C	14-Lead Plastic DIP	PDIP-14	MAX542CCPD
N/A	±1	±1	Zero Code	0°C to +70°C	14-Lead Small Outline IC	SO-14	AD5542LR
N/A	±2	±1.5	Zero Code	0°C to +70°C	14-Lead Small Outline IC	SO-14	AD5542JR
N/A	±1	±1	Zero Code	0°C to +70°C	14-Lead Small Outline IC	SO-14	MAX542AEPD
N/A	±2	±1	Zero Code	0°C to +70°C	14-Lead Small Outline IC	SO-14	MAX542BEPD
N/A	±4	±1	Zero Code	0°C to +70°C	14-Lead Small Outline IC	SO-14	MAX542CEPD

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DAC8830IBD	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DAC 8830I
DAC8830IBD.A	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DAC 8830I
DAC8830IBDR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DAC 8830I
DAC8830IBDR.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DAC 8830I
DAC8830IBDRG4.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DAC 8830I
DAC8830ICD	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DAC 8830I
DAC8830ICD.A	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DAC 8830I
DAC8830ICDG4	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DAC 8830I
DAC8830ICDR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DAC 8830I
DAC8830ICDR.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DAC 8830I
DAC8830ICDRG4.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DAC 8830I
DAC8830ID	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DAC 8830I
DAC8830ID.A	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DAC 8830I
DAC8830IDR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DAC 8830I
DAC8830IDR.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DAC 8830I
DAC8830IDRG4.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DAC 8830I
DAC8831IBD	Active	Production	SOIC (D) 14	50 TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DAC8831I

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DAC8831IBD.A	Active	Production	SOIC (D) 14	50 TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DAC8831I
DAC8831IBDG4.A	Active	Production	SOIC (D) 14	50 TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DAC8831I
DAC8831IBDR	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DAC8831I
DAC8831IBDR.A	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DAC8831I
DAC8831ICD	Active	Production	SOIC (D) 14	50 TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DAC8831I
DAC8831ICD.A	Active	Production	SOIC (D) 14	50 TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DAC8831I
DAC8831ICDR	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DAC8831I
DAC8831ICDR.A	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DAC8831I
DAC8831ICDRG4.A	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DAC8831I
DAC8831ICRGYT	Active	Production	VQFN (RGY) 14	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BKE
DAC8831ICRGYT.A	Active	Production	VQFN (RGY) 14	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BKE
DAC8831ID	Active	Production	SOIC (D) 14	50 TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DAC8831I
DAC8831ID.A	Active	Production	SOIC (D) 14	50 TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DAC8831I
DAC8831IDG4	Active	Production	SOIC (D) 14	50 TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DAC8831I
DAC8831IDR	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DAC8831I
DAC8831IDR.A	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DAC8831I

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF DAC8830, DAC8831 :

- Enhanced Product : [DAC8830-EP](#), [DAC8831-EP](#)

NOTE: Qualified Version Definitions:

- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC8830IBDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
DAC8830ICDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
DAC8830IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
DAC8831IBDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
DAC8831ICDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
DAC8831ICRGYT	VQFN	RGY	14	250	180.0	12.4	3.85	3.85	1.35	8.0	12.0	Q1
DAC8831IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

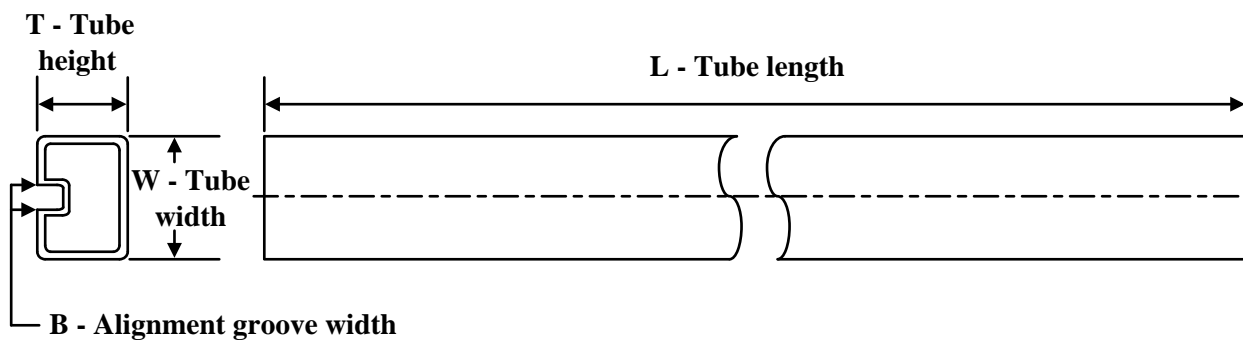
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC8830IBDR	SOIC	D	8	2500	350.0	350.0	43.0
DAC8830ICDR	SOIC	D	8	2500	350.0	350.0	43.0
DAC8830IDR	SOIC	D	8	2500	350.0	350.0	43.0
DAC8831IBDR	SOIC	D	14	2500	350.0	350.0	43.0
DAC8831ICDR	SOIC	D	14	2500	350.0	350.0	43.0
DAC8831ICRGYT	VQFN	RGY	14	250	210.0	185.0	35.0
DAC8831IDR	SOIC	D	14	2500	350.0	350.0	43.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
DAC8830IBD	D	SOIC	8	75	505.46	6.76	3810	4
DAC8830IBD.A	D	SOIC	8	75	505.46	6.76	3810	4
DAC8830ICD	D	SOIC	8	75	505.46	6.76	3810	4
DAC8830ICD.A	D	SOIC	8	75	505.46	6.76	3810	4
DAC8830ICDG4	D	SOIC	8	75	505.46	6.76	3810	4
DAC8830ID	D	SOIC	8	75	505.46	6.76	3810	4
DAC8830ID.A	D	SOIC	8	75	505.46	6.76	3810	4
DAC8831IBD	D	SOIC	14	50	505.46	6.76	3810	4
DAC8831IBD.A	D	SOIC	14	50	505.46	6.76	3810	4
DAC8831IBDG4.A	D	SOIC	14	50	505.46	6.76	3810	4
DAC8831ICD	D	SOIC	14	50	505.46	6.76	3810	4
DAC8831ICD.A	D	SOIC	14	50	505.46	6.76	3810	4
DAC8831ID	D	SOIC	14	50	505.46	6.76	3810	4
DAC8831ID.A	D	SOIC	14	50	505.46	6.76	3810	4
DAC8831IDG4	D	SOIC	14	50	505.46	6.76	3810	4



D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

D0014A**PACKAGE OUTLINE****SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



4220718/A 09/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

EXAMPLE BOARD LAYOUT

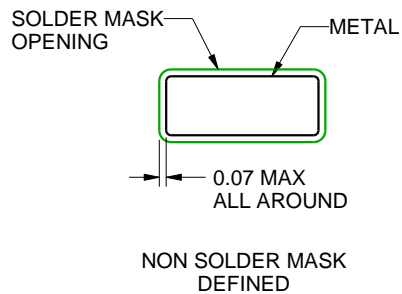
D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

RGY 14

VQFN - 1 mm max height

3.5 x 3.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4231541/A



VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



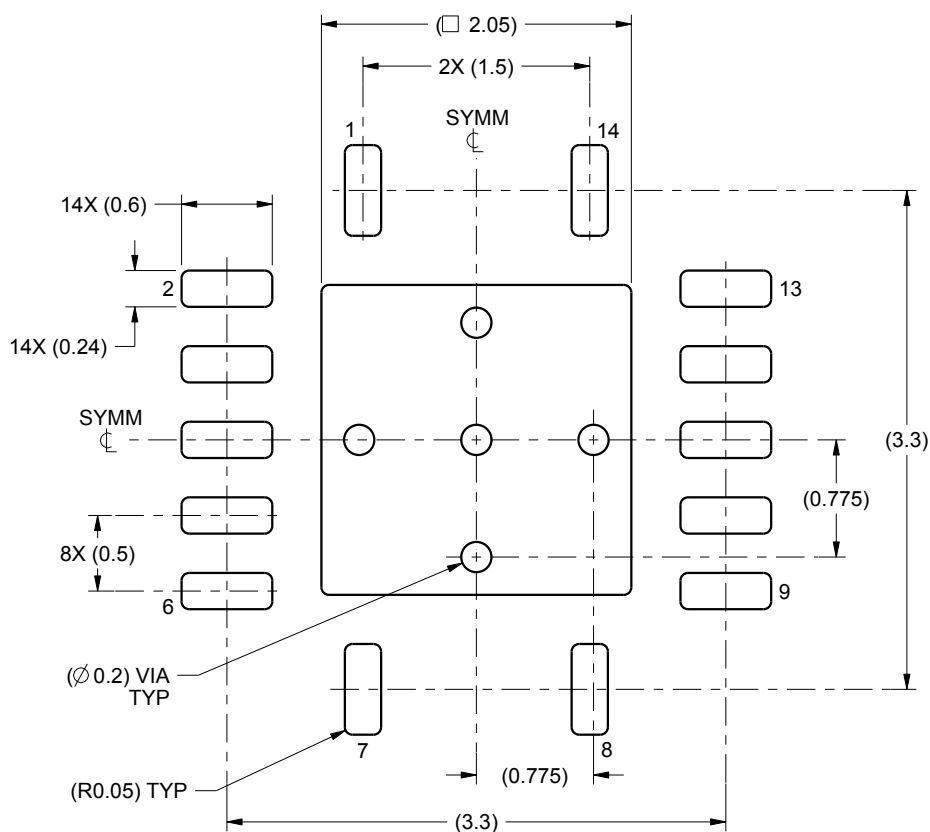
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

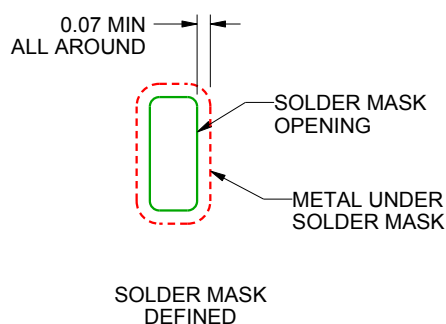
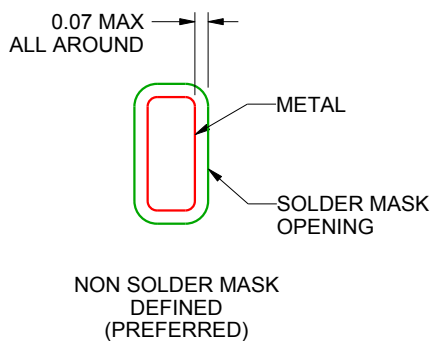
RGY0014A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

4219040/A 09/2015

NOTES: (continued)

- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slue271).

EXAMPLE STENCIL DESIGN

RGY0014A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
80% PRINTED SOLDER COVERAGE BY AREA
SCALE:20X

4219040/A 09/2015

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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