4-channel PWM driver for CD and MD use

BH6512FS / BH6513FS

The BH6512FS/BH6513FS are 4-channel PWM drivers for driving the motors and actuators in CD and MD players. MOSFET output stages are employed to keep power consumption down, and a charge pump circuit is included to multiply the VG voltage.

●Applications

CD and MD players (portable units)

●Features

1) Four power MOS H-bridges.
2) Charge pump (×3).
3) PWM input.
4) Low on-resistance.
5) Low power consumption.
6) Compact SSOP-A32 package.

●Absolute maximum ratings (Ta = 25°C)

Parameter	Symbol	Limits	Unit
H-bridge power supply voltage	VM	9	V
Control circuit power supply voltage	V_{DD}	9	V
Pre-driver power supply voltage	VG (pin18)	12	V
Driver output current	I_O (ch3, ch4) I_O (ch1, ch2)	500 300*1	mA
Power dissipation	Pd	850*2	mW
Operating temperature	Topr	−20～+85	℃
Storage temperature	Tstg	−55～+150	℃

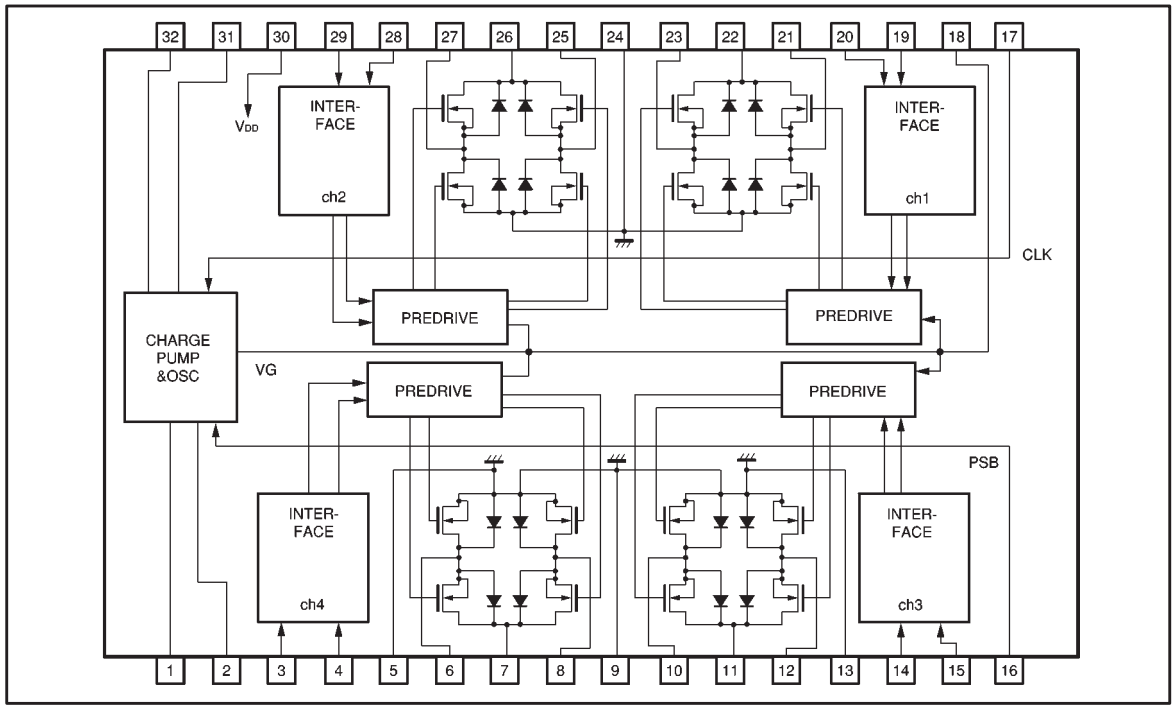
*1 500ms.
*2 Reduced by 6.8mW for each increase in Ta of 1℃ over 25℃.

●Recommended operating conditions (Ta = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
H-bridge power supply voltage	VM	1.6	2.5	5.5	V
Control circuit power supply voltage	V_{DD}	2.4 2.7*3	3.0	5.5	V
Pre-driver power supply voltage	VG (pin18)	VM+3.0	9	11.5	V
Ambient temperature	Ta	−35	25	85	℃
Pulse input frequency	f_{IN}	−	176.4	200	kHz

*3 When VG is supplied externally.

●Block diagram



●Pin descriptions

Pin No.	Pin name	Function	Pin No.	Pin name	Function
1	C2M	Negative connection pin for charge pump capacitor 2	17	CLK	Synchronous clock input
			18	VG	Charge pump output
2	C2P	Positive connection pin for charge pump capacitor 2	19	IN1R	Channel 1 reverse input
			20	IN1F	Channel 1 forward input
3	IN4R	Channel 4 reverse input	21	OUT1F	Channel 1 forward output
4	IN4F	Channel 4 forward input	22	VM1	Channel 1 power block power supply
5	GND4	Channel 4 GND and pre block GND	23	OUT1R	Channel 1 reverse output
6	OUT4F	Channel 4 forward output	24	GND12	Channels 1 and 2 power GND
7	VM4	Channel 4 power block power supply	25	OUT2R	Channel 2 reverse output
8	OUT4R	Channel 4 reverse output	26	VM2	Channel 2 power block power supply
9	GND34	Channels 3 and 4 power GND	27	OUT2F	Channel 2 forward output
10	OUT3R	Channel 3 reverse output	28	IN2F	Channel 2 forward input
11	VM3	Channel 3 power block power supply	29	IN2R	Channel 2 reverse input
12	OUT3F	Channel 3 forward output	30	VDD	Pre block power supply
13	GND3	Channel 3 power GND	31	C1M	Negative connection pin for charge pump capacitor 1
14	IN3F	Channel 3 forward input			
15	IN3R	Channel 3 reverse input	32	C1P	Positive connection pin for charge pump capacitor 1
16	PSB	Power off			

●Input / output circuits

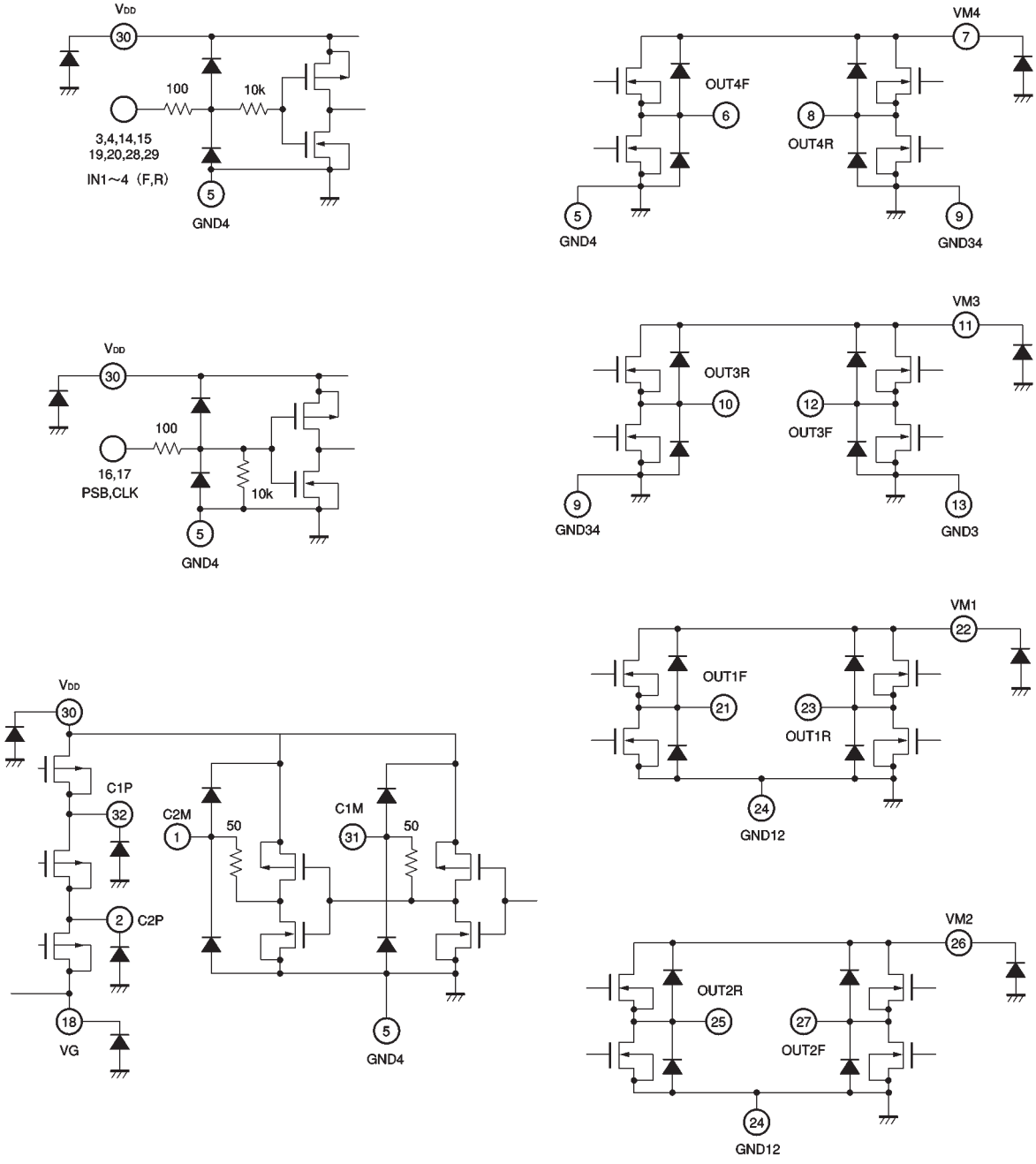


Fig.1

●Electrical characteristics (unless otherwise noted, Ta = 25°C, VM = 2.5V, V_{DD} = 3V, VG is the internally pumped output, f_{IN} = 176kHz, and RL = 8Ω −47μH)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
〈H-bridge power supply current〉						
No input	IMST	—	—	1	μA	—
〈Control circuit power supply current〉						
Standby	IDDST	—	—	1	μA	PSB=L
No signal	IDDO	—	0.6	1	mA	PSB=H, all inputs Low
Operation	IDDA	—	3.3	6.5	mA	PSB=H, all channels driven together
〈Pre-drive power supply voltage〉						
No input	IG1	7.5	8.9	10	V	PSB=H, all inputs Low
Operation	IG2	6.0	7.2	9.5	V	PSB=H, all channels driven together
〈Logic input characteristics〉						
Input high level voltage	VIH	V_{DD}−0.6	—	—	V	—
Input low level voltage	VIL	—	—	0.6	V	—
Input high level current 1	IIH1	—	—	1	μA	V_{IN} = 3V, each driver input
Input low level current 1	IIL1	−1	—	—	μA	V_{IN} = 0V, each driver input
Input high level current 2	IIH2	—	300	600	μA	V_{IN} = 3V, CLK, PSB pins
Input low level current 2	IIL2	−1	—	—	μA	V_{IN} = 0V, CLK, PSB pins
Output on-resistance	RON3, 4	—	0.8	1.2	Ω	Balance of top and bottom resistors VG = 10V
	RON1, 2	—	1.2	2.0		
Output transmission delay time	tRISE	—	0.2	1	μsec	—
	tFALL	—	0.2	1	μsec	—
Minimum input pulse width	tmin	200	—	—	nsec	Output pulse width 2 / 3 tmin or more
〈Oscillator circuit〉						
Free-running frequency	fosc	150	300	400	kHz	Pin 32 waveform monitor
Clock period range	fsync	100	—	500	kHz	Input from CLK input

◎Not designed for radiation resistance.

●Driver truth table

PSB*	IN1～4F	IN1～4R	OUT1～3F	OUT1～3R	OUT4F	OUT4R
H	L	L	L	L	L	L
H	L	H	L	H	L	H
H	H	L	H	L	L	L
H	H	H	L	L	H	L
L	×	×	High-Z	High-Z	High-Z	High-Z

* When PSB is Low, all outputs are high impedance, regardless of the state of the inputs. Also, the voltage multiplier circuit oscillator stops oscillating.

●Measurement circuit

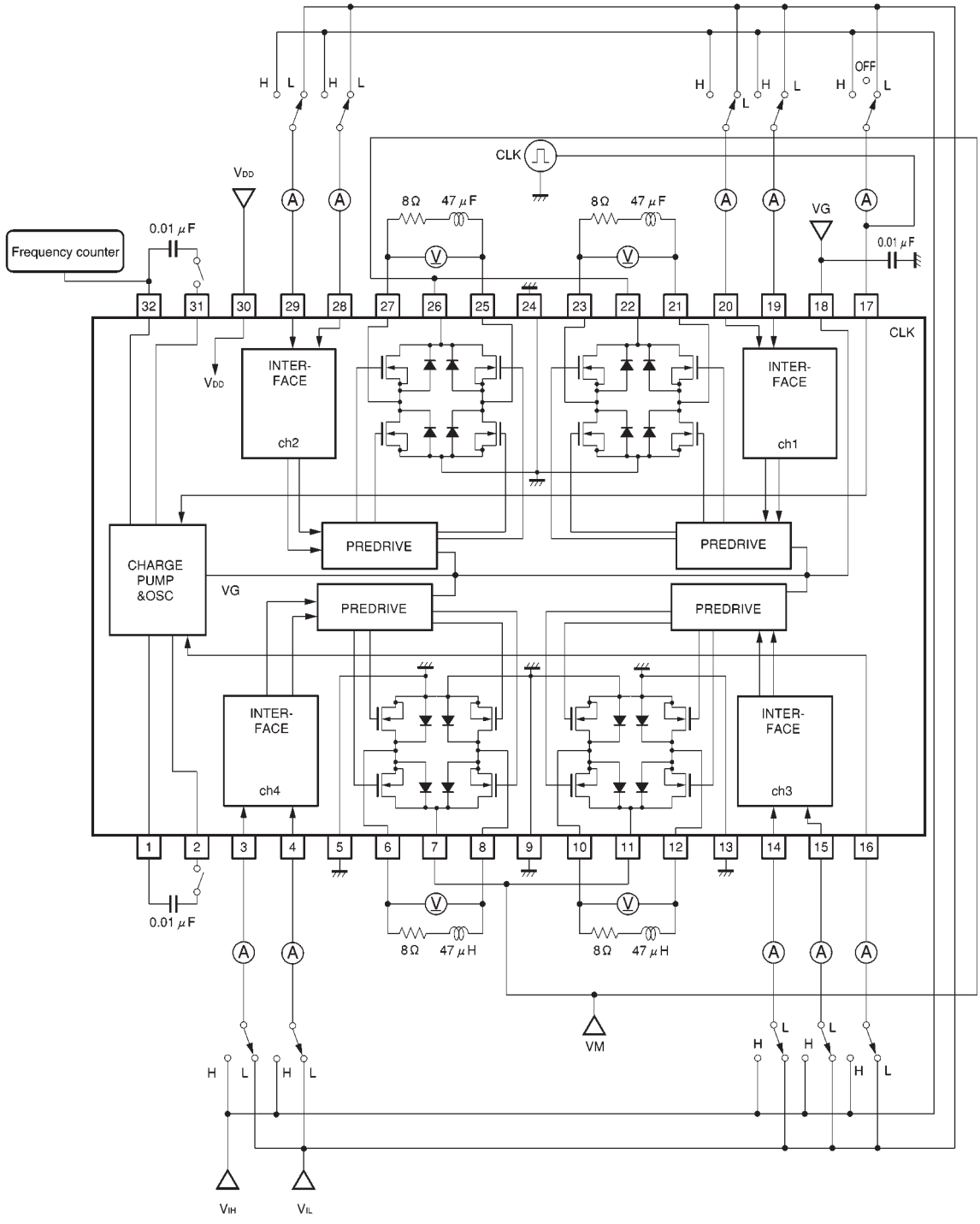


Fig.2

●Operation notes

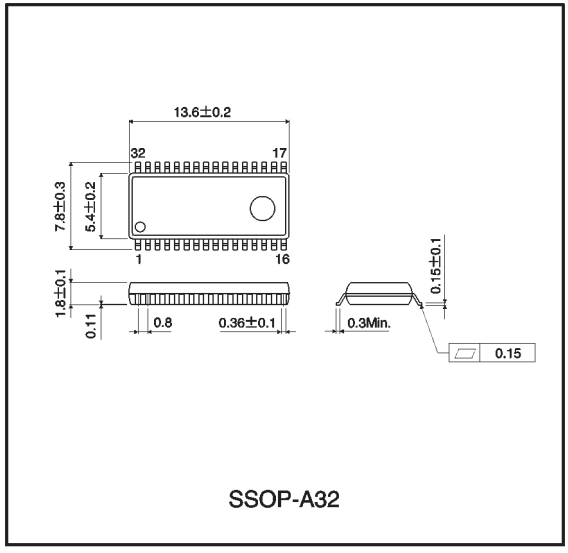
(1) The charge pump circuit is a × 3 multiplier that uses the voltage on pin 30 as its reference. Therefore, set the voltage (V_{DD}) on pin 30 so that the VG does not exceed its rating.

(2) If you will use an externally-supplied VG, disconnect the capacitors between pins 31 and 32 and pins 1 and 2.

(3) The charge pump oscillator circuit runs freely when the CLK pin is connected to either V_{DD} or GND. Also, as there is a pull-down resistor on the chip, it will also free run if CLK is left floating.

To synchronize with an external clock, input the clock pulses from the CLK pin.

●External dimensions (Units: mm)



SSOP-A32