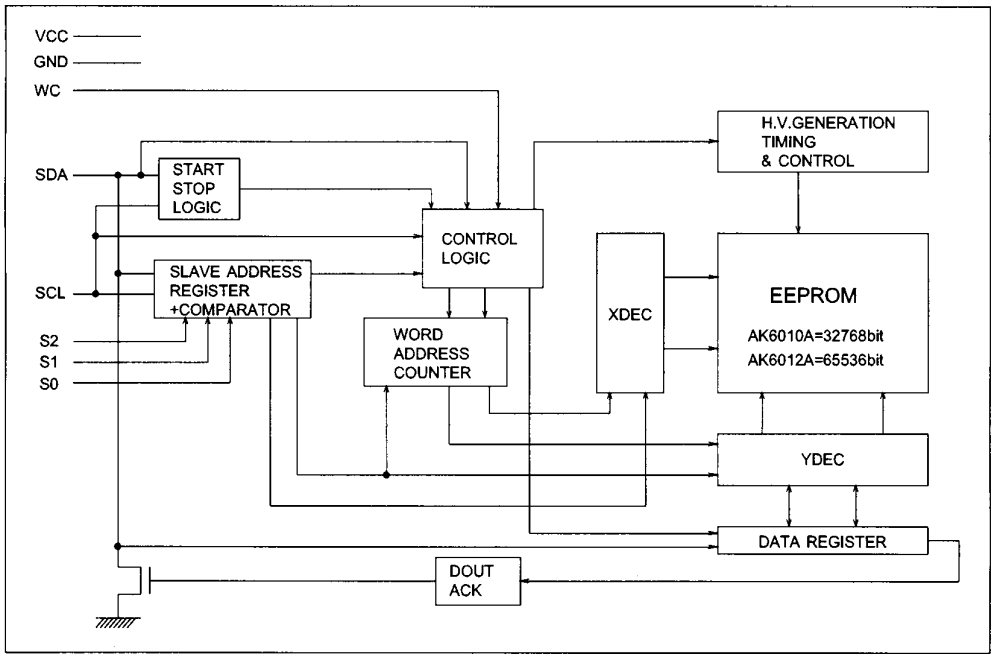
AK6010A / 12A

I²C bus 32K / 64Kbit Serial CMOS EEPROM

Features

- ADVANCED CMOS EEPROM TECHNOLOGY
- READ/WRITE NON-VOLATILE MEMORY
- WIDE VCC OPERATION ··· Vcc = 1.8V ~ 5.5V
- AK6010A・・32768 bits, 4096 × 8 organization
  AK6012A・・65536 bits, 8192 × 8 organization
- I²C™ SERIAL INTERFACE
- LOW POWER CONSUMPTION
  - 0.8μA max. Standby
- HIGH RELIABILITY
  - Endurance : 100K cycles
  - Data Retention : 10 years
- 32 byte page write mode
- Automatic write cycle time-out with auto-ERASE
- IDEAL FOR LOW DENSITY DATA STORAGE
  - Low cost, space saving, 8-pin package (SOP)



Block Diagram

I²C™ is a registered trademark of Phillips Corporation.

General Description

The AK6010A/12A is a 32768/65536-bit serial CMOS EEPROM divided into 4096/8192 registers of 8 bits each.
The AK6010A/12A can operate full function under wide operating voltage range from 1.8V to 5.5V. The charge up circuit is integrated for high voltage generation that is used for write operation.

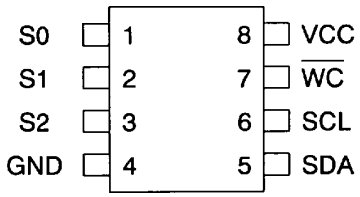
The AK6010A/12A conforms to all specifications in the 2 wire protocol and is controlled by serial clock (SK) and serial data (SDA) line.

Some devices can be connected to the same bus. Each device connected to the bus is software addressable by a unique address, and can operate as either a transmitter or receiver. In addition to transmitters and receivers, devices can also be considered as masters or slaves when performing data transfers (see Table1). The master is the device which initiates a data transfers on the bus and generates the clock signals to permit that transfer. At that time, the device addressed is considered as the slave.

TERM	DESCRIPTION
Transmitter	The device which sends the data to the bus
Receiver	The device which receives the data from the bus
Master	The device which initiates a transfer, generates clock signals and terminates a transfer
Slave	The device addressed by a master

Table 1. Definitions

■ Pin arrangement



Pin Name	Function
S0,S1,S2	Device Address Inputs
SCL	Clock Input
SDA	Data Input / Output
$\overline{WC}$	Write Control
Vcc	Power Supply
GND	Ground

■ Type of Products

Model	Memory size	Temp.Range	Vcc	Package
AK6010AF	32Kbits	-40°C~85°C	1.8V~5.5V	8pin Plastic SOP
AK6012AF	64Kbits	-40°C~85°C	1.8V~5.5V	8pin Plastic SOP

■ DATA TRANSFER

All commands are preceded by a START condition. After the START condition, a slave address is sent. After the AK6010A/12A recognizes the START condition, the devices interfaced to the bus wait for the slave address to be transmitted over the SDA line. If the transmitted slave address matches an address of one of the devices, the designated slave pulls the SDA line to LOW (ACKNOWLEDGE) .
The data transfer is always terminated by a STOP condition generated by the master.

[Data validity]
The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW.

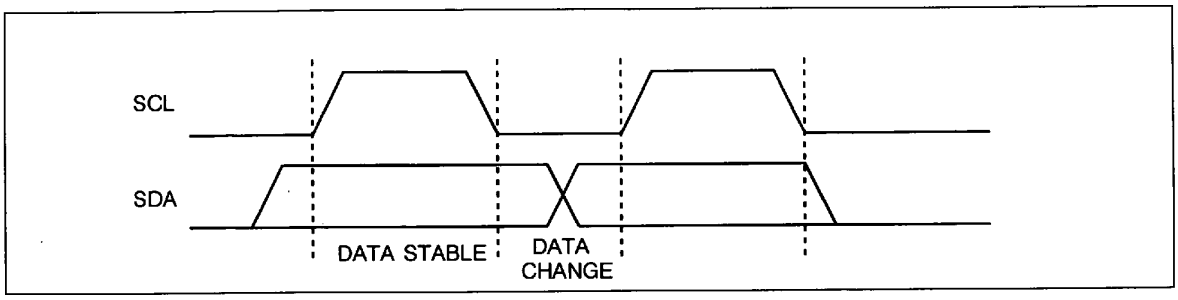


Figure1. Data transfer

[START and STOP condition]
A HIGH to LOW transition on the SDA line while SCL is HIGH defines a START condition. All commands are preceded by the START condition.

A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition. All communications are terminated by the STOP condition. After a read sequence, the STOP condition will place the EEPROM in a standby power mode.

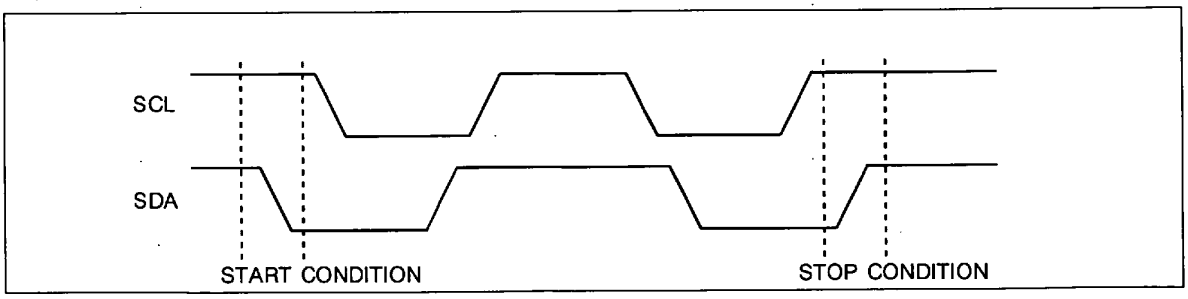


Figure2. Start and STOP Definition

[ACKNOWLEDGE]

ACKNOWLEDGE is a software convention used to indicate successful data transfers. The transmitting device will release the bus after transmitting eight bits. During the next clock (ninth clock), the receiver will pull the SDA line to LOW to acknowledge that it received the eight bits of data.
The AK6010A/12A will respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a write operation have been selected, the AK6010A/12A will respond with an acknowledge after the receipt of each subsequent eight bit word.

In the read mode the AK6010A/12A slave will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no STOP condition is generated by the master, the slave will continue to transmit data. If an acknowledge is not detected, the slave will terminate further data transmissions and await the STOP condition to return to the standby power mode.

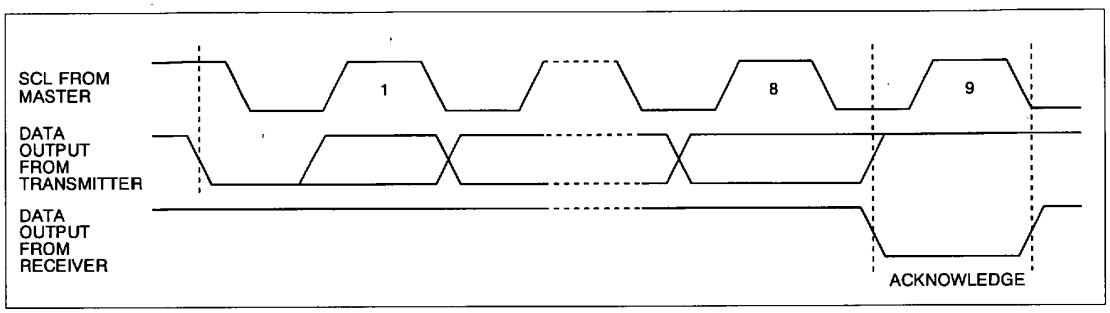


Figure3. Acknowledge Response from Receiver

[SLAVE ADDRESS]

After the START condition, a SLAVE ADDRESS is sent. If the transmitted slave address matches an address of one of the device, the designated slave pulls the SDA line to LOW .

The most significant four bits of the slave address are fixed as "1010". The next three bits are S0, S1 and S2 device address bits. These three bits identify the specific device on the bus. They is set by the hard wired input pins (S0 pin, S1 pin and S2 pin). Therefore a total of eight devices can be connected to the same bus.

The last bit of the slave address (R/$\overline{W}$ bit) defines whether a write or read condition is requested by the master. A "1" indicates that the read operation is to be executed. A "0" indicates that the write operation is to be executed.

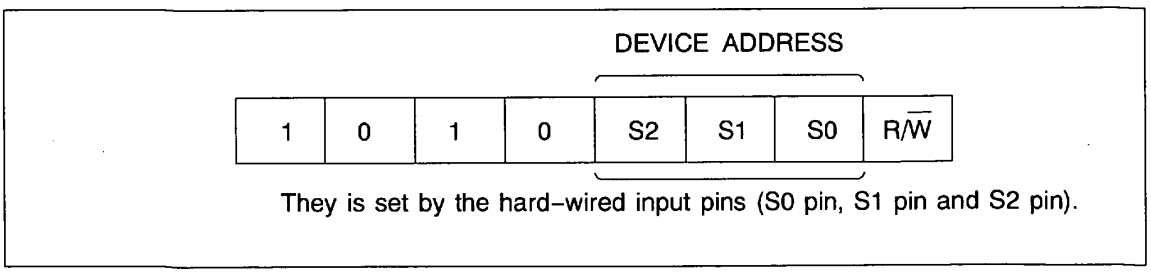


Figure4. Slave Address

Pin Descriptions

SCL (Serial Clock)
The SCL input is used to clock all data into and out of the device.

SDA (Serial Data)
The SDA is a bidirectional pin used to transfer data into and out of the device.
It is an open drain output and may be wire-ORed with any number of open drain or open collector outputs.

S0, S1, S2 (Device Address)
The S0, S1 and S2 are device address inputs that are used to set three bits of the slave address. A total of eight devices can be connected to the same bus.

$\overline{WC}$ (Write Control)
If the $\overline{WC}$ is High level, WRITE operations onto the upper quarter of the memory (AK6010A: C00~FFF(Hex), AK6012A:1800~1FFF(Hex)) will not be executed. If the $\overline{WC}$ is Low level, the AK6010A/12A will be enabled to perform WRITE operation.

As the $\overline{WC}$ is internally pulled down to GND, the AK6010A/12A will be enabled to perform WRITE operation if the $\overline{WC}$ is left floating.
$\overline{WC}$ must not change from the start condition input to the stop condition input.

VCC (Power Supply)

GND (Ground)

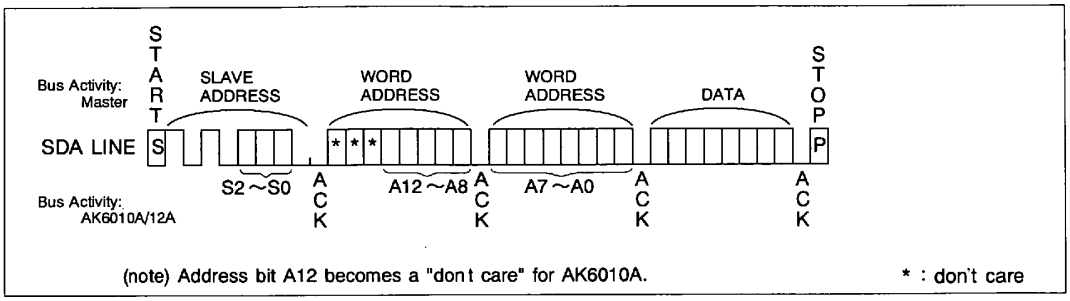
Functional Descriptions

■ WRITE Operations

BYTE WRITE

A write operation requires a word address following the slave address word (R/$\overline{W}$=0) and acknowledge. The word address is comprised of eight bits and provides access to any one of the 4096/8192 words. Upon receipt of the word address the AK6010A/12A responds with an acknowledge, and awaits the next eight bits of data, again, responding with an acknowledge.

The master then terminates the transfer by generating a stop condition, at which time the AK6010A/12A begins the internal write cycle to the nonvolatile memory. While the internal write cycle is in progress the AK6010A/12A inputs are disable, and the device will not respond to any requests from the master.



BYTE WRITE

PAGE WRITE

The AK6010A/12A is capable of a thirty-two byte page write operation.

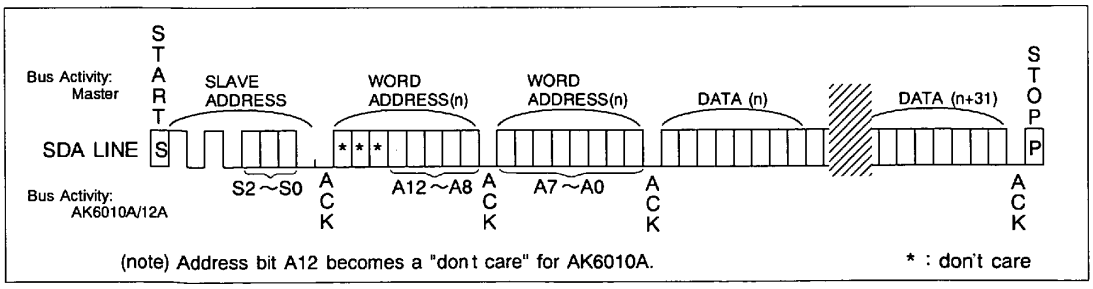
It is initiated in the same manner as the byte write operation. But instead of terminating the write cycle after the first data word is transferred, the master can transmit up to thirty-one more words. After the receipt of each word, the AK6010A/12A will respond with an acknowledge. The master then terminates the transfer by generating a stop condition, at which time the AK6010A/12A begins the internal write cycle to the nonvolatile memory.

After the receipt of each word, the five lower order address pointer bits are internally incremented by one. The higher order seven/eight bits of the word address remains constant.

AK6010A: When the highest address is reached (XXXX XXX1 1111), the address counter rolls over to address "XXXX XXX0 0000" allowing the read cycle to be continued indefinitely.

AK6012A: When the highest address is reached (X XXXX XXX1 1111), the address counter rolls over to address "X XXXX XXX0 0000" allowing the read cycle to be continued indefinitely.

If the master should transmit more than thirty-two words prior to generating the stop condition, the address counter will "roll over" and the previously written data will be overwritten. When the master transmit thirty-four words prior to the stop condition, thirty-third word will be overwritten to first word, and thirty-fourth word will be overwritten to second word.

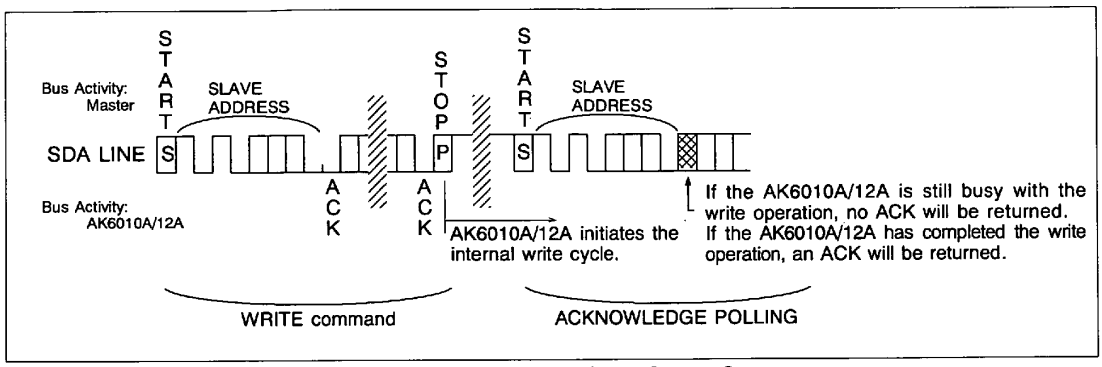


PAGE WRITE

ACKNOWLEDGE POLLING

Since the device will not acknowledge during the internal write cycle, this can be used to determine when the cycle is complete. This feature (ACK polling) can be used to maximize bus troughtput. Once the stop condition is issued to indicate the end of the host's write operation the AK6010A/12A initiates the internal write cycle. ACK polling can be initiated immediately. This involves issuing the start condition followed by the slave address for a write operation. If the AK6010A/12A is still busy with the write operation no ACK will be returned. If the AK6010/12A has completed the write operation an ACK will be returned and the host can then proceed with the next read or write operation.

When the write operation is executed after the ACK polling, the host can issue the byte address consecutively after the ACK is returned. When the read operation is executed after the ACK polling, the host should issue the stop condition once.



ACKNOWLEDGE POLLING

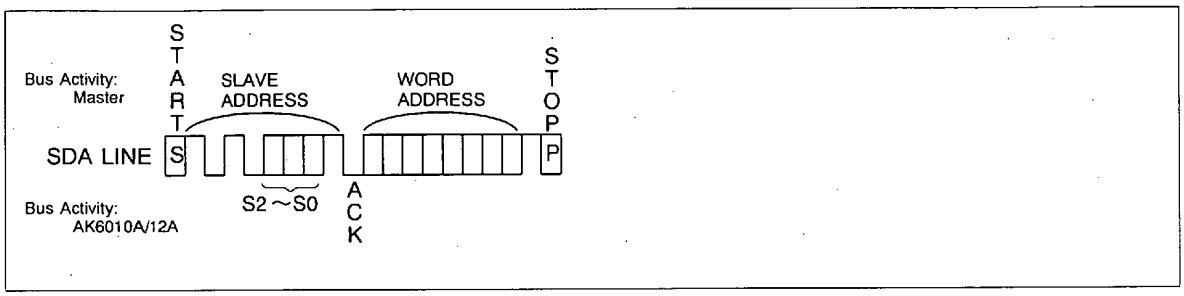
■ READ Operations

There are three basic read operations: current address read, random read, and sequential read. Read operations are initiated in the same manner as write operations, with the exception that the R/$\overline{W}$ bit of the slave address is set to a one.

It is noted that the ninth clock cycle of the read operation is not a "don't care". To terminate a read operation, the master must hold SDA HIGH during the ninth clock cycle and then issue a stop condition.

CURRENT ADDRESS READ

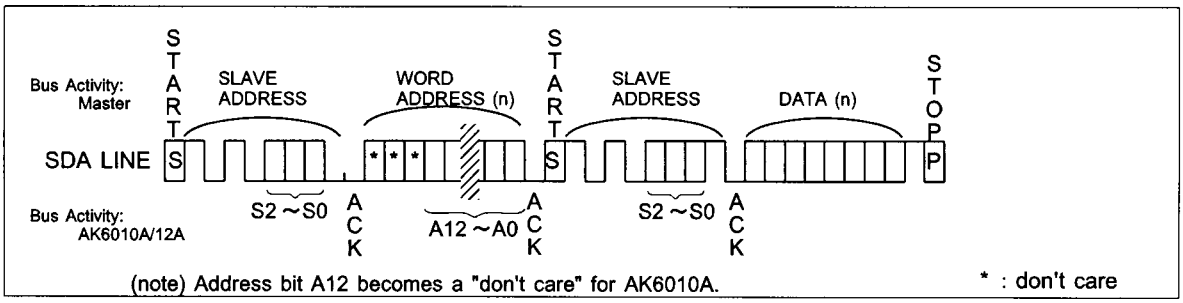
Internally the AK6010A/12A contains an address counter that maintains the address of the last word accessed, incremented by one. Therefore, if the last access (either a read or write) was to address n, the next read operation would access data from address n+1.
Upon receipt of the slave address with R/$\overline{W}$ bit set to one, the AK6010A/12A issues an acknowledge and transmits the eight bit word. The master will not acknowledge the transfer but generate a stop condition, and therefore the AK6010A/12A discontinues transmission.



CURRENT ADDRESS READ

RANDOM READ

Random read operations allow the master to access any memory location in a random manner. Prior to issuing the slave address with the R/$\overline{W}$ bit set to one, the master must first perform a "dummy" write operation.
The master issues the start condition, slave address and then the word address it is to read. After the word address acknowledge, the master immediately reissues the start condition and the slave address with the R/$\overline{W}$ bit set to one. This will be followed by an acknowledge from the AK6010A/12A and then by the eight bit word. The master will not acknowledge the transfer but generate the stop condition, and therefore the AK6010A/12A discontinues transmission.



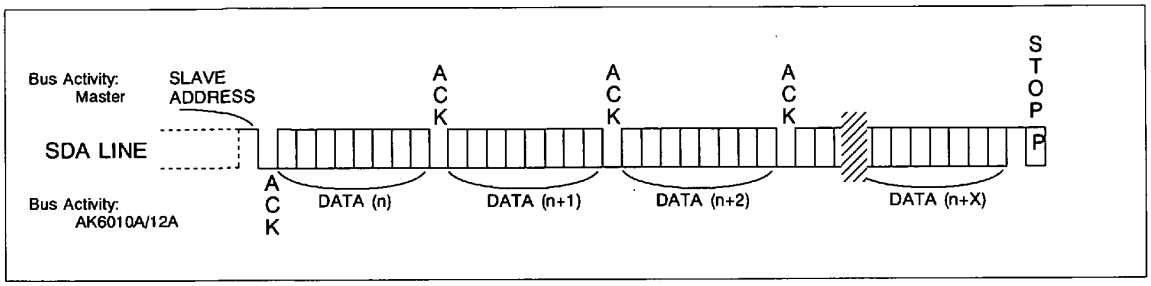
RANDOM READ

SEQUENTIAL READ

Sequential read can be initiated as either a current read or random read. The first word is transmitted in the same manner as the other read modes. However the master responds with an acknowledge, indicating it requires additional data. The AK6010A/12A continues to output data for each acknowledge received. The data output is sequential, with the data from address n followed by the data from n+1. The master will not acknowledge the transfer but generate the stop condition, and therefore the AK6010A/12A discontinues transmission.

AK6010A ・・・ When the highest address is reached ($FFF), the address counter rolls over to address $000 allowing the read cycle to be continued indefinitely.

AK6012A ・・・ When the highest address is reached ($1FFF), the address counter rolls over to address $0000 allowing the read cycle to be continued indefinitely.



SEQUENTIAL READ

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Power Supply	VCC	-0.6	+7.0	V
All Input Voltages with Respect to Ground	VIO	-0.6	VCC+0.6	V
Ambient storage temperature	Tst	-65	+150	°C

Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum conditions for extended periods may affect device reliability.

Recommended Operating Condition

Parameter	Symbol	Min	Max	Unit
Power Supply	VCC	1.8	5.5	V
Ambient Operating Temperature	Ta	-40	+85	°C

Electrical Characteristics

(1)DC Electrical Characteristics

(-40°C≤Ta≤85°C, 1.8V≤VCC≤5.5V unless otherwise specified)

Parameter	Symbol	Condition		Min.	Max.	Unit
Current Dissipation (WRITE)	ICC1	VCC=5.5V fSCL=400KHz	AK6010A		4.0	mA
			AK6012A		5.0	mA
	ICC2	VCC=2.5V fSCL=100KHz	AK6010A		3.5	mA
			AK6012A		4.5	mA
	ICC3	VCC=1.8V fSCL=100KHz	AK6010A		2.5	mA
			AK6012A		3.5	mA
Current Dissipation (READ)	ICC4	VCC=5.5V fSCL=400KHz	AK6010A		500	uA
			AK6012A		700	uA
	ICC5	VCC=2.5V fSCL=100KHz	AK6010A		200	uA
			AK6012A		250	uA
	ICC6	VCC=1.8V fSCL=100KHz	AK6010A		150	uA
			AK6012A		200	uA
Current Dissipation (Standby)	ICCS	VCC=5.5V, *1			0.8	uA
Input High Voltage	VIH1	2.5V≤VCC≤5.5V		0.7×VCC	VCC+0.5	V
	VIH2	1.8V≤VCC<2.5V		0.8×VCC	VCC+0.5	V
Input Low Voltage	VIL1	2.5V≤VCC≤5.5V		-0.3	0.3×VCC	V
	VIL2	1.8V≤VCC<2.5V		-0.3	0.2×VCC	V
Output Low Voltage	VOL1	2.5V≤VCC≤5.5V IOL=4.5mA			0.4	V
	VOL2	1.8V≤VCC<2.5V IOL=3mA			0.4	V
Hysteresis of Schmitt trigger inputs (SCL, SDA) *2	VHYS			0.05×VCC		V
Input Leakage Current *3	ILI	VCC=5.5V,VIN=VCC/GND			±1.0	uA
Output Leakage Current	ILO	VCC=5.5V, VOUT=VCC/GND			±1.0	uA

*1:VIN=VCC / GND, $\overline{WC}$=GND

*2:The parameter is periodically sampled and not 100% tested.

*3:SCL,SDA,S0,S1,S2

(2)Capacitance

(Ta=25°C, f=1MHz,VCC=5.0V)

Parameter	Symbol	Condition	Min.	Max.	Unit
Input/Output Capacitance (SDA)	CI/O	VI/O=0V		8.0	pF
Input Capacitance (SCL)	CIN	VIN=0V		6.0	pF

(note) The parameter is periodically sampled and not 100% tested.

(3)AC Electrical Characteristics1: Standard mode

(-40°C≤Ta≤85°C, 1.8V≤VCC≤5.5V unless otherwise specified)

Parameter	Symbol	Condition	Min.	Max.	Unit
SCL Clock Frequency	fSCL			100	KHz
Noise Suppression Time Constant at SCL,SDA *5	tI			100	ns
SCL Low to SDA Data Out Valid : SDA	tAA1		0.2	3.5	us
	tAA2		0.3	3.5	us
	tAA3		0.3	4.5	us
Time the Bus Must be Free before a New Transmission can start	tBUF		4.7		us
Start Condition Hold Time	tHD:STA		4.0		us
Clock Low Period	tLOW		4.7		us
Clock High Period	tHIGH		4.0		us
Start Condition Setup Time	tSU:STA		4.7		us
Data in Hold Time	tHD:DAT		0		us
Data in Setup Time	tSU:DAT		250		ns
SDA and SCL Rise Time *5	tR			1.0	us
SDA and SCL Fall Time *5	tF			0.3	us
Stop Condition Setup Time	tSU:STO		4.0		us
Data Out Hold Time	tDH		100		ns
Write Cycle Time *4	tWR			10	ms

*4: The write cycle time (tWR) is the time from a valid stop condition of a write sequence to the end of the internal program cycle.
Since the device will not acknowledge during the internal program cycle, this can be used to determine when the cycle is complete. This feature (ACK polling) can be used to maximize bus troughtput.

*5: The parameter is periodically sampled and not 100% tested.

(4)AC Electrical Characteristics2: Fast mode

(-40°C≤Ta≤85°C, 4.5V≤VCC≤5.5V unless otherwise specified)

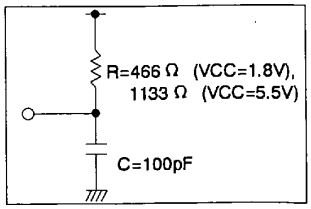
Parameter	Symbol	Condition	Min.	Max.	Unit
SCL Clock Frequency	fSCL			400	KHz
Noise Suppression Time Constant at SCL,SDA *7	tI			50	ns
SCL Low to SDA Data Out Valid : SDA	tAA		0.2	0.9	us
Time the Bus Must be Free before a New Transmission can start	tBUF		1.3		us
Start Condition Hold Time	tHD:STA		0.6		us
Clock Low Period	tLOW		1.3		us
Clock High Period	tHIGH		0.6		us
Start Condition Setup Time	tSU:STA		0.6		us
Data in Hold Time	tHD:DAT		0		us
Data in Setup Time	tSU:DAT		100		ns
SDA and SCL Rise Time *7	tR			0.3	us
SDA and SCL Fall Time *7	tF			0.3	us
Stop Condition Setup Time	tSU:STO		0.6		us
Data Out Hold Time	tDH		50		ns
Write Cycle Time *6	tWR			10	ms

*6: The write cycle time (tWR) is the time from a valid stop condition of a write sequence to the end of the internal program cycle.
Since the device will not acknowledge during the internal program cycle, this can be used to determine when the cycle is complete. This feature (ACK polling) can be used to maximize bus troughtput.

*7: The parameter is periodically sampled and not 100% tested.

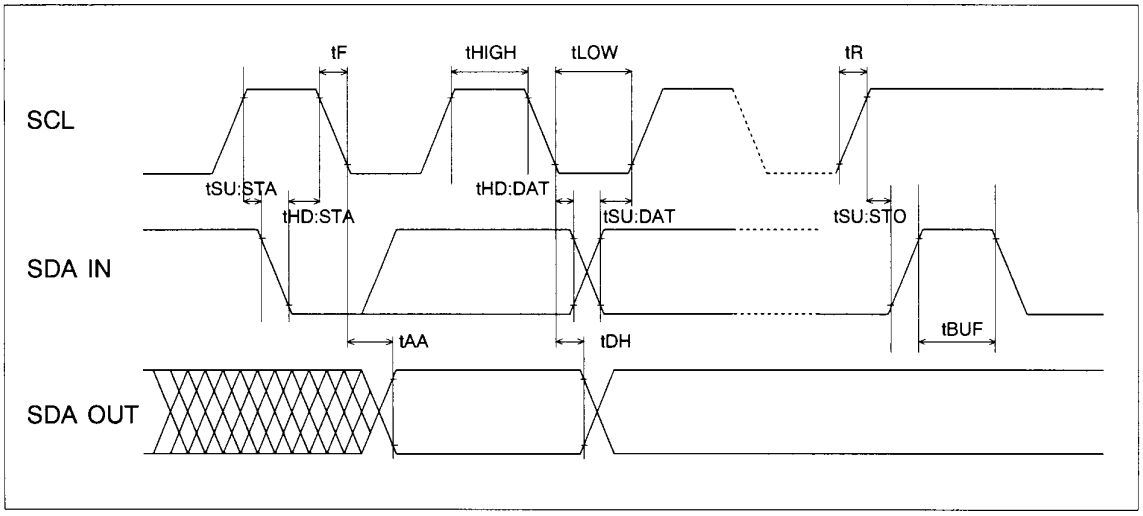
■ **AC Conditions of Test**

Input Pulse Levels	0.1×VCC~0.9×VCC
Input Rise and Fall Times	10ns
Output Timing Level	0.5×VCC

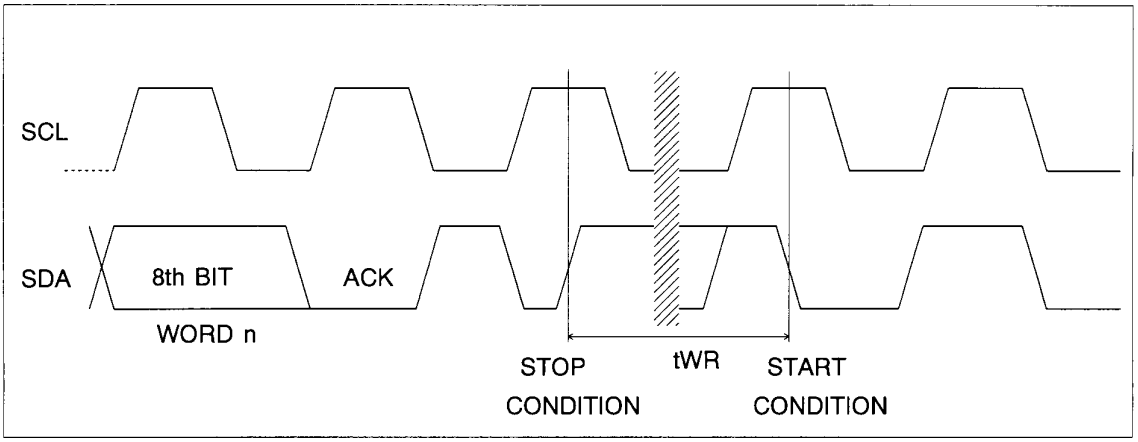


Equivalent AC Load Circuit

Synchronous Data Timing



BUS TIMING



WRITE CYCLE TIMING

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