SC2598

Low Voltage DDR Termination Regulator

Features

- Input to linear regulator (VIN): 1.0V to 3.6V
- Output (VTT): 0.5V to 1.8V
- Bias Voltage (VDD): 2.35V to 3.6V
- Up to 3A sink or source from VTT for DDR through DDR4
- ± 1% over temperature (with respect to VDDQ/2, including internal resistor divider variation) VREF and VTT
- Logic-level enable input
- Built in soft-start
- Thermal shutdown with auto-restart
- Over current protection
- Minimal output capacitance
- Package: SOIC8-EDP

Applications

- DDR Memory Termination

Description

The SC2598 is designed to meet the latest JEDEC specification for low power DDR3 and DDR4, while also supporting DDR and DDR2. The SC2598 regulates up to ± 3A for VTT and up to ± 40mA for VREF.

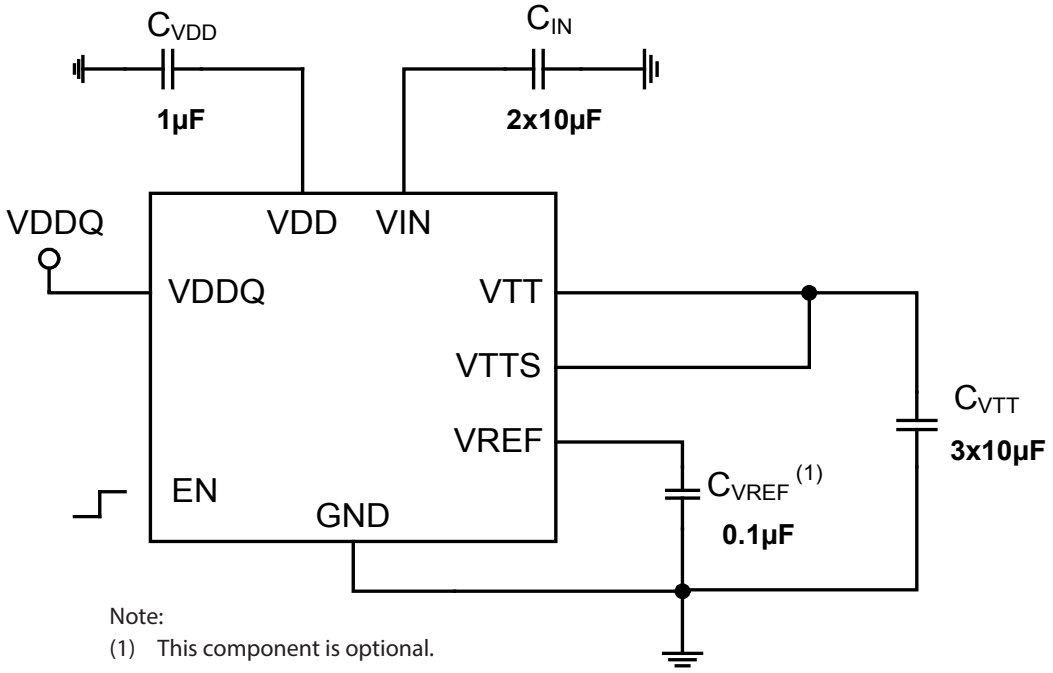
The SC2598 also provides an accuracy of ±1% over temperature (which takes into account the internal resistor divider) for VREF and VTT for the memory controller and DRAM.

SC2598 protection features include thermal shutdown with auto-restart for VTT and over-current limit for both VTT and VREF.

Under-Voltage-Lock-Out circuits are included to ensure that the output is off when the bias voltage falls below its threshold, and that the part behaves elegantly in power-up or power-down.

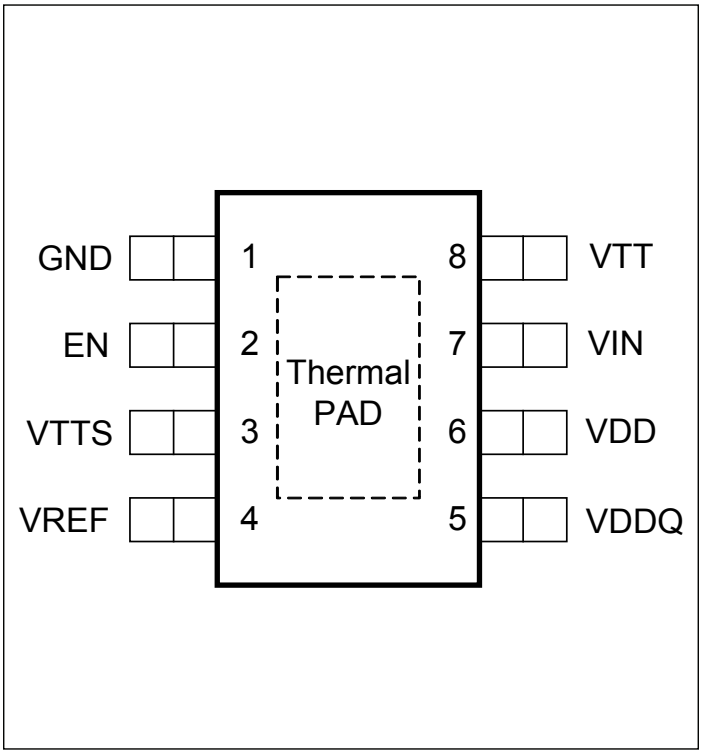
The low external parts count combined with industry leading specifications make SC2598 an attractive solution for DDR through DDR4 termination.

Typical Application Circuit



Note:
(1) This component is optional.

Pin Configuration

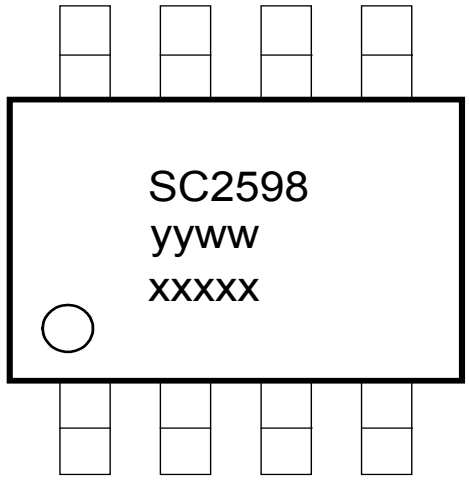


Ordering Information

Device	Package
SC2598SETRC[1][2]	SOIC8-EDP
SC2598EVB	Evaluation Board

Notes:
(1) Available in tape and reel only. A reel contains 2500 devices.
(2) Lead-free packaging only. Device is WEEE and RoHS compliant and halogen-free.

Marking Information



yyww = Date Code
xxxxx = Semtech Lot Number

SEMTECH

Absolute Maximum Ratings

VIN (V)	-0.3 to 4.3
VDD to GND (V)	-0.3 to 4.3
VTT to GND (V)	-0.3 to VDD
EN (V)	-0.3 to 6.0
Other pins	-0.3 to 4.3
ESD Protection Level[1] (kV)	4

Thermal Information

Thermal Resistance, Junction to Ambient[2] (°C/W)	46
Thermal Resistance, Junction to Ambient[3] (°C/W)	38
Maximum Junction Temperature (°C)	+150
Storage Temperature Range (°C)	-65 to +150
Peak IR Reflow Temperature (10s to 30s) (°C)	+260

Exceeding the above specifications may result in permanent damage to the device or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not recommended.

Notes:
(1) HBM: tested according to ANSI/ESDA/JEDEC JS-001.
(2) Calculated from package in still air, mounted to 3 x 4.5 (in), 4 layer FR4 PCB with thermal vias under the exposed pad per JESD51 standards.
(3) Based upon lab measurement on EVB board: 3 x 2 (in), 4 layer FR4 PCB with thermal vias under the exposed pad.

Electrical Characteristics

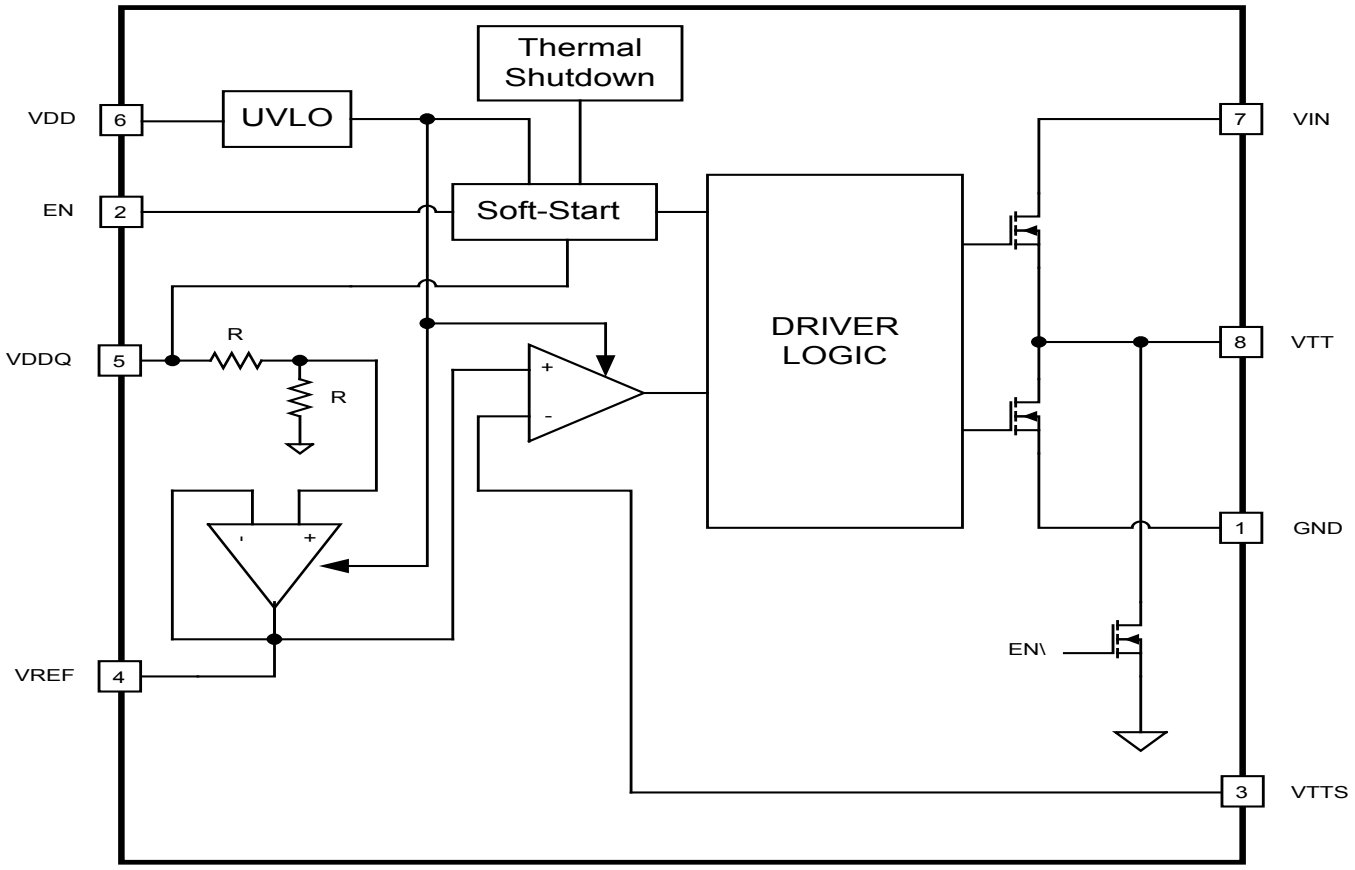
Unless otherwise noted T_J = -40 to +125°C, V_{IN} = 1.2V, V_{DD} = 3.3V, $V_{DD\,Q}$ = 1.2V . Typical values are at T_A = 25°C.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input Supplies						
LDO Supply Voltage	V_{IN}		1		3.6	V
VDD Supply Voltage	V_{DD}		2.35		3.6	V
VDD UVLO Threshold		Measured at VDD pin, rising edge	2.0		2.25	V
		Measured at VDD pin, falling edge	1.95		2.15	
VDD UVLO Hysteresis				0.1		V
Quiescent Current for VDD	I_Q	Load =0A, EN = High, $V_{VDDQ} \geq 1V$		415	700	µA
Shutdown Current for VDD	I_{QSD}	Load =0A, EN = Low, $V_{VDDQ} \geq 1V$, I_{REF} = 0A		160	400	µA
		Load =0A, EN = Low, V_{VDDQ} = 0V, I_{REF} = 0A		100	160	µA
Quiescent Current for V_{IN}	I_{IN}	Load =0A, EN = High		3	30	µA
Shutdown Current for V_{IN}	I_{INSD}	Load =0A, EN = Low		3	20	µA
VTT Output						
Output Voltage Range	VTT		0.5		1.8	V
Output Voltage Tolerance with respect to VDDQ/2		Load = 0A, VTT = 0.5V to 1.8V	-1		+1	%

Electrical Characteristics (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Load Regulation		-2A ≤ Load ≤ 2A	-25		+25	mV
On-Resistance		High-Side MOSFET (source), Load = 0.1A	50	100	150	mΩ
		Low-Side MOSFET (sink), Load = 0.1A	40	140	300	
Discharge MOSFET On-Resistance		EN = Low		8		Ω
Reference Input/Output						
VDDQ Voltage Range			1		3.6	V
VDDQ Input Bias Current			0		10	µA
Tolerance with respect to VDDQ/2		Load = 0A, VREF = 0.5V to 1.8V	-1		1	%
VREF Source Current Limit			40			mA
VREF Sink Current Limit			- 40			
Protection						
Thermal Shutdown Threshold				160		^{0}C
Thermal Restart Hysteresis				20		^{0}C
Output Current Limit Threshold		Ambient Temperature: 25 ^{0}C	3.7	4.3		A
Soft-Start						
VTT Soft-Start Time		From EN = High to V_{TT} = 90% VREF		40		µs
Logic						
EN Logic Threshold		EN = High	1.7			V
		EN = Low			0.3	
EN Input Current			-1		1	µA

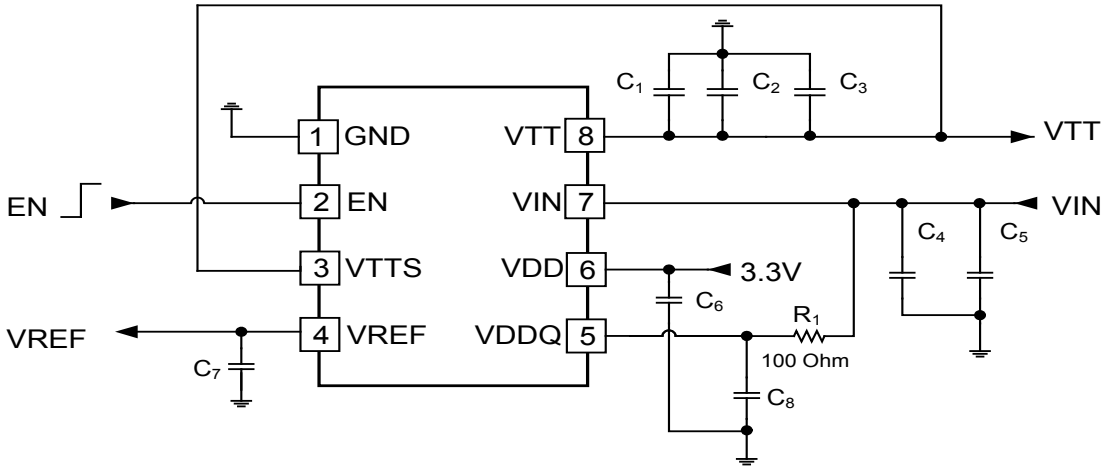
Block Diagram



Pin Descriptions

Pin #	Pin Name	Pin Function
1	GND	Ground reference for the IC.
2	EN	Logic input to enable or disable the VTT output. If EN pin is grounded to shut down the linear regulator, VREF remains active.
3	VTTS	VTT output sense input. Connect VTTS to the output at the output capacitor to implement remote sense.
4	VREF	The reference output, equal to one half of VDDQ. Connect a 100nF capacitor from this pin to GND.
5	VDDQ	External reference input.
6	VDD	Input bias voltage. Connect a ceramic capacitor from this pin to GND.
7	VIN	LDO input. Connect ceramic capacitors from this pin to GND.
8	VTT	Output of the linear regulator. Connect ceramic capacitors from this pin to GND.
PAD	NC	Thermal pad. Not electrically connected. Connect to the GND plane using multiple vias for optimal heat sinking.

Detailed Application Circuit



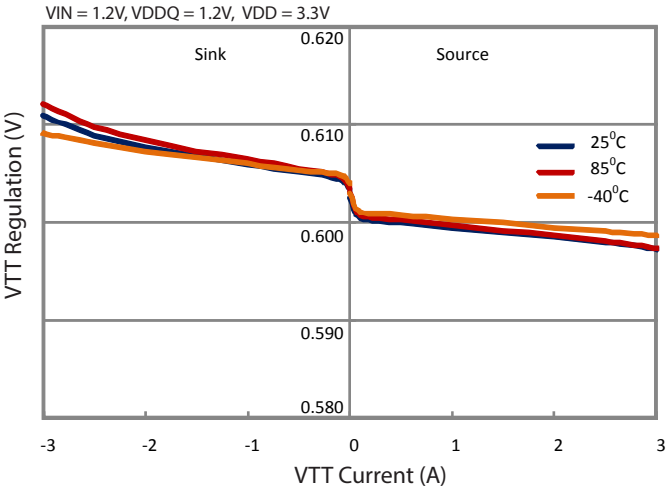
Bill Of Materials

Reference Designator	Description	Value	Part Number	Manufacture
C_1, C_2, C_3, C_4, C_5,	Ceramic Capacitor	10uF/0805/X7R	GRM21BR71A106KE51	Murata
C_6	Ceramic Capacitor	1uF/0603/X7R	GRM188R71A105KA61D	Murata
C_7, C_8	Ceramic Capacitor	0.1uF/0603/X7R	GRM188R71H104KA93D	Murata

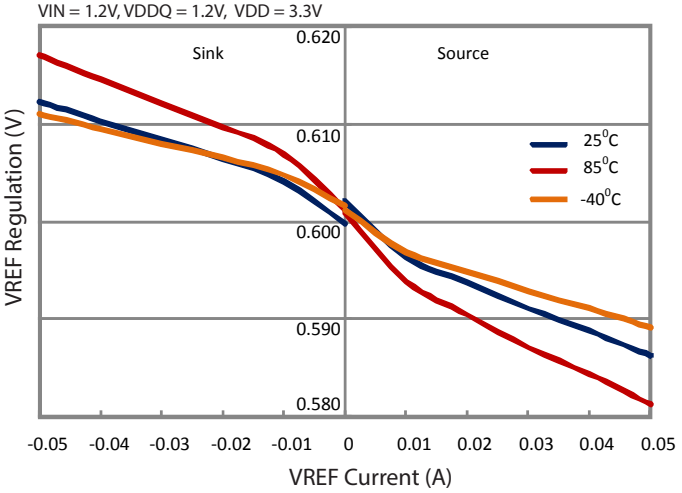
Typical Characteristics

Characteristics in this section are based upon the detailed application circuit on page 6.

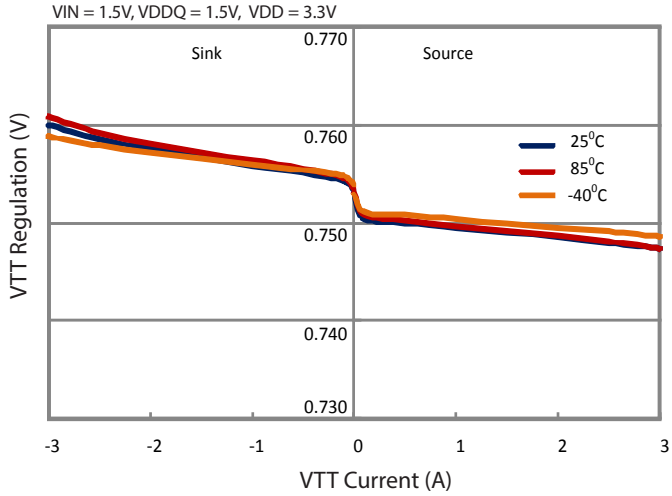
0.6V VTT Regulation Sink/Source



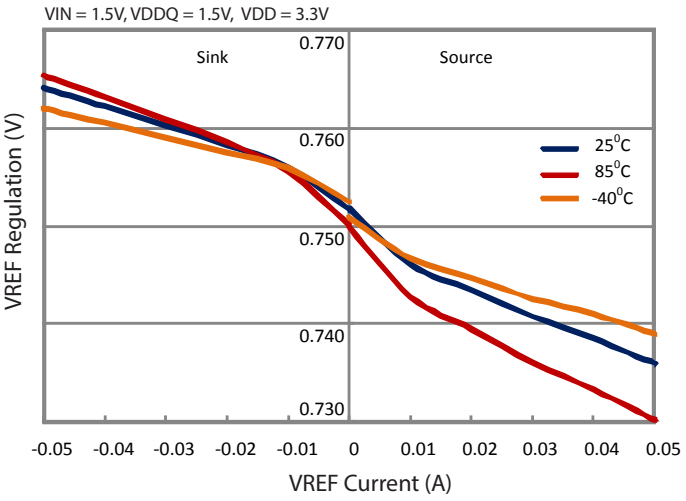
0.6V VREF Regulation Sink/Source



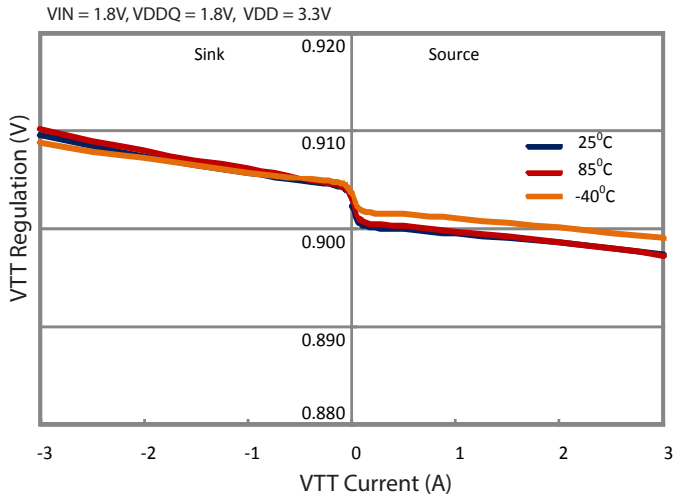
0.75V VTT Regulation Sink/Source



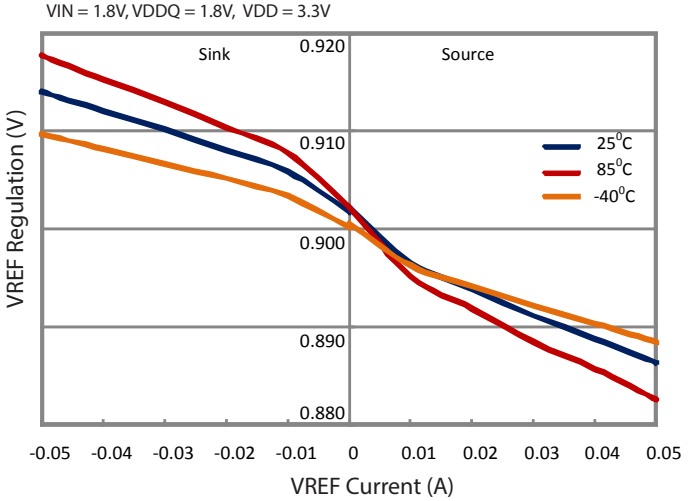
0.75V VREF Regulation Sink/Source



0.9V VTT Regulation Sink/Source



0.9V VREF Regulation Sink/Source

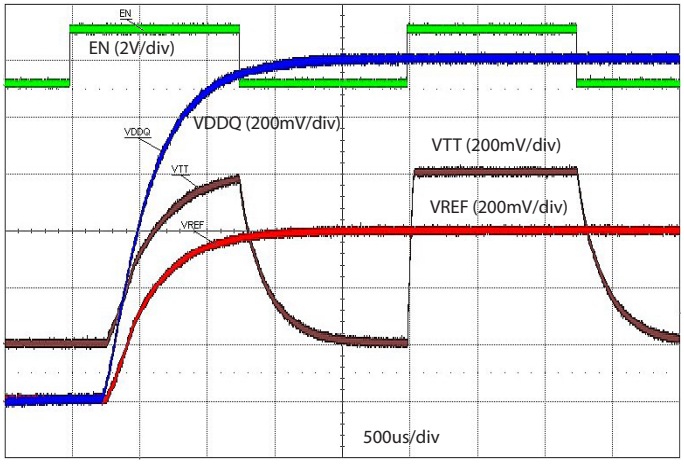


Typical Characteristics

Characteristics in this section are based upon the detailed application circuit on page 6.

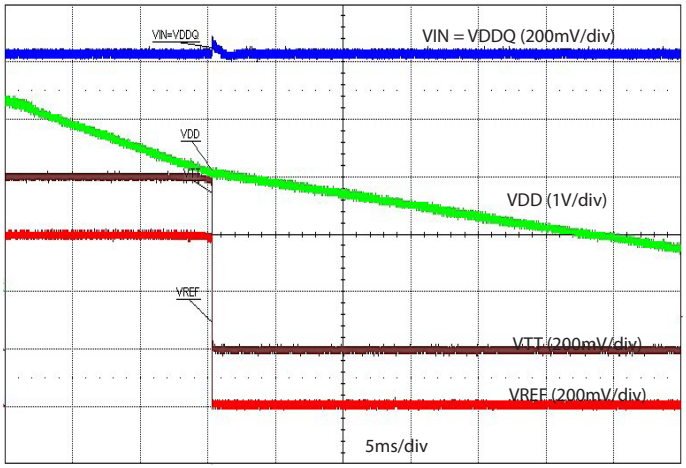
Start-Up and Shutdown Using EN

VIN = 1.2V, VDD = 3.3V, VREF = 0A, VTT = 0A



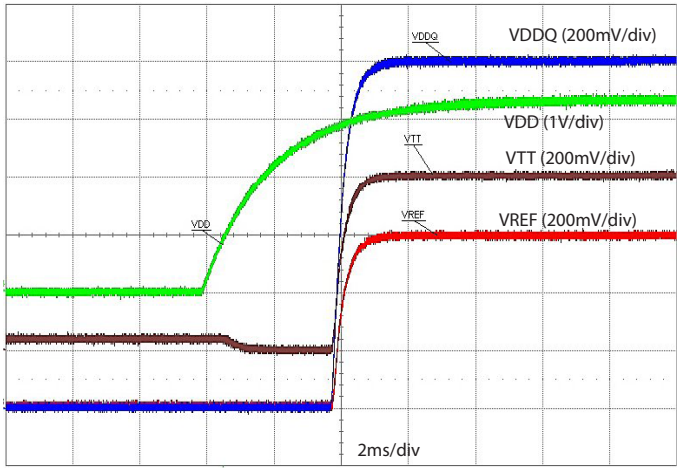
Shutdown Using VDD

VREF = 40mA, VTT = 1A



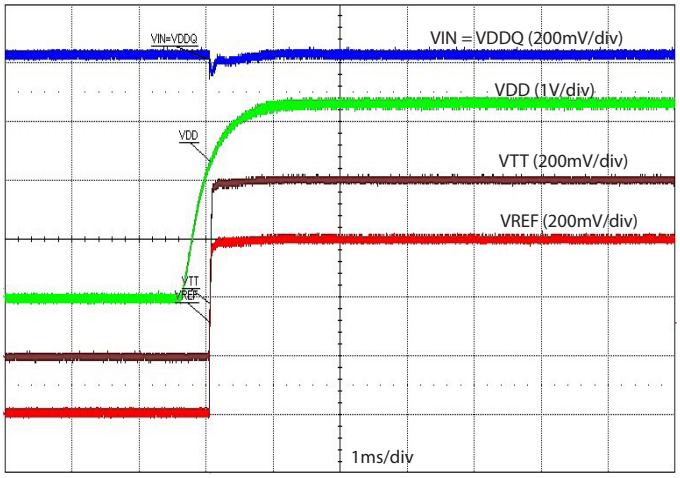
Start-Up Using VDDQ

VREF = 0A, VTT = 0A, VIN = 1.2V



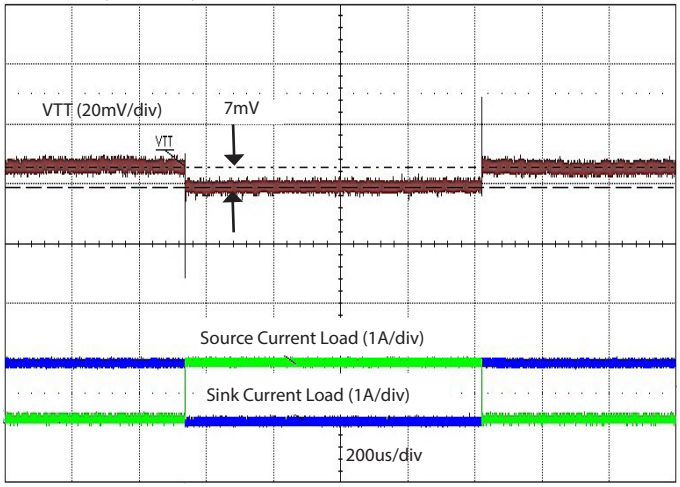
Start-Up Using VDD

VREF = 40mA, VTT = 1A



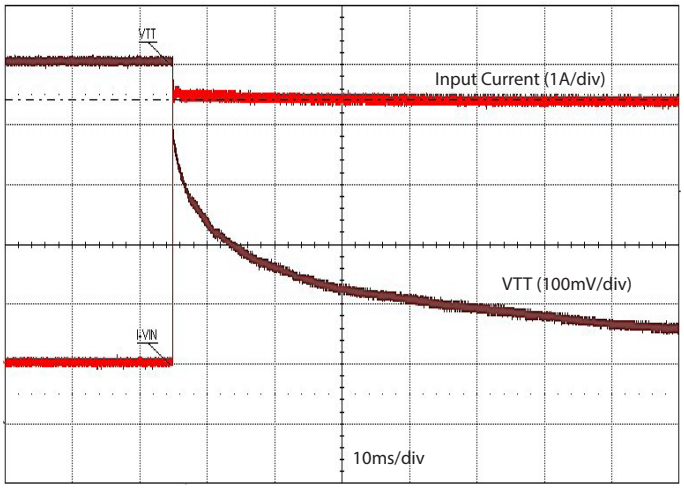
Load Transient Source and Sink: -1A to +1A

VDDQ = 1.2V, VIN = 1.2V, VDD = 3.3V



Current Limit with VTT Shorted

VDDQ = 1.2V, VIN = 1.2V, VDD = 3.3V



Applications Information

VTT Output

VTT starts to ramp up when EN and VDD meet their startup thresholds. SC2598 regulates VTT to the voltage at VREF and can support up to 3A for sourcing or sinking capability.

To achieve tight regulation and fast dynamic response at VTT, it is recommended to connect the VTTS sense signal to VTT at the ceramic output capacitors.

VREF Output

VREF starts to ramp up when VDD meets the UVLO threshold. SC2598 regulates VREF to one-half of VDDQ. To reduce the component count and provide a good accuracy reference for VTT, SC2598 includes an internal resistor divider network. SC2598 is capable of sinking or sourcing up to 40mA at VREF. To reduce the component count further, SC2598 does not require the user to have a local ceramic capacitor at the VREF pin - but it is recommended to layout with a capacitor place holder.

EN Input

The EN pin is used to enable and disable VTT only; it does not control VREF. When EN is pulled low, the VTT output is discharged internally to ground through an 8Ω FET.

Protection

SC2598 has thermal protection with auto-restart. When the junction temperature is above the thermal shutdown threshold (160°C), SC2598 disables VTT, while VREF remains present. When the junction temperature drops below the hysteretic window, typically at 140°C, SC2598 will be enabled again.

SC2598 has a built-in current limit feature to prevent damage to the sink and source FETs. If VTT is shorted to VDD or ground, SC2598 will sink or source current up to the current limit threshold.

Input Capacitor

The primary purpose of input capacitance is to provide the charge to the VTT output capacitor when there is a load transient at VTT. In the typical application circuit, VDDQ equals VIN, and VTT equals one-half of VDDQ. As a result, theory tells us that the input capacitance can be chosen to be half of the output capacitance.

Ceramic capacitors have a capacitance value that degrades with temperature, DC and AC bias, and their chemistry. Usually, ceramic capacitors need to be derated by 50% when operated at their rated DC voltage. Therefore, it is recommended to use capacitors with a voltage rating of 6.3V or higher for 3.3V or lower applications.

Stability and VTT Capacitor

Figure 1 shows the small signal model for the sourcing current loop stability. The low frequency pole is formed by C_{OUT} and R_L. Since this pole depends on those variables, it is recommended to have at least one 10uF ceramic capacitor at C_{OUT} for stability. Additional 10uF capacitors can be added to improve the transient response. SC2598 has an internal compensation network to ensure the stability as the load changes.

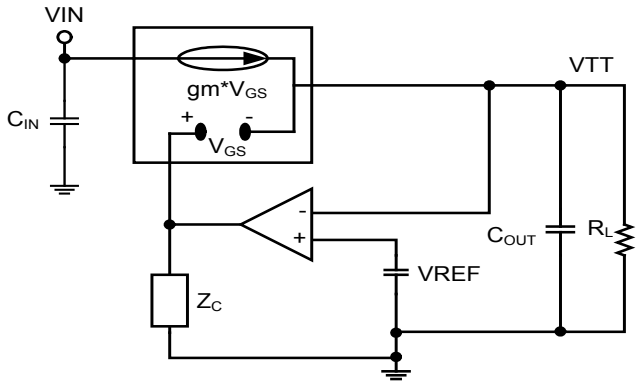


Figure 1 — Small Signal Model

Figure 2 shows the bode plot with the crossover frequency at around 0.8MHz and 36 degree phase margin. Another parameter affecting the loop stability is parasitic inductance in the PCB layout and output capacitor (ESL). The gain plot shows a peaking around 2.5 MHz after the crossover frequency due to the effect of ESL. Minimizing the ESL reduces this peaking and shifts it to a higher frequency. In addition to following the layout guidelines below, it is recommended that any VTT capacitor have a self-resonant frequency (SRF) greater than 1 MHz. This

criteria is met by selecting a capacitor with capacitance C and ESL satisfying the following condition:

$$\frac{1}{2\pi\sqrt{ESL \cdot C}} > 1\ MHz$$

The capacitor manufacturer should provide an ESL or SRF value or an impedance vs frequency curve where the minimum value occurs at the SRF. In general, a larger capacitor will have more ESL and therefore higher SRF, so a ceramic capacitor sized 0805 or smaller is recommended.

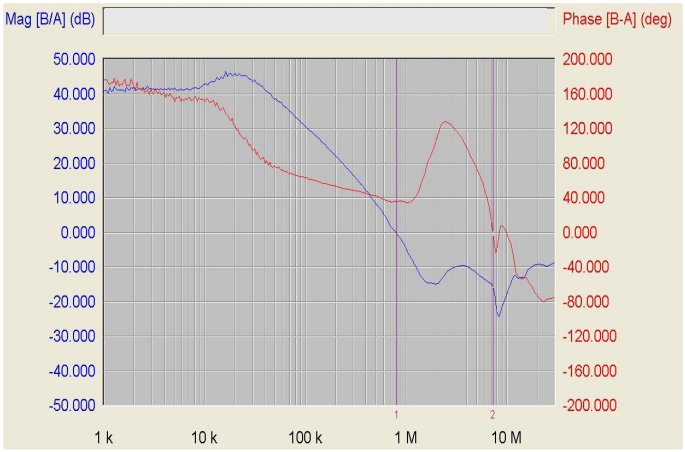


Figure 2 — Gain and Phase Bode Plot
Fc = 810KHz, PM = 36 degree at 1A Source

PCB Layout

The SC2598 requires minimal external components to provide a VTT solution. Figure 3 shows the component placement and layout for the application circuit on page 6. The SC2598 thermal pad is not electrically connected internally and does not require to be connected to GND. For optimal thermal performance, connect to the GND plane using multiple vias.

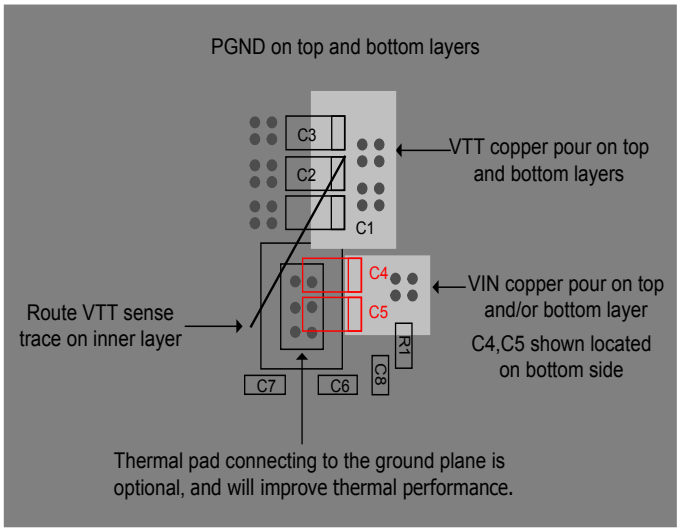


Figure 3 — Component Placement and Layout

Critical Layout Guidelines

Bias and Reference Capacitors:

A 1µF capacitor must be placed as close as possible to the IC and connected between pin 6 (VDD) and the ground plane.

A place holder for a 0.1µF capacitor should be placed as close as possible to the IC and connected between pin 4 (VREF) and the ground plane. This capacitor is optional, but it is recommended to layout with a capacitor place holder.

VDDQ Reference Capacitor:

An R-C filter from the supply used for VDDQ consisting of a 100 Ω resistor and a 0.1µF capacitor should be placed as close as possible to the IC and connected between pin 5 (VDDQ) and the ground plane, as shown on page 6.

VTT and VIN Capacitors:

Since SC2598 provides both sink and source capabilities, the loop impedance through the input and VTT capacitors plays an important role in circuit stability. Figure 4 shows both sink and source current loops. Close attention to board layout is needed to reduce ESL in these loops.

During a bode plot measurement for the sourcing current loop, an injected small AC signal flows around the loop from C_{IN} to Q_T through C_{VTT} and then returns to C_{VIN} through the ground plane. Therefore, it is recommended to keep the C_{IN} and C_{VTT} capacitors as close as possible to reduce the ESL impedance between them. Similarly in the sinking current loop, an injected small AC signal flows from C_{VTT} through Q_B and then returns to C_{VTT} through the GND plane. Therefore, it is recommended to keep ESL small for this loop. Balancing the ESL of those loops gives the best-case for stability.

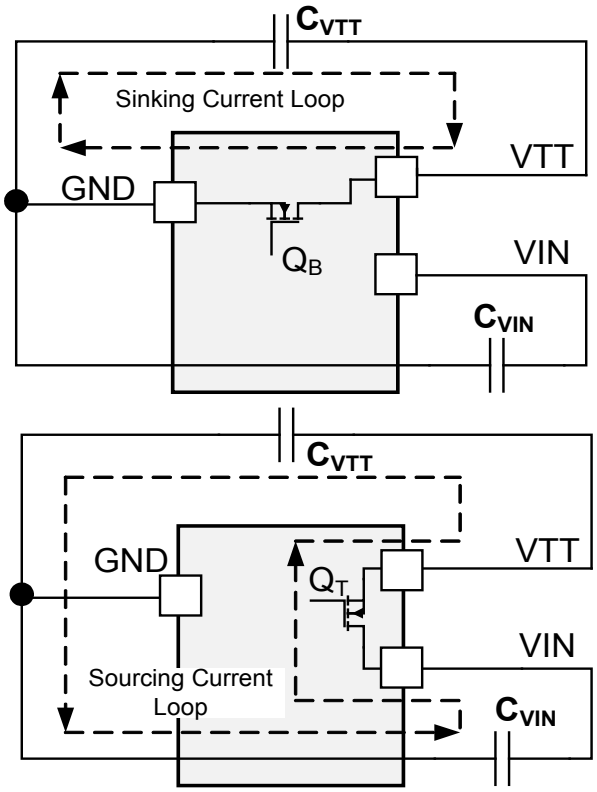
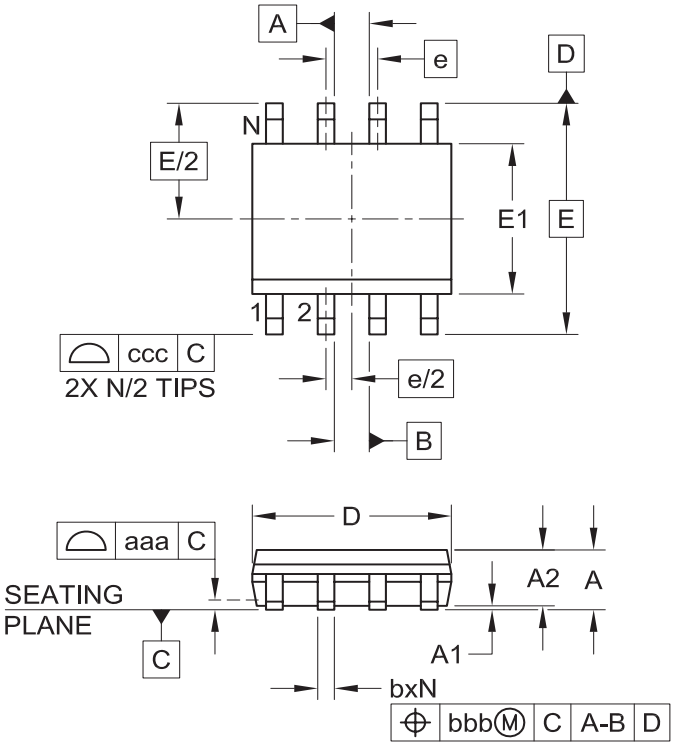
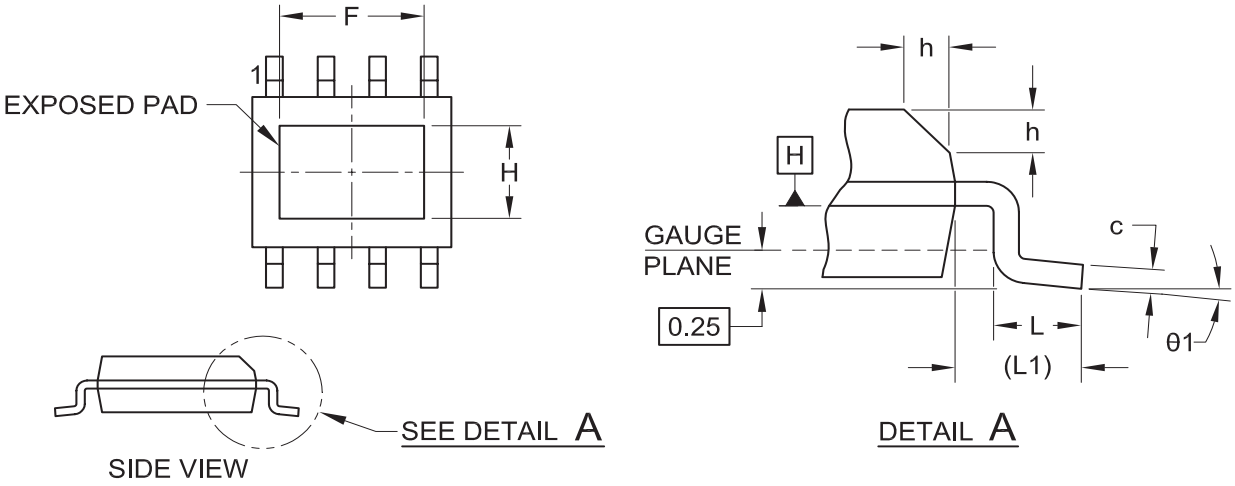


Figure 4 — Small AC Signal Current Loops

Outline Drawing — SOIC8-EDP



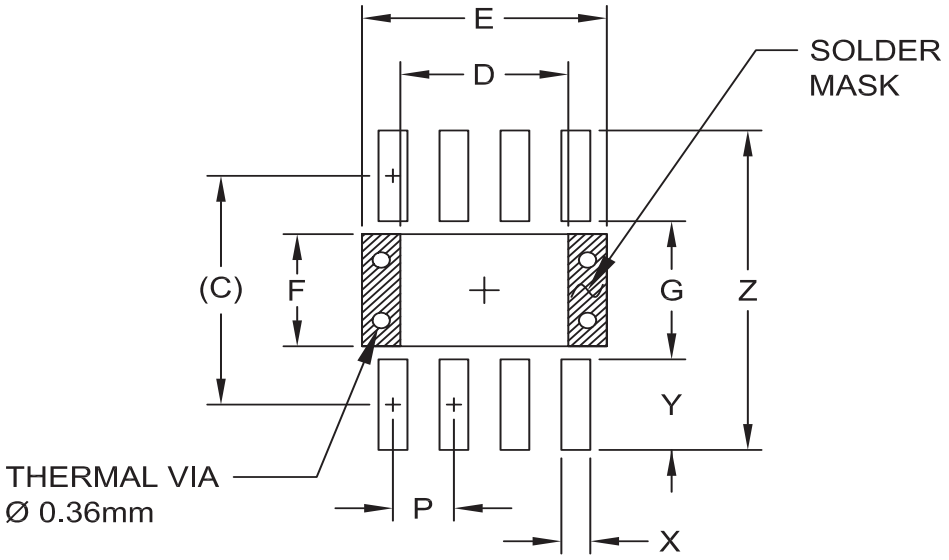
DIMENSIONS			
DIM	MILLIMETERS		
	MIN	NOM	MAX
A	1.25	—	1.75
A1	0.00	—	0.15
A2	1.25	—	1.65
b	0.31	—	0.51
c	0.17	—	0.25
D	4.80	4.90	5.00
E	6.00 BSC		
E1	3.80	3.90	4.00
e	1.27 BSC		
F	2.95	—	3.85
H	2.15	—	2.70
h	0.25	—	0.50
L	0.40	0.72	1.27
L1	(1.05)		
N	8		
θ1	0°	—	8°
aaa	0.10		
bbb	0.25		
ccc	0.25		



NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H- .
3. DIMENSIONS "E1" AND "D" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
4. THE MEASUREMENT OF DIMENSION "F" DOES NOT INCLUDE EXPOSED TIE BAR.

Land Pattern — SOIC8-EDP



DIMENSIONS	
DIM	MILLIMETERS
C	(5.30)
D	3.50
E	5.10
F	2.60
G	3.20
P	1.27
X	0.60
Y	2.10
Z	7.40

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. THIS LAND PATTERN IS FOR REFERENCE PURPOSE ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.
3. THERMAL VIAS IN THE LAND PATTERN OF THE EXPOSED PAD SHALL BE CONNECTED TO A SYSTEM GROUND PLANE. FAILURE TO DO SO MAY COMPROMISE THE THERMAL AND/OR FUNCTIONAL PERFORMANCE OF THE DEVICE.
4. REFERENCE IPC-SM-782A, SECTION 9.1, RLP NO. 300A.

Contact Information

Semtech Corporation
Power Mangement Products Division
200 Flynn Road, Camarillo, CA 93012
Phone: (805) 498-2111 Fax: (805) 498-3804

www.semtech.com