BGT24AR4

Silicon Germanium 24 GHz Quad Receiver MMIC

Data Sheet

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Final

RF & Protection Devices

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BGT24AR4 Silicon Germanium 24 GHz Quad Receiver MMIC

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Page	Subjects (major changes since last revision)

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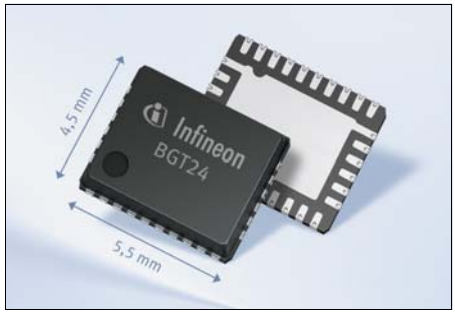


- Gilbert based quad homodyne 24 GHz downconverter with integrated IF filters and programmable gain base band amplifiers
- Single ended RF terminals
- Low single side band noise figure: NF_{ssb} = 10 dB typ.
- High downconverter P1dB input compression point: -6 dBm typ.
- Low LO input power required: -6 dBm
- On chip LO level and temperature sensors
- Muliplexed output of analog sensor signals
- Integrated saturation detectors for downconverters and IF amplifiers
- Disable mode for downconverter and base band amplifiers via SPI
- IF chain testability
- Single supply voltage: 3.3 V typ.
- Low power consumption: 610 mW typ.
- 200 GHz bipolar SiGe:C technology b7hf200
- Fully ESD protected device
- VQFN-32-9 leadless plastic package including lead-tip-inspection (LTI) feature
- Pb-free (RoHS compliant) package
- AEC Q100 qualified

RoHS

Description

The BGT24AR4 is a Silicon Germanium MMIC, accommodating four separate homodyne receiver chains. Each receiver consists of a downconverter operating in the 24 GHz ISM band. LO buffer amplifiers are included to relax LO drive requirements. IF signal filtering and amplification is provided on chip.

Saturation detectors for downconverter- and IF output signals as well as an IF chain test feature are integrated for monitoring purposes.

A temperature- and LO power sensor signal is accessible through a multiplexed analog output.

The following functionalities can be controlled via the 32 bit SPI bus:

- Enabling of downconverter and base band amplifiers
- Selection of base band amplifiers' gain
- Selection of the sensor signal being available through the analog output

Product Name	Package	Chip	Marking
BGT24AR4	VQFN32-9	T1825	BGT24AR4

The MMIC is manufactured in a 200GHz, 0.18µm SiGe:C technology and is packaged in a 32 pin leadless RoHs compliant VQFN package with lead-tip-inspection (LTI) feature.

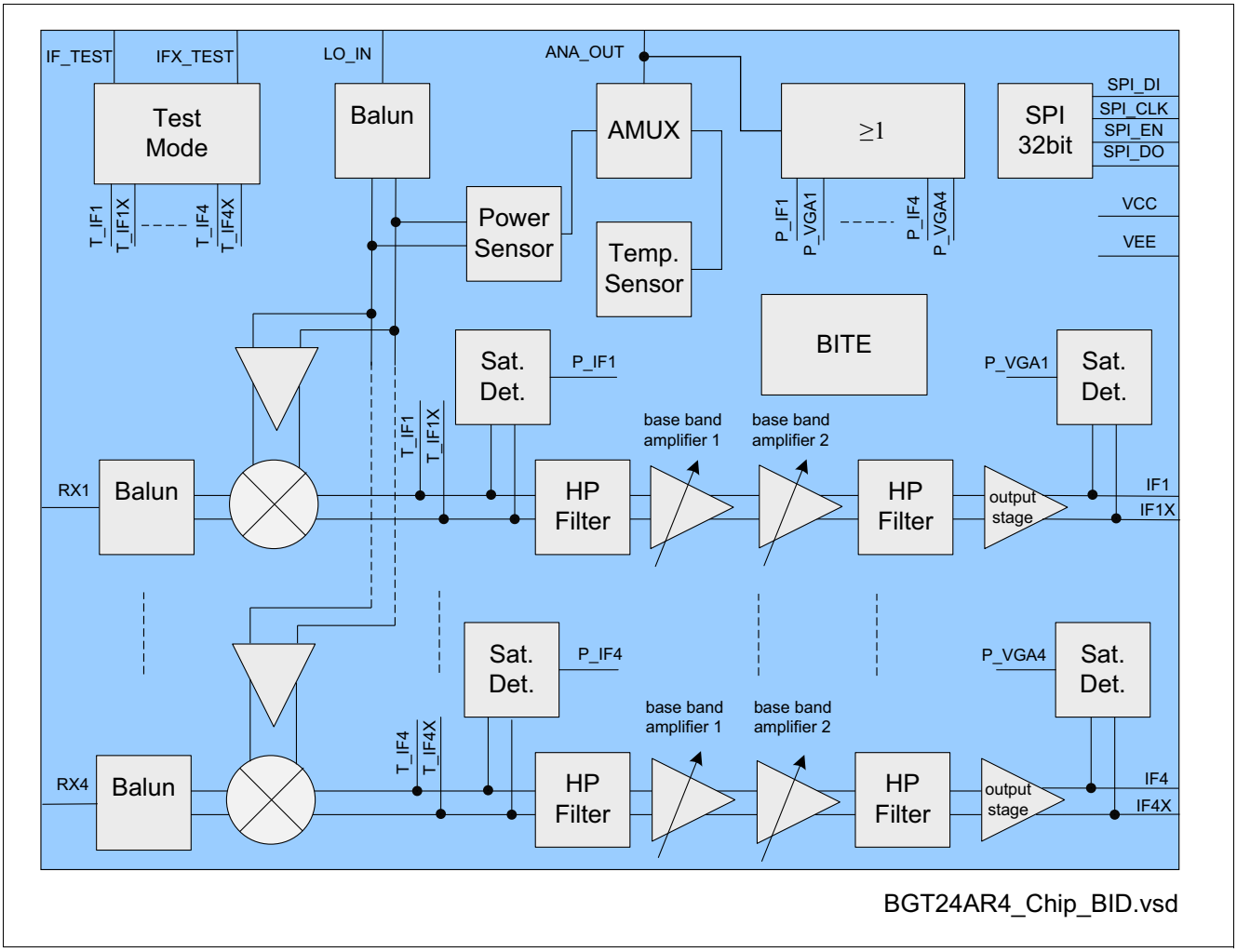


Figure 1 BGT24AR4 Block Diagram

2 Electrical Characteristics

2.1 Absolute Maximum Ratings

Table 1 **Absolute Maximum Ratings,** T_A = -40 °C to 125 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Test	Note / Test Condition
		Min.	Typ.	Max.			
Supply voltage	V_{CC}	-0.3	–	V_{cc}+0.3	V	■	–
DC voltage at RF pins	VDC_{RF}	–	–	0	V	■	MMIC provides short circuit to GND for LO_IN and RX1 to RX4 pins
RF input power	P_{RF}	–	–	0	dBm	■	–
LO input power	P_{LO}	–	–	12	dBm	■	–
Voltage applied to none-RF pins[1)]	V_{IO}	-0.3	–	V_{cc}+0.3	V	■	–
Total power dissipation	P_{DISS}	–	–	1200	mW	■	–
Junction temperature	T_J	-40	–	170	°C	■	–
Ambient temperature range	T_A	-40	–	125	°C	■	T_A = temperature at package soldering point
Storage temperature range	T_{STG}	-50	–	125	°C	■	–

1) For SPI_EN, SPI_DI, SPI_CLK the applied voltage may exceed given ratings als long as current into these pins is limited to I_{SPI} = 1 mA

Attention: Stresses exceeding the maximum values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

Attention: Integrated protection functions are designed to prevent IC destruction under fault conditions as described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.

Attention: Test ■ means that the parameter is not subject to production test. It was verified by design / characterization.

Note: ***No permanent damage of the device is possible due to an undefined SPI state***

2.2 ESD Integrity

Table 2 ESD Integrity

Parameter	Symbol	Values			Unit	Test	Note / Test Condition
		Min.	Typ.	Max.			
ESD robustness HBM[1)]	$V_{ESD-HBM}$	-1	–	1	kV	■	All pins
ESD robustness, CDM[2)]	$V_{ESD-CBM}$	-500	–	500	V	■	All pins
		-750	–	750		■	Package corner pins

1) According to ANSI/ESDA/JEDEC JS-001 (R = 1.5kOhm, C = 100pF) for Electrostatic Discharge Sensitivity Testing, Human Body Model (HBM)-Component Level

2) According to JEDEC JESD22-C101 Field-Induced Charged Device Model (CDM), Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components
Please note that this result is subject to:
- lot variations within the manufacturing process as specified by Infineon
- changes in the specific test setup

Attention: Test ■ means that the parameter is not subject to production test. It was verified by design / characterization.

2.3 Power Supply

Table 3 Electrical Characteristics, T_A = -40 °C ... 125 °C, positive current flowing into pin (unless otherwise specified)**.**

Parameter	Symbol	Values			Unit	Test	Note / Test Condition
		Min.	Typ.	Max.			
Supply voltage	V_{CC}	3.135	3.3	3.465	V		–
Supply current	I_{CC}	–	185	220	mA		SPI state: 0025 CC25 Hex no RF signal present
Supply current standby mode	$I_{CCstandby}$	–	–	35	mA		SPI state:0000 CC00 Hex

2.4 RX Characteristics

Table 4 **Electrical Characteristics** , V_{CC} = 3.135 V to 3.465 V, T_A = -40 °C to 125 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified), parameters specified in the frequency range from 24 GHz to 24.25 GHz including a matching structure and package footprint provided by Infineon using the high frequency laminate Rogers 4350B (see AN358)

Parameter	Symbol	Values			Unit	Test	Note / Test Condition
		Min.	Typ.	Max.			
RF frequency range	f_{RF}	24.00	24.125	24.250	GHz	■	–
RF input impedance	Z_{RF}	–	50	–	Ω	■	Single ended inclu - ding off chip compen- sation
Input return loss RF port RX1, RX4 RX2, RX3	RL_{RF}	 12 9	 – –	 – –	dB	■	V_{CC} = 3.3 V, T_A = 25 °C, P_{LO} = 0 dBm
RF/RF isolation (channel separation)	$I_{RF,RF}$	35	–	–	dB	■	not valid for RX1/ RX2
RF_{RX1}/ RF_{RX2} isolation (channel separation)	I_{RF_RX1,RF_RX2}	32	–	–	dB	■	–
LO/RF leakage	$L_{LO,RF}$	–	–	-27	dBm	■	P_{LO} = 0 dBm
Mixer's P1dB @ RF inputs	$P_{1dB\ IN}$	-7	-6	–	dBm	■	–
RX channel gain: power gain voltage gain	 G_P G_V	 39.2 47	 42.2 50	 47.2 55	 dB dB		At IF load 300 Ω differential
RX channel gain variation	ΔG	-1	0	1	dB		Channel to channel
RX channel phase variation	$\Delta\varphi$	-3	0	3	deg		Channel to channel
RX channel noise figure	NF	–	10.0	14.1	dB		At IF load 300 Ω differential
RX channel output full scale	V_{RX}	1.2	–	–	V_{PP}		At IF load 300 Ω differential
RX channel spurious free range at output full scale	a_{RX}	50	–	–	dBc		–
IF VGA gain adjustment range	R_{VGA}	-18	–	0	dB		With 6 dB gain steps
IF high pass filter's cut off frequency	$f_{cut\ off}$	525	600	675	kHz		3 dB definition
IF high pass filter's lower slope order		–	2nd	–	–	■	–
IF output impedance	Z_{IF}	250	300	350	Ω	■	–
IF test signal frequency	f_{IF}	100	–	5000	kHz	■	–
IF test signal level	V_{IF}	2	4	6	mV_{RMS}	■	–
IF test signal input impedance	$Z_{IF,test}$	500	1000	1400	Ω	■	–

Table 4 **Electrical Characteristics** (cont'd), V_{CC} = 3.135 V to 3.465 V, T_A = -40 °C to 125 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified), parameters specified in the frequency range from 24 GHz to 24.25 GHz including a matching structure and package footprint provided by Infineon using the high frequency laminate Rogers 4350B (see AN358)

Parameter	Symbol	Values			Unit	Test	Note / Test Condition
		Min.	Typ.	Max.			
IF output common mode voltage	V_{IF_CM}	1.4	–	2.4	V		At IF load 300 Ω differential, steady state
IF test voltage conversion gain	G_{IF_TEST}	34	39	43	dB		At f = 2 MHz, IF load 300 Ω differential, max. gain settings
Step response characteristics: Maximum overshoot voltage at single IF line in reference to GND	$V^{max}_{IF\_CM}$	–	–	V_{IF_CM} +0.76	V	■	At IF load 300 Ω differential
Step response characteristics: Minimum overshoot voltage at single IF line in reference to GND	$V^{min}_{IF\_CM}$	V_{IF_CM} -0.93	–	–	V	■	At IF load 300 Ω differential
Step response characteristics: Maximum slew rate	SR	–	–	106	V/µs	■	At IF load 300 Ω differential
Step response characteristics: Settling time	T_S	–	–	5.5	µs	■	At V_{IF_CM} = ±10 mV, P_{RFmax} = -20 dBm, IF load 300 Ω differential
Standby to ON mode transition slew rate at single IF line in reference to GND	SR_ON	–	–	55	V/µs	■	At IF load 300 Ω differential
IF power supply ripple rejection	$PSRR_{IF}$	40	–	–	dB	■	f_{IF} ≤ 5 MHz V_{CC} = 3.3 V, T_A = 25 °C

Note: - Test signal can be switched off (via SPI)
- Test signal can be switched to one RX channel (via SPI)
- Test signal can be switched to all RX channels (via SPI)

Attention: Test ■ means that the parameter is not subject to production test. It was verified by design / characterization.

2.5 LO Characteristics

Table 5 **Electrical Characteristics,** V_{CC} = 3.135 V to 3.465 V, T_A = -40 °C to 125 °C , all voltages with respect to ground, positive current flowing into pin (unless otherwise specified), parameters specified in the frequency range from 24 GHz to 24.25 GHz include a matching structure and package footprint provided by Infineon using the high frequency laminate Rogers 4350B (see AN358)

Parameter	Symbol	Values			Unit	Test	Note / Test Condition
		Min.	Typ.	Max.			
LO frequency range	f_{LO}	24.00	24.125	24.250	GHz	■	–
LO input power	P_{LO}	-6	–	3	dBm	■	–
Input return loss LO port	RL_{LO}	8	–	–	dB	■	V_{CC} = 3.3 V, T_A = 25 °C, P_{LO} = 0 dBm
LO input impedance	Z_{LO}	–	50	–	Ω	■	Single ended including off chip compensation

Attention: Test ■ means that the parameter is not subject to production test. It was verified by design / characterization.

2.6 IF Saturation Detector

Table 6 **Electrical Characteristics,** V_{CC} = 3.135 V to 3.465 V, T_A = -40 °C to 125 °C , all voltages with respect to ground, positive current flowing into pin (unless otherwise specified), parameters specified in the frequency range from 24 GHz to 24.25 GHz include a matching structure and package footprint provided by Infineon using the high frequency laminate Rogers 4350B (see AN358)

Parameter	Symbol	Values			Unit	Test	Note / Test Condition
		Min.	Typ.	Max.			
Input RX (RF) activation power level of mixer output saturation flag	P_{SAT}	$P_{1dB\ IN}$ - 8	$P_{1dB\ IN}$ - 4	$P_{1dB\ IN}$	dBm	■	–
VGA output activation voltage level of VGA saturation flag	V_{SAT}	–	1.3	1.55	V_{PP}		At IF load 300 Ω differential
Low level output	$Sat\text{-}Flag_{low}$	–	–	0.8	V		–
High level output	$Sat\text{-}Flag_{high}$	2.4	–	–	V		–
Load capacitance	$CL_{Sat\text{-}Flag}$	–	–	30	pF	■	–
Load resistance	$RL_{Sat\text{-}Flag}$	10	–	–	kΩ	■	–
IF saturation flag setup time	$T\_setup_{Sat\text{-}Flag}$	–	–	22.5	ns	■	–
IF saturation flag hold time	$T\_hold_{Sat\text{-}Flag}$	–	–	22.5	ns	■	–

Note: All saturation detection signals are logical OR combined to one discrete output signal.

Attention: Test ■ means that the parameter is not subject to production test. It was verified by design / characterization.

2.7 Sensor Multiplexer

Table 7 **Electrical Characteristics,** V_{CC} = 3.135 V to 3.465 V, T_A = -40 °C to 125 °C, application and MMIC external circuit acc. to Application Note AN358, all voltages with respect to ground (unless otherwise specified)

Parameter	Symbol	Values			Unit	Test	Note / Test Condition
		Min.	Typ.	Max.			
Output impedance	R_{OUTmux}	–	20	40	Ω	■	at pin ANA_OUT; multiplexer output activated

Attention: Test ■ means that the parameter is not subject to production test. It was verified by design / characterization.

2.8 Temperature Sensor

Table 8 **Electrical Characteristics,** V_{CC} = 3.3 V, T_A = -40 °C to 125 °C, application and MMIC external circuit acc. to Application Note AN358, all voltages with respect to ground (unless otherwise specified)**.**

Parameter	Symbol	Values			Unit	Test	Note / Test Condition
		Min.	Typ.	Max.			
Temperature sensor operating range[1)]	T_{TSENS}	-40	–	125	°C	■	–
Output voltage	$V_{SENSE25}$	1.4	1.5	1.6	V		at T_{Si} = 25°C
Sensitivity[1)]	S_{TSENS}	4.3	4.7	5.1	mV/K	■	–
Setup time[1)]	t_{TSENS}	–	–	20	µs	■	C_{Load} ≤ 30 pF, R_{Load} ≥ 10 kΩ
Power supply rejection ratio	$PSRR$	10	24	–	dB	■	measured at T_{Si} = 25°C and $V_{CC,MIN}/V_{CC,MAX}$

1) Guaranteed by device design, not subject to production test

Attention: Test ■ means that the parameter is not subject to production test. It was verified by design / characterization.

3 Pin Description

Table 9 Pin Definition and Function

Pin No.	Name	Function
1	IF_TEST	IF test signal
2	VCC	Supply voltage
3	n.c	connected to ground acc. to AN358
4	LO_IN	LO input signal
5	n.c.	connected to ground acc. to AN358
6	SPI_DO	SPI data output
7	SPI_EN	SPI enable
8	SPI_CLK	SPI clock
9	SPI_DI	SPI data input
10	ANA_OUT	Analog output signal / saturation flag
11	VEE	Ground
12	RX1	RF input receiver 1
13	n.c.	connected to ground acc. to AN358
14	IF2X	Complementary IF output receiver 2
15	IF2	IF output receiver 2
16	IF1X	Complementary IF output receiver 1
17	IF1	IF output receiver 1
18	n.c.	connected to ground acc. to AN358
19	RX2	RF input receiver 2
20	n.c.	connected to ground acc. to AN358
21	VEE.	Ground
22	IFX_TEST	Complementary IF test signal
23	n.c.	connected to ground acc. to AN358
24	RX3	RF input receiver 3
25	n.c.	connected to ground acc. to AN358
26	IF4	IF output receiver 4
27	IF4X	Complementary IF output receiver 4
28	IF3	IF output receiver 3
29	IF3X	Complementary IF output receiver 3
30	VEE	Ground
31	RX4	RF input receiver 4
32	n.c.	connected to ground acc. to AN358

Table 10 I/O internal circuits

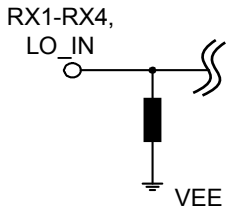
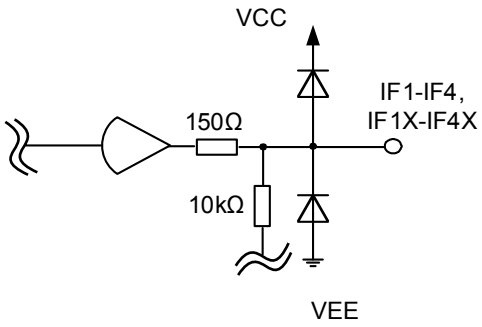
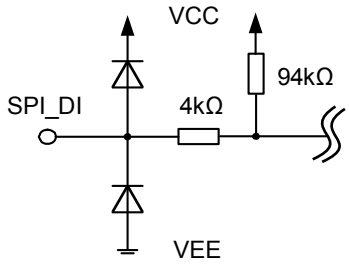
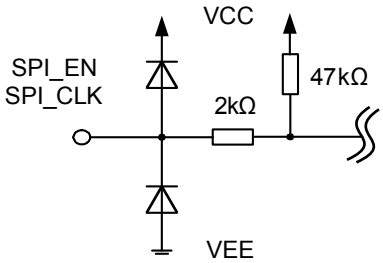
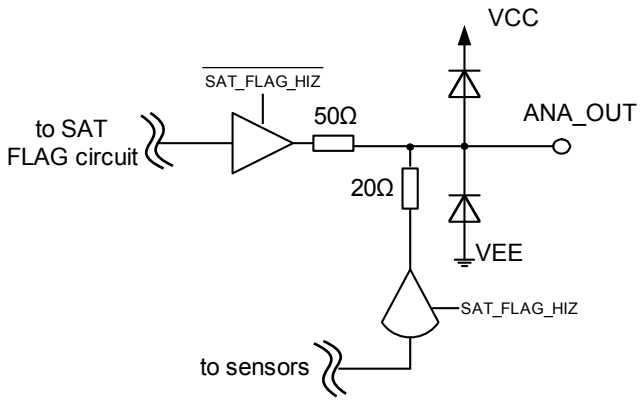
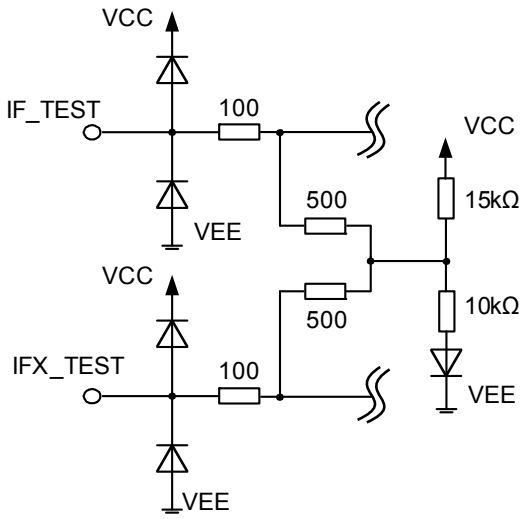
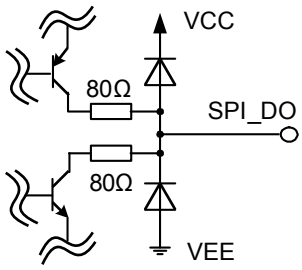
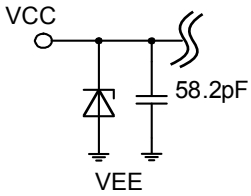
Pin No.	Name	I/O internal circuits
4, 12, 19, 24, 31	LO_IN, RX1, RX2, RX3, RX4	
14, 15, 16, 17, 26, 27, 28, 29	IF2X, IF2, IF1X, IF1, IF4, IF4X, IF3, IF3X	
9	SPI_DI	
7, 8	SPI_EN, SPI_CLK	

Table 10 I/O internal circuits

Pin No.	Name	I/O internal circuits
10	ANA_OUT	
1, 22	IF_TEST, IFX_TEST	
6	SPI_DO	
2	VCC	

4 SPI

Communication to the receiver is done via a Serial-Peripheral-Interface (SPI). The 32 bit SPI has a hardwired Power-On reset, which sets the output bits to a defined state after turning on the supply voltage. Data transmission is started by a negative edge on SPI_EN. Data at SPI_DI is then read at the falling edge of SPI_CLK. The most significant bit (MSB) is read first.

Table 11 SPI Data Bit Description

Data Bit	Name	Description (Logic High)	Power ON Reset State
0 (LSB)	EN_34	Enables mixer and base band amplifier output stage and supporting functions (for RX3 and RX4)	Low
1	LG1_	Activates 6dB gain stage of base band amplifier 1 (for RX3 and RX4	Low
2	HG1_34	Activates 12dB gain stage of base band amplifier 1 (for RX3 and RX4)	Low
3	LG2_34	Activates 6dB gain stage of base band amplifier 2 (for RX3 and RX4)	Low
4	MG2_34	Activates 12dB gain stage of base band amplifier 2 (for RX3 and RX4)	Low
5	HG2_34	Activates 18dB gain stage of base band amplifier 2 (for RX3 and RX4)	Low
6	IFTEST4	Activates test signal for IF channel 4	Low
7	IFTEST3	Activates test signal for IF channel 3	Low
8	IFTEST2	Activates test signal for IF channel 2	Low
9	IFTEST1	Activates test signal for IF channel 1	Low
10	PC1	Test bit	High
11	PC2	Test bit	High
12	EN_RF14	Test bit	Low
13	EN_RF23	Test bit	Low
14	DIS_DIV	Test bit	High
15	DIS_LO	Test bit	High
16	EN_12	Enables mixer and base band amplifier output stage and supporting functions (for RX1 and RX2	Low

Table 11 SPI Data Bit Description (cont'd)

Data Bit	Name	Description (Logic High)	Power ON Reset State
17	LG1_12	Activates 6dB gain stage of base band amplifier 1 (for RX1 and RX2)	Low
18	HG1_12	Activates 12dB gain stage of base band amplifier 1 (for RX1 and RX2)	Low
19	~~LG2_12~~	Activates 6dB gain stage of base band amplifier 2 (for RX1 and RX2	Low
20	MG2_12	Activates 12dB gain stage of base band amplifier 2 (for RX1 and RX2)	Low
21	HG2_12	Activates 18dB gain stage of base band amplifier 2 (for RX1 and RX2)	Low
22	AMUX_SEL0	Sets analog multiplexer	Low
23	AMUX_SEL1	Sets analog multiplexer	Low
24	AMUX_SEL2	MSB to set analog multiplexer	Low
25	SAT_FLAG_HIZ	Sets sat flag output into high impedance state and enables multiplexer output to be active	Low
26	DCO_3	Test bit	Low
27	SENSOR_SEL0	Selects power sensor signal	Low
28	SENSOR_SEL1	MSB to select power sensor signal	Low
29	DCO_0	Test bit	Low
30	DCO_1	Test bit	Low
31 (MSB)	DCO_2	Test bit	Low

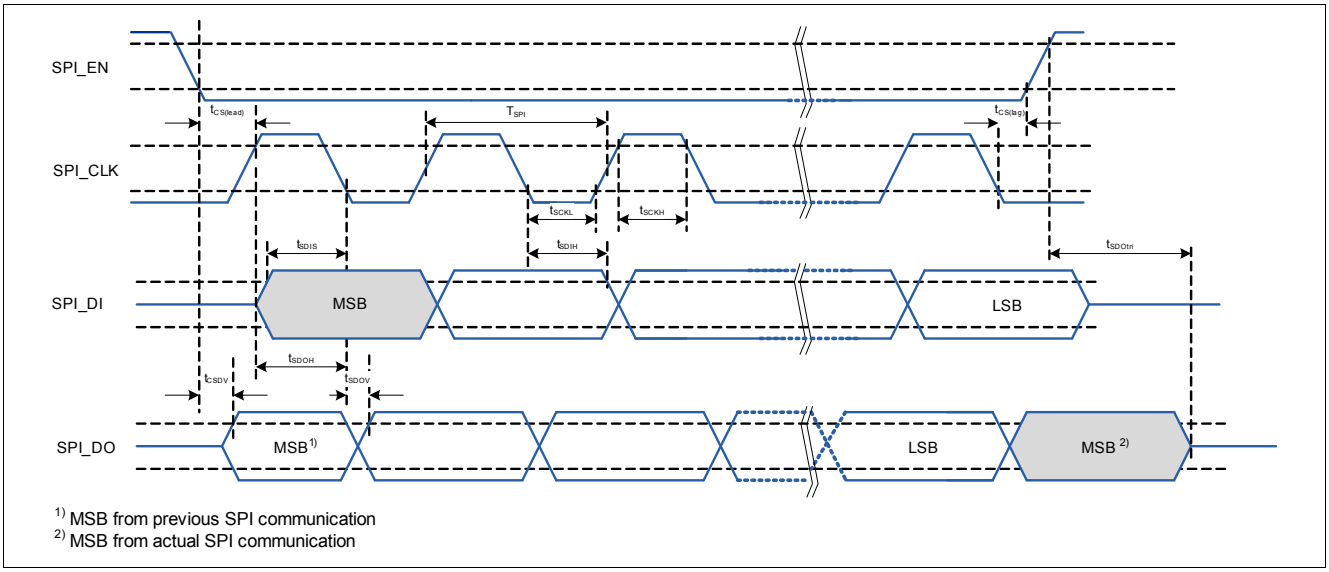


Figure 2 Timing Diagram of the SPI

Table 12 SPI Interface

Parameter	Symbol	Values			Unit	Test
		Min.	Typ.	Max.		
SPI_CLK period	t_{SPI}	50	–	–	ns	
SPI_CLK low time	t_{SCKL}	0.40 t_{SPI}	0.5 t_{SPI}	0.60 t_{SPI}	ns	■
SPI_CLK high time	t_{SCKH}	0.40 t_{SPI}	0.5 t_{SPI}	0.60 t_{SPI}	ns	■
Chip select lead time	$t_{CS(lead)}$	20	–	–	ns	■
Time between falling edge of SPI_CLK and SPI_DO valid	t_{SDOV}	–	–	30	ns	■
Setup time of SPI_DI before falling edge of SPI_CLK	t_{SDIS}	10	–	–	ns	■
Hold time of SPI_DI after falling edge of SPI_CLK	t_{SDIH}	10	–	–	ns	■
Hold time of SPI_DO with respect to subsequent falling edge of SPI_CLK	t_{SDOH}	0	–	–	ns	■
Hold time of SPI_EN after last falling edge of SPI_CLK	$t_{CS(lag)}$	20	–	–	ns	■
Delay between rising edge of SPI_EN and SPI_DO tristate (leakage current < 12µA)	t_{SDOtri}	–	–	100	ns	■
Delay between falling edge of SPI_EN and MSB at SPI_DO valid	t_{CSDV}	–	–	90	ns	■
Minimum time between two SPI commands	$t_{min2SPI}$	5	–	–	µs	■

Attention: Test ■ means that the parameter is not subject to production test. It was verified by design / characterization.

Table 13 Specification for SPI pins

Parameter	Symbol	Values			Unit	Test
		Min.	Typ.	Max.		
High level input voltage	V_{I_high}	2.0	–	–	V	■
Low level input voltage	V_{I_low}	–	–	0.8	V	■
Input voltage hysteresis	V_{hys}	50	–	–	mV	■
Input current	I_{IN}	-150	–	150	µA	
Input capacitance (EN, CLK, DI)	CS_{IN}	–	–	2	pF	■
SPI_DO output high voltage (VCC=3.3V,I_{SDO} =1mA)	V_{O_high}	2.4	–	–	V	
SPI_DO output low voltage (VCC=3.3V,I_{SDO} =1mA)	V_{O_low}	–	–	0.8	V	
SPI_DO load capacitance	$CSL\ DO$	–	–	30	pF	■
SPI_DO load resistance	$RSL\ DO$	10	–	–	kΩ	■
Pull Up resistor (SPI_DI) T_A = 25 °C	RPL_SPI_DI	78	98	118	kΩ	■
Pull Up resistor (SPI_CLK, SPI_EN) T_A = 25 °C	RPL_SPI_CLK, RPL_SPI_EN	39	49	59	kΩ	■
Leakage current @ SPI_DO in high Z state (Testvoltage 2.4 V)	$IL\ DO$	–	–	12	µA	

Attention: Test ■ means that the parameter is not subject to production test. It was verified by design / characterization.

5 Sensor Multiplexer

Output signals of the temperature and LO output level sensor are provided multiplexed at the output pin ANA_OUT using an analog multiplexer (AMUX) circuit.

Additionally, a MMIC internal band gap reference voltage can be read out.

Table 14 Truth Table AMUX [1)]

Output signal ANA_OUT	AMUX1_SEL2	AMUX1_SEL1	AMUX1_SEL0
Temperature sensor output voltage	0	0	X
Sensor Output (see **Table 15**)	0	1	0
Band gap voltage	1	0	0

1) No valid output for deviating states

Table 15 Sensor Configuration [1)]

Sensor Output	Sensor_SEL1	Sensor_SEL0
LO Power sensor	0	0

1) No valid output for deviating states

6 Package Dimensions

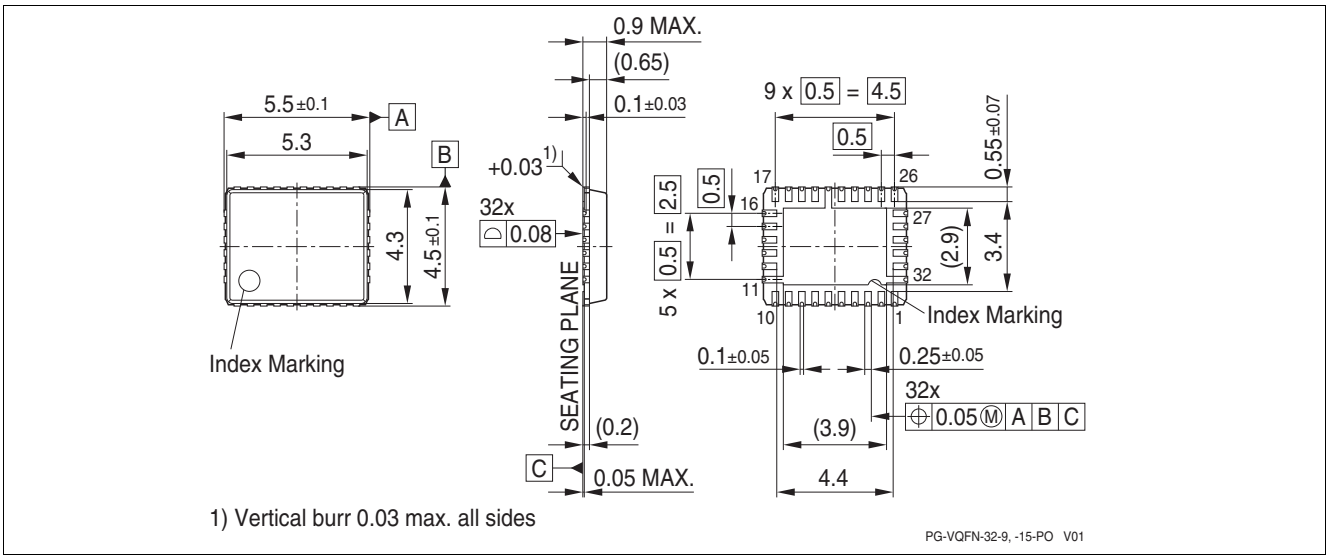


Figure 3 Package Outline (Top, Side and Bottom View) of VQFN32-9

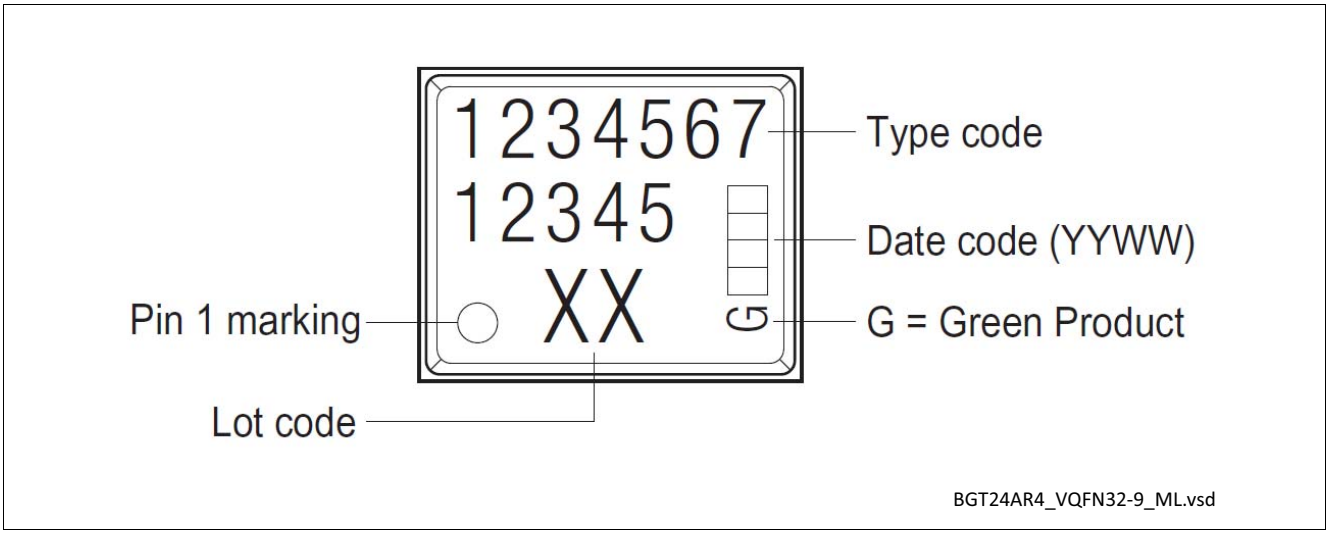


Figure 4 Marking Layout VQFN32-9 (example)

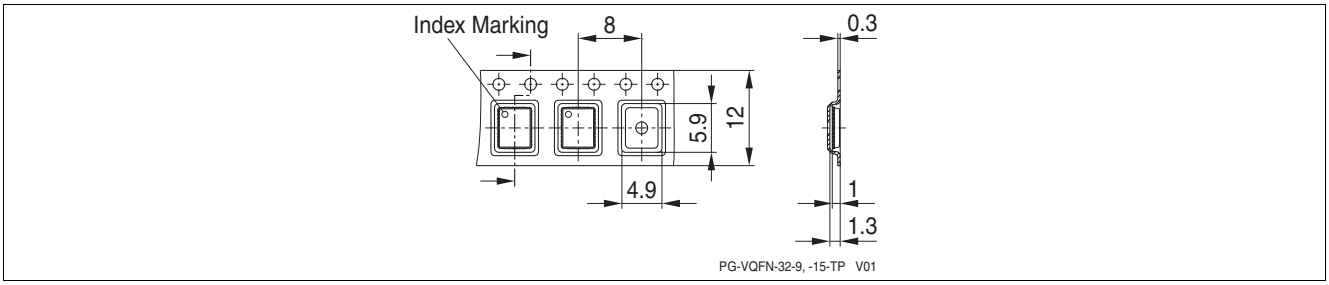


Figure 5 Tape of VQFN32-9, Ø Reel: 330 mm, Pieces / Reel: 3000, Reels / Box: 1

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