

27960KX

BURST ACCESS 1M (128K x 8) CHMOS EPROM

- Synchronous 4-Byte Data Burst Access
- Simple Interface to the 80960KA/KB
- High Performance Clock to Data Out
 - Zero Wait State Data-to-Data Burst
 - Supports 16, 20 and 25 MHz
 - 80960KA/KB Devices
- Asynch Microcontroller Reset Function
 - Returns to Known State with High Z Outputs
- CHMOS[®] III-E for High Performance and Low Power
 - 125 mA Active, 30 mA Standby
 - TTL Compatible Inputs
- 1 Mbit Density Configures as 128K x 8

Intel's 27960KX is a 5V only, 1,048,576 bit, Erasable Programmable Read Only Memory, organized as 128K words of 8 bits.

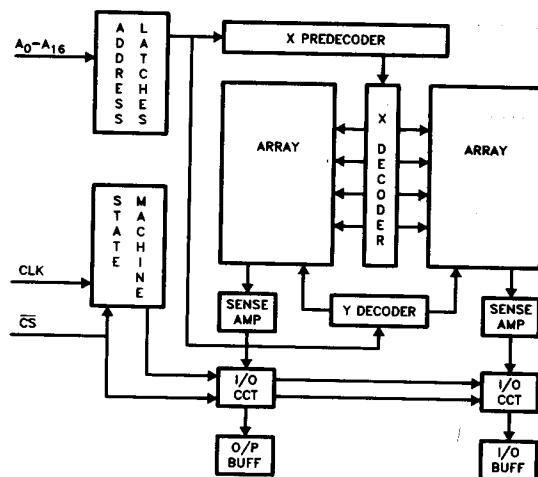
The 27960KX provides a simple synchronous burst interface to the 80960KA/KB bus. Internally the 27960KX is organized in 4 byte blocks, in which each byte is accessed sequentially. The internal state machine is factory configured to generate either 1 or 2 wait-states between the address and first data byte. High performance outputs provide zero wait-state data to data accesses at clock frequencies up to 25 MHz.

An asynchronous microcontroller ~~RESET~~ feature puts the outputs in the high impedance state and takes the internal state machine to a known state where a new burst access can begin.

The 27960KX is available in 44 lead PLCC package, providing optimum cost effectiveness.

The 27960KX is manufactured on Intel's 1 micron CHMOS III-E technology. The Quick-Pulse Programming™ algorithm provides fast, reliable programming with throughput under 17 seconds for optimized equipment.

^{*}CHMOS is a patented process of Intel Corporation.



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Figure 1. 27960KX Burst EPROM Block Diagram

27960KX BURST EPROM

EPROMs are established as the preferred code storage device in embedded applications. The non-volatile, flexible, reliable, cost effective EPROM makes a product easier to design, manufacture and service. Until recently, however, EPROMs could not match the performance needs of high-end systems. The 27960KX was designed to support the 80960KA/KB embedded processor. It utilizes the burst interface to offer near zero-wait state performance without the high cost normally associated with this performance.

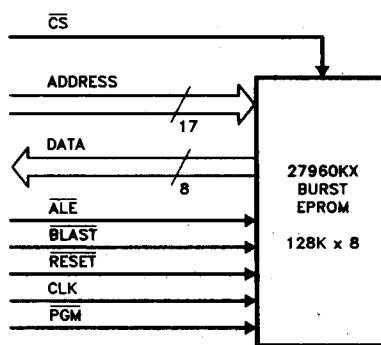
In embedded designs, board space and cost must be kept at a minimum without impacting performance and reliability. The 27960KX removes the need for expensive high-speed shadow RAM backed up by slow EPROM or ROM for non-volatile code storage. Code optimization concerns are reduced with "off-chip" code fetches no longer crippling to system performance. FONTS can be run directly out of these EPROMs at the same performance as high-speed DRAMs. With the 27960KX, the EPROM is the ideal code or FONT storage device for your 80960KA/KB system.

Architecture

The 27960KX provides a simple, synchronous burst interface to the 80960KA/KB's bus. Internally, the 27960KX is organized in 4 byte blocks each byte is accessed sequentially. A burst access begins on the first clock pulse after CS is asserted. The address of the four byte block is latched by the rising edge of ALE. After a preset number of wait-states (1 or 2), data is output one byte at a time on each subsequent clock cycle. A burst access is terminated on the rising edge of CLOCK if BLAST is asserted. High performance outputs provide zero wait-state data to data accesses at clock frequencies up to 25 MHz. Extra power and ground pins dedicated to the outputs reduce the effects of fast output switching on device performance.

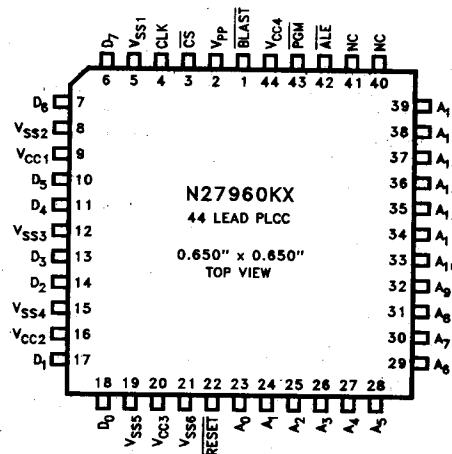
The 27960KX delivers 4 bytes of data in 8 clock cycles at 25 MHz and 4 bytes of data in 7 clock cycles at 20 MHz. In a 32-bit configuration, this translates into a read bandwidth of 50 Mbytes/sec and 45 Mbytes/sec respectively. Performance capability of the 27960KX in different 80960KA/KB systems is given in Table 1.

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Figure 2. 27960KX Burst EPROM Signal Set



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Figure 3. 27960KX 44-Lead PLCC Pinout

PIN DESCRIPTIONS

Symbol	Pin	Function
A ₀ -A ₁₆ :	23-39	ADDRESS INPUTS: During a burst operation, A ₂ through A ₁₆ provide the base address pointing to a block of four consecutive bytes. A ₀ and A ₁ select the first byte of the burst access. The 27960KX latches valid addresses in the first clock cycle. An internal address generator increments addresses A ₀ and A ₁ for subsequent bytes of the burst.
D ₀ -D ₇ :	18, 17, 14, 13, 11, 10, 7, 6	DATA INPUTS/OUTPUTS
ALE	42	ADDRESS LATCH ENABLE: Indicates the transfer of a physical address. ALE is an active low signal used to latch the addresses from the processor. Addresses are latched on the rising edge of ALE. Valid addresses must be present at or before ALE becomes valid.
CS	3	CHIP SELECT: Master device enable. When asserted (active low) data can be written to and read from the device. In read mode, CS enables the state machine and the I/O circuitry.
		NOTES: <ol style="list-style-type: none"> 1. The address decode path is independent of CS, i.e., X and Y decoding is always powered up. 2. For programming, CS should remain low for the entire cycle. Program and verify functions are done one byte at a time. 3. CS going high does not terminate a concurrent burst cycle. 4. CS must be deasserted between bursts.
BLAST	1	BURST LAST: Terminates a concurrent burst data cycle at the rising edge of the CLK. It must be asserted by the fourth data byte.
RESET	22	RESET: Resets the state machine into a known state, tri-states the outputs. The duration of RESET should be 10 CLK cycles minimum. At least 5 clock cycles are required after deassertion of RESET before beginning the next cycle. Reset will abort a concurrent bus cycle.

PIN DESCRIPTIONS (Continued)

Symbol	Pin	Function
PGM	43	PROGRAM-PULSE CONTROL INPUT
V _{PP}	2	PROGRAMMING POWER SUPPLY V _{PP}
V _{SS}	5, 8, 12, 15, 19, 21	GROUND
V _{CC}	9, 16, 20, 44	SUPPLY VOLTAGE INPUT

Table 1. Performance Capability

25/20 MHz 2 WS NON-BUFFERED : 4 WORDS/8 CLOCK CYCLES → 50/40 MBYTES/SEC

ADDR	A ₀₀	WS	WS	-	-	-	RS	A ₀₁	WS	WS	-	-	-	RS
DATA	-	-	-	D ₀₀	D ₀₁	D ₀₂	D ₀₃	-	-	-	-	-	D ₁₀	D ₁₁
CLK	C ₁	C ₂	C ₃	C ₄	C ₅	C ₆	C ₇	C ₁	C ₂	C ₃	C ₄	C ₅	C ₆	C ₇

20 MHz 1 WS NON-BUFFERED : 4 WORDS/7 CLOCK CYCLES → 45 MBYTES/SEC

ADDR	A ₀₀	WS	-	-	-	RS	A ₀₁	WS	-	-	-	-	RS	A ₀₃	WS
DATA	-	-	D ₀₀	D ₀₁	D ₀₂	D ₀₃	-	-	-	D ₁₀	D ₁₁	D ₁₂	D ₁₃	-	
CLK	C ₁	C ₂	C ₃	C ₄	C ₅	C ₆	C ₇	C ₁	C ₂	C ₃	C ₄	C ₅	C ₆	C ₇	

16 MHz 1 WS BUFFERED : 4 WORDS/7 CLOCK CYCLES → 36 MBYTES/SEC

ADDR	A ₀₀	WS	-	-	-	RS	A ₀₁	WS	-	-	-	-	RS	A ₀₃	WS
DATA	-	-	D ₀₀	D ₀₁	D ₀₂	D ₀₃	-	-	-	D ₁₀	D ₁₁	D ₁₂	D ₁₃	-	
CLK	C ₁	C ₂	C ₃	C ₄	C ₅	C ₆	C ₇	C ₁	C ₂	C ₃	C ₄	C ₅	C ₆	C ₇	

INTERFACE EXAMPLE

Overview

The following design offers a simple interface to the 80960KA/KB's bus.

A non-buffered 27960KX burst EPROM system is shown in Figure 4. Since the 27960KX is capable of driving a 120 pF load, large, non-buffered systems can be implemented by stacking up to 2 banks of 4 EPROMs, giving a memory size of 256K x 32. The input capacitive load seen on the address lines (due to the EPROM only) is 24 pF for a 128K x 32

system (shown) and 48 pF for a 256K x 32 system. The EPROM is specified at 4 pF for input capacitance and 12 pF typical for output capacitance. Larger systems can be implemented with buffers.

Chip Select Logic

High order address lines are decoded to provide CS. Qualification with other signals is not required. The chip select logic can be implemented with standard asynchronous decoders, PAL's or PLD's (like Intel's 85C960).

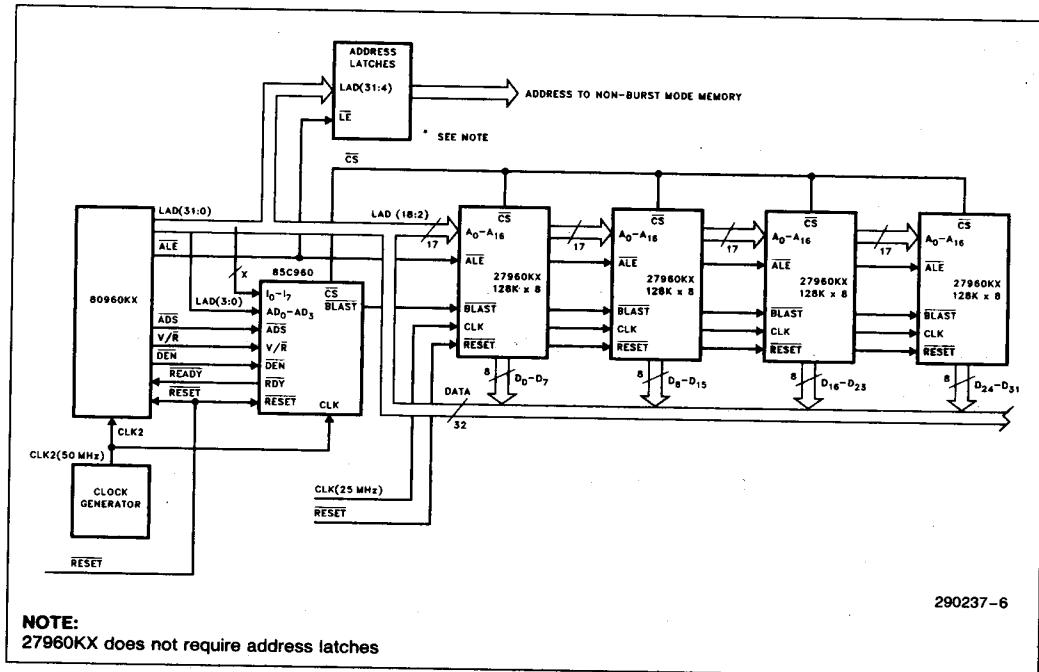


Figure 4. 128K x 32 Burst EPROM System

Waveforms

Figure 5 shows the timing waveforms of 27960KX reads in a 32-bit system.

CS setup time

\overline{CS} setup time is the time between \overline{CS} asserted and the first rising CLK edge of CLK (during the address cycle). Since a memory access begins on the first CLK rising edge after \overline{CS} asserted, a minimum \overline{CS} setup time of 5 ns (t_{SVCH}) at 25 MHz is required. With the 80960KA/KB's maximum valid address delay of 18 ns at 25 MHz, 13 ns remains for \overline{CS} decoding logic.

CS Deassert between bursts

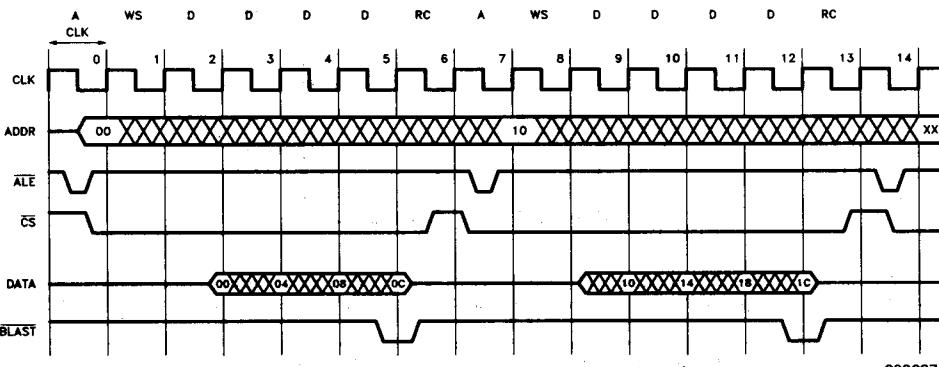
After every EPROM read (one to four words) \overline{CS} must be deasserted.

Reset and RESET

The 27960KX uses RESET. The 80960 KA/KB RESET signal must be inverted for the 27960KX.

Clock Phase

The initial rising edge of CLK and CLK2 must be in phase with as small a skew as possible.



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NOTES:

1. 1-0-0-0 Burst Read → 1 indicates the number of wait states to access the first word
0's indicate the number of wait states for subsequent data words (0 in this case)
2. 27960KX latches addresses on the rising edge of ALE: it has an internal address generator which increments addresses for subsequent words of the burst.

Figure 5. Two Cycles of a 27960KX 1 Wait State, 4-Byte Read (1-0-0-0 Burst Read) in a 32-Bit System**27960KX DEVICE NAMES**

The device names on the 27960KX were derived as mnemonics that correspond to the number of wait states and expected operating frequency for the device. For example, the 25 MHz, 2 wait state 27960KX is named 27960K2-25.

AC TIMING DERIVATIONS

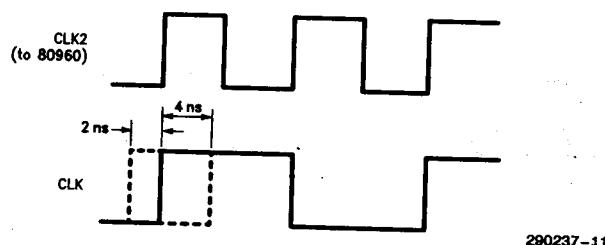
The AC timings for the 27960KX were generated specifically to meet the requirements of the 80960KA/KB microprocessor. In each case the applicable 80960KA/KB clock frequency and AC timing were taken together with an address buffer delay (if needed) and a 4 ns positive clock skew or a 2 ns negative clock skew (see Figure 6A) guardband to

generate the 27960KX AC timing. Worst case timings were always assumed. The example below shows how the 27960K1-20 t_{avc0h} timing was derived.

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@20 MHz the clock cycle is ~50 ns.
t₆ of the 80960KA/KB is 2-20 ns.
4 ns clock skew guardband.

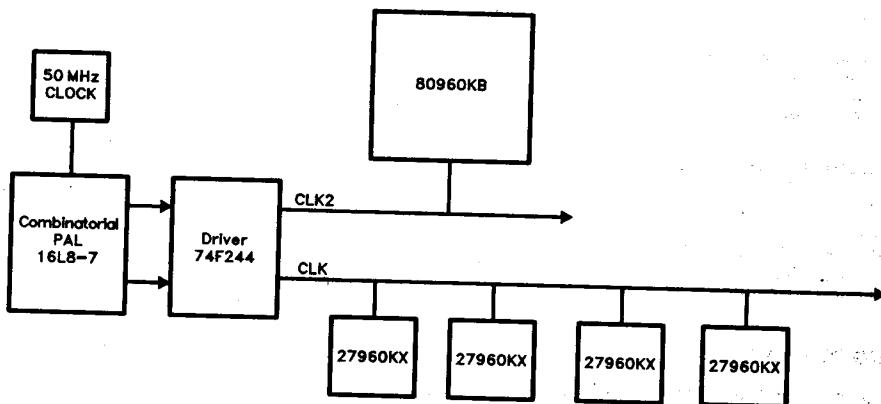
$$\begin{aligned} 27960K1-20 \text{ t}_{avc0h} &= 50 \text{ ns} - 20 \text{ ns} - 4 \text{ ns} \\ &= 26 \text{ ns} \end{aligned}$$

On timings such as this, where the EPROM is faster than the microprocessor, we specified the EPROM's timing leaving the excess time as system guardband.

**NOTE:**

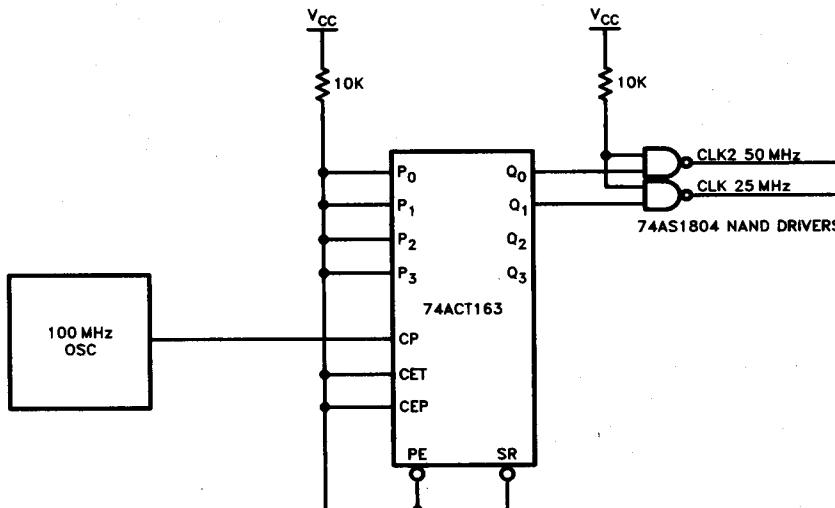
The 27960KX allows a positive clock skew (CLK2 leading CLK) of up to 4 ns and a negative clock skew (CLK2 lagging CLK) of up to 2 ns. The larger positive clock skew takes into account longer trace lengths and heavier loading on the 1x clock trace.

Figure 6A. Definition of Positive and Negative Clock Skew

**NOTE:**

CLK and CLK2 are generated by the same PAL. This minimizes skew between CLK and CLK2. Both PAL outputs are fed to a 74F244 driver. The EPROMs should be as close to the clock driver as possible.

Figure 6B. Example Clock Circuit with Minimum Skew



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NOTE:

This clock generation circuit uses a 100 MHz oscillator. The EPROMs should be as close to the NAND drivers as possible.

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Figure 6C. Example Clock Circuit Using a 100 MHz Oscillator

Decoders are needed for the systems address (chip select) decoding. For the 27960KX's timings we assumed a 5-10 ns chip select decoder for 16 MHz and 20 MHz frequencies and a 5-9 ns decoder for 25 MHz systems. The example below shows how the 27960K2-25 tsvch timing was derived.

@25 MHz the clock cycle is ~ 40 ns.

t_6 of the 80960KA/KB is 2-18 ns.

Decoder = 9 ns

4 ns clock skew guardband

$$27960K2-25 \text{ tsvch} = 40 \text{ ns} - 18 \text{ ns} - 9 \text{ ns} - 4 \text{ ns} = 9 \text{ ns}$$

The list below shows the buffers used in generating these timings:

	Input Buffer	Output Buffer
20 MHz	9 ns	5 ns
16 MHz	10 ns	7 ns

The 20 MHz buffers are slightly faster in keeping with the increased sensitivity for higher performance. We chose the above buffers because of their wide availability. Significantly faster buffers are available for applications requiring them. The example below shows tchqv for the 27960K2-20.

@20 MHz the clock cycle is ~ 50 ns.

t_{10} of the 80960KA/KB is 3 ns.

Output buffer for 20 MHz = 5 ns.

4 ns clock skew guardband

$$27960K2-20 \text{ tchqv} = 50 \text{ ns} - 5 \text{ ns} - 3 \text{ ns} - 4 \text{ ns} = 38 \text{ ns}$$

SYSTEM BUFFERING CONSIDERATIONS

For many large system applications buffering may be required between the microprocessor and memory devices. The 20 MHz - 2 WS and 16 MHz 27960KX AC timings take this into account. For applications at these frequencies not requiring buffering these devices will provide an additional 5-10 ns of system guardband.

ABSOLUTE MAXIMUM RATINGS*

Read Operating Temperature 0°C to + 70°C(8)
 Case Temperature under Bias -10°C to + 80°C(8)
 Storage Temperature -65°C to + 125°C
 All Input or Output Voltages -0.6V to + 6.5V(4)
 with Respect to Ground
 Voltage on A₉ -0.6V to + 13.0V(4)
 with Respect to Ground
 V_{PP} Supply Voltage -0.6V to + 14.0V(4)
 with Respect to Ground
 V_{CC} Supply Voltage -0.6V to + 7.0V(4)
 with Respect to Ground

NOTICE: This data sheet contains preliminary information on new products in production. The specifications are subject to change without notice. Verify with your local Intel Sales office that you have the latest data sheet before finalizing a design.

*WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.

DC CHARACTERISTICS: READ OPERATION

0°C < T_A < + 70°C, V_{CC} = 5V ± 10%, TTL Inputs

Symbol	Parameter		Notes	Min	Max	Unit	Test Condition
I _{LI}	Input Load Current				1	µA	V _{IN} = 5.5V
I _{LO}	Output Leakage Current				10	µA	V _{OUT} = 5.5V
I _{PP}	V _{PP} Load Current Read				10	µA	V _{PP} = 0 to V _{CC} , PGM = V _{IH}
I _{SB}	V _{CC} Standby	Switching	2		45	mA	CS = V _{IH} , f = 25 MHz
		Stable	2		30	mA	CS = V _{IH}
I _{CC}	V _{CC} Active Current		1, 3, 7		125	mA	CS = V _{IL} , f = 25 MHz, I _{OUT} = 0 mA
V _{IL}	Input Low Voltage		4	-0.5	0.8	V	
V _{IH}	Input High Voltage			2.0	V _{CC} + 1	V	
V _{OL}	Output Low Voltage				0.45	V	I _{OL} = 2.1 mA
V _{OH}	Output High Voltage		5	V _{CC} - 0.8		V	I _{OH} = -100 µA
			5	2.4		V	I _{OH} = -400 µA
I _{OS}	Output Short Circuit		6		100	mA	

NOTES:

1. Maximum current is with outputs unloaded.
2. I_{CC} standby current assumes no output loading, i.e., I_{OH} = I_{OL} = 0 mA.
3. I_{CC} is the sum of current through V_{CC3} + V_{CC4} and does not include the current through V_{CC1} and V_{CC2}. (V_{CC1} and V_{CC2} supply power to the output drivers. V_{CC3} and V_{CC4} supply power to the rest of the device.)
4. Minimum DC voltage on input and output pins is -0.5V. During transitions, this level may undershoot to -2.0V for periods less than 20 ns.
5. Maximum DC voltage on input and output pins is V_{CC} + 0.5V which may overshoot to V_{CC} + 2.0V for periods less than 20 ns.
6. One output shorted for no more than one second. I_{OS} is sampled but not 100% tested.
7. I_{CC} max measured with a 10.11 µF capacitor between V_{CC} and V_{SS}.
8. This specification defines commercial product operating temperatures.

EXPLANATION OF AC SYMBOLS

The nomenclature used for timing parameters are as per IEEE STD 662-1980 IEEE Standard Terminology for Semiconductor Memory.

Each timing symbol has five characters. The first is always a "t" (for time). The second character represents a signal name, e.g., (CLK, ALE, etc.). The third character represents the signal's level (high or low) for the signal indicated by the second character. The fourth character represents a signal name at which a transition occurs marking the end of the time interval being specified.

The fifth character represents the signal level indicated for the fourth character. The list below shows character representations.

A:	Address	R:	Reset
B:	BLAST	Q:	Data
C:	Clock	S:	CS
H:	Logic High Level	t:	Time
L:	ALE/Logic Low Level	V:	Valid
P:	V _{PP} Programming Voltage	Z:	Tri-state level
X:	No longer a valid "driven" logic level		

AC CHARACTERISTICS: READ OPERATION $0^{\circ}\text{C} < T_A < +70^{\circ}\text{C}$, $V_{CC} = 5\text{V} \pm 10\%$

Versions				27960K2-25		27960K1-20		27960K2-20		27960K1-16		Unit
				25 MHz 2 Wait States		20 MHz 1 Wait State		20 MHz 2 Wait States		16 MHz 1 Wait State		
No	Symbol	Characteristic	Notes	Min	Max	Min	Max	Min	Max	Min	Max	
1	t_{AVC0H}	Address Valid to CLK High	CLK 0	12		18		10		15		ns
2	t_{AVLH}	Address Valid to ALE High		10		10		10		10		ns
3	t_{LLLH}	ALE Low to ALE High		12		12		12		12		ns
4	t_{LHAX}	ALE High to Address Invalid		8		8		8		8		ns
5	t_{SVCH}	CS Valid to CLK High	1, 5	5		8		7		8		ns
6	t_{CNHSX}	CLK High to CS Invalid	2	0		0		0		0		ns
7	t_{CHQV}	CLK High to Data Valid	7		33		43		38		45	ns
8	t_{CHQX}	CLK High to Data Invalid		7		7		7		7		ns
9	t_{CHQZ}	CLK High to Data High-Z	6		30		35		35		35	ns
10	t_{BVCH}	BLAST Valid to CLK High		15		15		15		15		ns
11	t_{CHBX}	CLK High to BLAST Invalid	3	5	35	5	45	5	45	5	45	ns

NOTES:

1. Valid signal level is meant to be either a logic high or logic low.
2. t_{CNHSX} —The subscript N represents the number of wait states for this parameter. CS can be de-asserted (high) after the number of wait states (N) has expired. The EPROM will continue to burst out data for the current cycle.
3. BLAST must be returned high before the next rising clock edge.
4. The sum of $t_{CHQV} + t_{AVCH} + NCLK$ will not equal actual t_{AVQV} if independent test conditions are used to obtain t_{AVCH} and t_{CHQV} (N = number of wait states).
5. CS must be deasserted after every burst read (see Figure 7).
6. Sampled, not 100% tested. The transition is measured ± 500 mV from steady state voltage.
7. For capacitive loads above 120 pF, t_{CHQV} can be derated by 1 ns/20 pF.

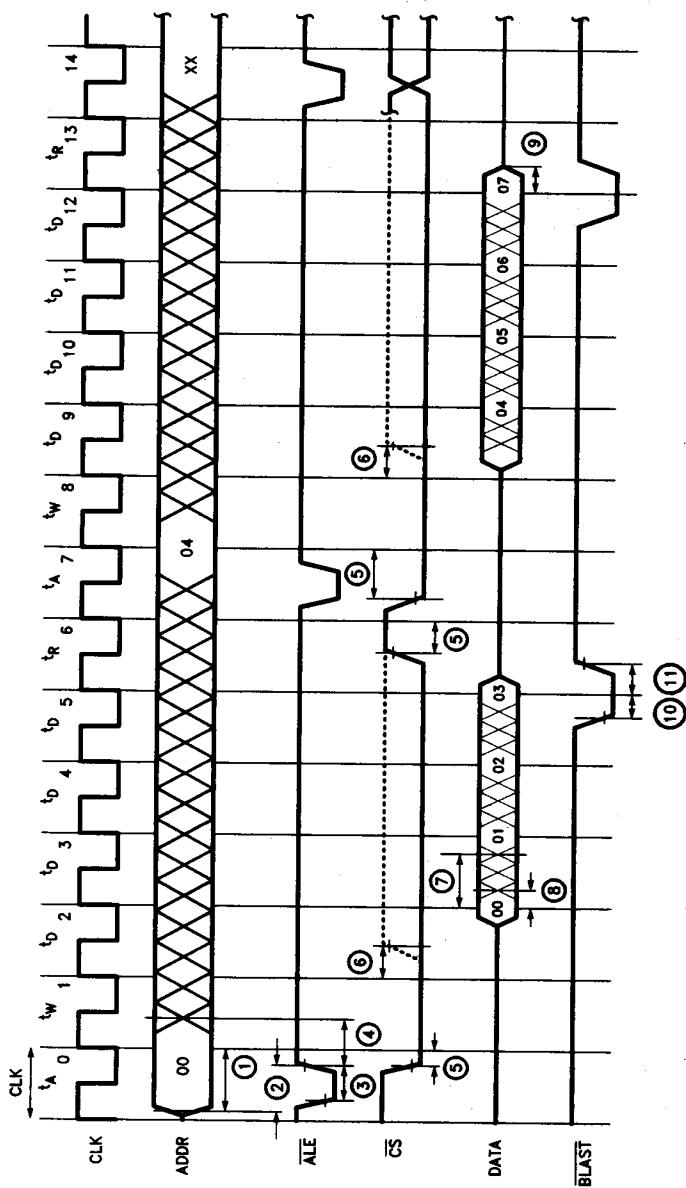


Figure 7. 27960KX 1 WS AC Read Waveforms

AC CONDITIONS OF TEST

Input Rise and Fall Times

(10% to 90%).....4 ns

Input Pulse Levels0.45V to 2.4V

Input Timing Reference Level1.5V

Output Timing Reference Level0.8V and 2.0V

Table 2. Mode Table

MODE	CS	PGM	BLAST	ALE	RESET	A ₉	V _{PP}	V _{CC}	OUTPUT
Read	V _{IL}	V _{IH}	V _{IH} ⁽¹⁾	V _{IH} ⁽²⁾	V _{IH}	X ⁽⁴⁾	V _{CC}	V _{CC}	D _{OUT}
Standby (6)	V _{IH}	X	X	X	V _{IH}	X	V _{CC} ⁽⁵⁾	V _{CC}	High Z
Program	V _{IL}	V _{IL}	V _{IH}	V _{IH} ⁽²⁾	V _{IH}	X	(3)	(3)	D _{IN}
Program Verify	V _{IL}	V _{IH}	V _{IH} ⁽¹⁾	V _{IH}	V _{IH}	X	(3)	(3)	D _{OUT}
Program Inhibit	V _{IH}	X	X	X	V _{IH}	X	(3)	(3)	High Z
ID Byte 0: Manufacturer	V _{IL}	V _{IH}	V _{IH} ⁽¹⁾	V _{IH} ⁽²⁾	V _{IH}	V _{ID} ⁽³⁾	V _{CC}	V _{CC}	89H
ID Byte 1: Part (27960)	V _{IL}	V _{IH}	V _{IH} ⁽¹⁾	V _{IH} ⁽²⁾	V _{IH}	V _{ID} ⁽³⁾	V _{CC}	V _{CC}	E0H
ID Byte 2: KX	V _{IL}	V _{IH}	V _{IH} ⁽¹⁾	V _{IH} ⁽²⁾	V _{IL}	V _{ID} ⁽³⁾	V _{CC}	V _{CC}	00B
ID Byte 3: 1 Wait-State 2 Wait-States	V _{IL}	V _{IH}	V _{IH} ⁽¹⁾	V _{IH} ⁽²⁾	V _{IL}	V _{ID} ⁽³⁾	V _{CC}	V _{CC}	01B 10B
Reset	X	X	X	X	V _{IL}	X	V _{CC}	V _{CC}	High Z

NOTES:

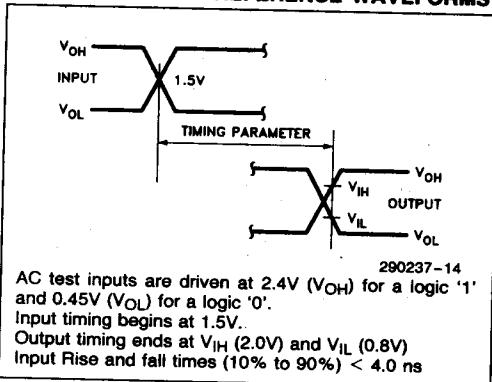
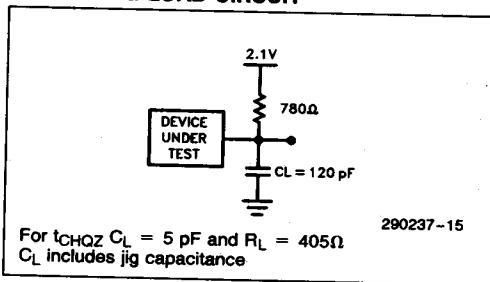
1. V_{IH} until data terminated at which time BLAST must go to V_{IL}.
2. Need to toggle from V_{IH} to V_{IL} to V_{IH} to latch address.
3. See DC Programming Characteristics for V_{CC}, V_{ID} and V_{PP} voltages.
4. X can be V_{IL} or V_{IH}.
5. V_{PP} = V_{CC} to meet standby current specification. V_{CC} > V_{PP} > V_{IL} will cause a slight increase in standby current.
6. The device must be in the idle state (by asserting RESET or using BLAST) before going into standby.

CAPACITANCE(1) $T_A = 25^\circ\text{C}$, $f = 1.0 \text{ MHz}$

Symbol	Parameter	Typ	Max	Unit	Condition
C_{IN}	Input Capacitance	4	6	pF	$V_{IN} = 0V$
C_{OUT}	Output Capacitance	12	15	pF	$V_{OUT} = 0V$
C_{VPP}	V_{PP} Capacitance	40	45	pF	$V_{IN} = 0V$

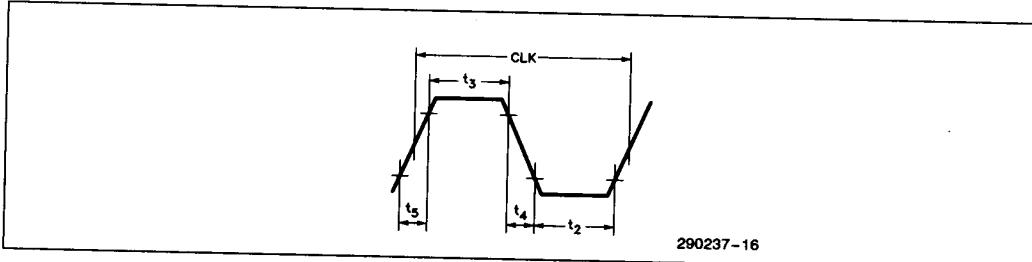
NOTE:

1. Sampled, not 100% tested

AC INPUT/OUTPUT REFERENCE WAVEFORMS**AC TESTING LOAD CIRCUIT****CLOCK CHARACTERISTICS**

Versions		25 MHz		20 MHz		16 MHz		Units
Symbol	Parameter	Min	Max	Min	Max	Min	Max	
CLK	Period	40		50		62.5		ns
T_5	Rise Time		10		10		10	ns
T_4	Fall Time		10		10		10	ns
T_2	Low Time	7		8		11		ns
T_3	High Time	7		8		11		ns

Max CLK Rise Time during Programming is 100 ns

CLOCK WAVEFORM

Program/Program Verify

Initially, and after each erasure, all bits of the EPROM are in the "1's" state. Data is introduced by selectively programming "0's" into the desired bit locations. Although only "0's" can be programmed, both "1's" and "0's" can be present in the data word. Ultraviolet erasure is the only way to change "0's" to "1's".

Program mode is entered when V_{PP} is raised to 12.75V. Program/Verify operation is synchronous with the clock and can only be initiated following an idle state. Program and Program Verify take place in 3 clock cycles. In the first clock cycle, addresses and data are input and programming occurs. Program Verify follows in the second clock cycle and the third clock cycle terminates synchronous Program/Verify operation, returning the state machine to the idle state with outputs at high impedance.

As in the Read mode, A_2 - A_{16} point to a four byte block in the memory array. During Programming the internal address increment circuitry is disabled and the programmer must supply A_0 and A_1 to point to an individual byte within the four byte block that is to be programmed. Only one byte is programmed in each 3 cycle program/Verify sequence.

Program Inhibit

Program Inhibit mode allows parallel programming and verification of multiple devices with different data. With V_{PP} at 12.75V, a Program/Verify sequence is initiated for any device that receives a valid ALE pulse and rising clock edge while \overline{CS} is asserted. A PGM pulse programs data in the first cycle of the sequence and data for Program Verify is output in the second cycle. The Program/Verify sequence is inhibited on any devices for which \overline{CS} is not asserted during the first (ALE) cycle. Data will not be programmed and the outputs will remain in their high impedance state.

intelligent Identifier™ Mode

The device's manufacturer, product type, and configuration are stored in a four byte block that can be

accessed by using the intelligent Identifier™ mode. The programmer can verify the device identifier and choose the programming algorithm that corresponds to the Intel 27960KX. The intelligent Identifier can also be used to verify that the product is configured with the desired Read mode options for wait states.

Intelligent Identifier mode is entered when A_9 (pin 32) is raised to its high voltage (V_H) level. The internal state machine is then set for intelligent Identifier Read operation. Reading the Identifier is similar to a Read operation on a one wait state configured product. Up to four bytes can be read in a single burst access. Intelligent Identifier read is terminated by a synchronous BLAST input, returning the state machine to the idle state with outputs at high impedance.

The four byte block code for the intelligent Identifier code is located at address 00H through 03H and is encoded as follows:

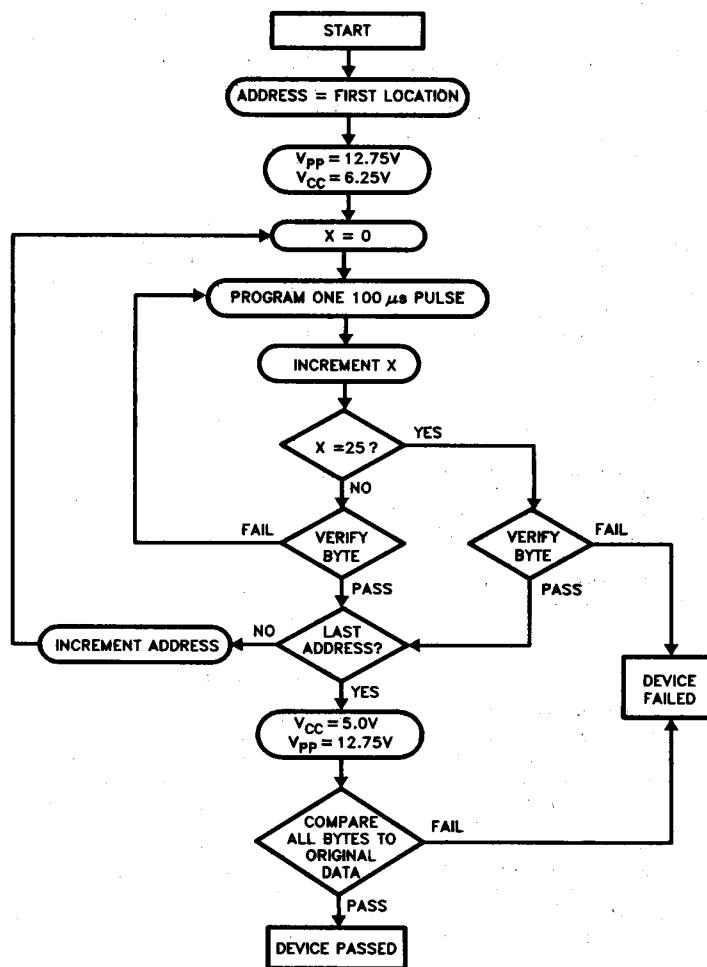
MEANING	(A_1, A_0)	DATA
Intel ID	Byte 00	89h
27960	Byte 01	E0h
KX	Byte 10	00b
1 wait state	Byte 11	01b
2 wait states	Byte 11	10b

4

RESET MODE

Due to the synchronous nature of the 27960KX, the various operating modes must be initiated from a known idle state. During normal operation, the internal state machine returns to an idle state at the termination of a bus access (after BLAST is asserted).

During initial device power up, the state machine is in an indeterminant state. The reset mode is provided to force operation in to the idle state. Reset mode is entered when the RESET pin is asserted. Output pins are asynchronously set to the high impedance state and address latches are put into the flow through mode. A reset is successfully completed and the state machine set in an idle state in the cycle after RESET has been asserted for a minimum of 10 clock cycles and deasserted for five clock cycles.



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Figure 8. Quick-Pulse Programming™ Algorithm

QUICK-PULSE PROGRAMMING ALGORITHM

The Quick-Pulse Programming algorithm programs Intel's 27960KX. Developed to substantially reduce programming throughput time, this algorithm allows optimized equipment to program a 27960KX in under 17 seconds. Actual programming time depends on the programmer used.

The Quick-Pulse Programming algorithm uses a 100 μ s pulse followed by a byte verification to determine when the addressed byte is correctly programmed. The algorithm terminates if 25 100 μ s

pulses fail to program a byte. Figure 8 shows the 27960KX Quick-Pulse Programming algorithm flowchart.

The entire program-pulse, byte-verify sequence is performed with $V_{CC} = 6.25V$ and $V_{PP} = 12.75V$. The programming equipment must establish V_{CC} before applying voltages to any other pins. When programming is complete, all bytes should be compared to the original data with $V_{CC} = 5.0V$ and $V_{PP} = 12.75V$.

D.C. PROGRAMMING CHARACTERISTICS $T_A = 25^\circ C \pm 5^\circ C$

Symbol	Parameter	Notes	Min	Max	Unit	Test Condition
I_{LI}	Input Load Current			10	μ A	$V_{IN} = V_{IH}$ or V_{IL}
I_{CC}	V_{CC} Program Current	1		125	mA	$CS = V_{IL}$
I_{PP}	V_{PP} Program Current	1		50	mA	$CS = V_{IL}$
V_{IL}	Input Low Voltage		-0.5	0.8	V	
V_{IH}	Input High Voltage		2.0	$V_{CC} + 0.5$	V	
V_{OL}	Output Low Voltage (Verify)			0.40	V	$I_{OL} = 2.1$ mA
V_{OH}	Output High Voltage (Verify)		$V_{CC} - 0.8$		V	$I_{OH} = -400$ μ A
V_{ID}	A_9 intelligent Identifier Voltage		11.5	12.5	V	
V_{CC}	Supply Voltage (Program)	2	6.0	6.5	V	
V_{PP}	Program Voltage	2	12.5	13.0	V	

NOTES:

1. The maximum current value is with outputs unloaded.
2. V_{CC} must be applied simultaneously or before V_{PP} and remove simultaneously or after V_{PP} .
3. During programming clock levels are V_{IH} and V_{IL} .

AC PROGRAMMING, RESET AND ID CHARACTERISTICS $T_A = 25^\circ\text{C} \pm 5^\circ\text{C}$

No	Symbol	Parameter	Notes	Min	Max	Units
1	t_{AVPL}	Address Valid to $\overline{\text{PGM}}$ Low		2		μs
2	t_{CHAX}	CLK High to Address Invalid		50		ns
3	t_{LLCH}	$\overline{\text{ALE}}$ Low to CLK High	1	50		ns
4	t_{CHLH}	CLK High to $\overline{\text{ALE}}$ High	2	50		ns
5	t_{SVCH}	$\overline{\text{CS}}$ Valid to CLK High		50		ns
6	t_{CHSX}	CLK High to $\overline{\text{CS}}$ Invalid	3			ns
7	t_{CHQV}	CLK High to DOUT Valid			100	ns
8	t_{CHQX}	CLK High to DOUT Invalid		0		ns
9	t_{BVCH}	BLAST Valid to CLK High		50		ns
10	t_{CHBX}	CLK High to $\overline{\text{BLAST}}$ Invalid	4	50		ns
11	t_{QVPL}	DATA Valid to $\overline{\text{PGM}}$ Low		2		μs
12	t_{PLPH}	$\overline{\text{PGM}}$ Program Pulse Width		95	105	μs
13	t_{PHQX}	$\overline{\text{PGM}}$ High to DIN Invalid		2		μs
14	t_{CLPL}	CLK Low to $\overline{\text{PGM}}$ Low		50		ns
15	t_{QZCH}	DIN in Tri-State to CLK High		2		μs
16	t_{VCS}	V_{CC} Program Voltage to CLK High	7	2		μs
17	t_{VPS}	V_{PP} Program Voltage to CLK High	7	2		μs
18	t_{A9HCH}	A_9 V_{ID} Voltage to CLK High		2		μs
19	t_{CHA9X}	CLK High to A_9 not V_{ID} Voltage		2		μs
20	t_{RVCH}	$\overline{\text{RESET}}$ Valid to CLK High	6	50		ns
21	t_{CHCL}	CLK High to CLK Low	5	100		ns
22	t_{CLCH}	CLK Low to CLK High	5	100		ns

NOTES:

1. If $\overline{\text{CS}}$ is low, $\overline{\text{ALE}}$ can go low no sooner than the falling edge of the previous CLK.
2. $\overline{\text{ALE}}$ must return high prior to the next rising edge of clock.
3. $\overline{\text{CS}}$ must remain low until after the rising edge CLK1.
4. BLAST must return high prior to the next rising edge of CLK.
5. Max CLK rise/fall time is 100 ns.
6. $\overline{\text{RESET}}$ must be held low for 10 cycles and high for 5 cycles before performing a read.
7. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP} .

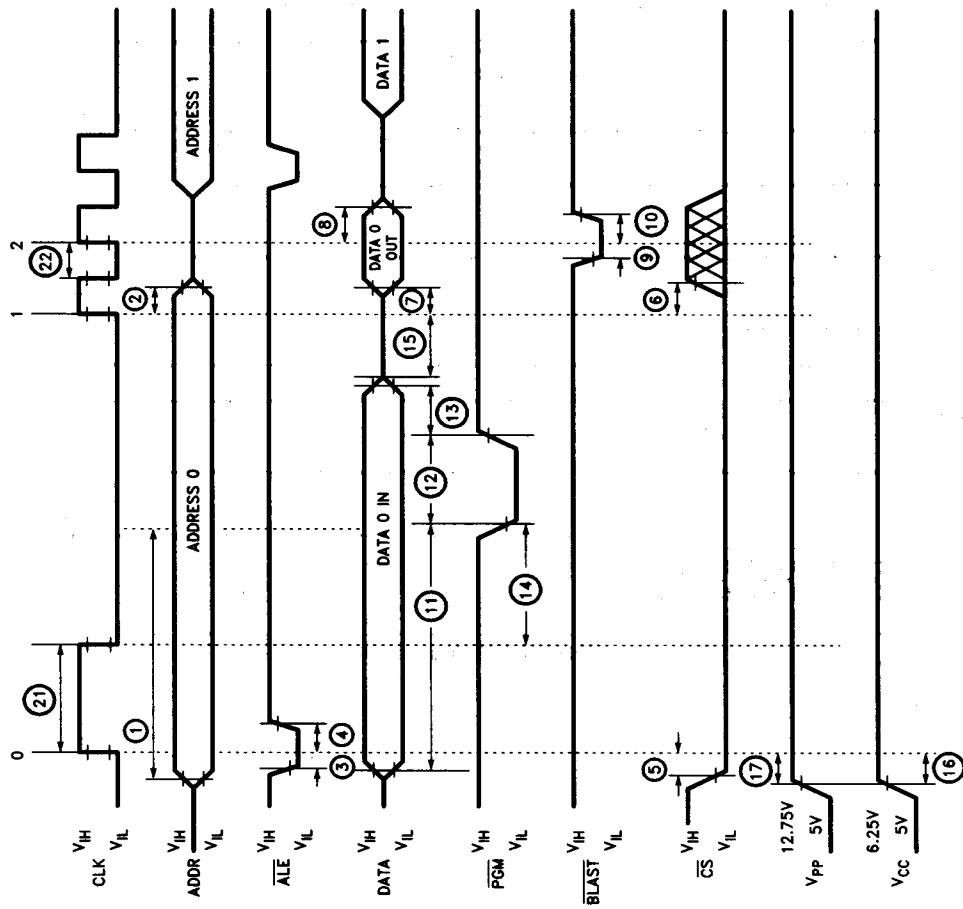


Figure 9. 27960KX Programming Waveforms

