SM530

Approved Product **Low EMI Spectrum Spread Clock**

FEATURES

- Reduces Systemic EMI.
- Modulates external source clock.
- 3 - 5 Volt power supply.
- 14 to 120 MHz.operating frequency range
- Output is multiplied or divided by 1, 2 or 4.
- Digitally controlled modulation.
- TTL/CMOS compatible outputs.
- Center and Down Spread modulation.
- Compliant with all major CISC, RISC and DSP processors.
- Low short term jitter.
- Synchronous output enable.
- Power down mode for low current operation
- Available in 20 pin SSOP and TSSOP packages.

APPLICATIONS

- Desktop/Laptop Computer
- Modems
- Scanners, Printers, Copiers, Fax Machines, MFP's
- Disk and CD-ROM Drives
- Automotive and EmbeddedSystems
- Networking, LAN/WAN
- Digital Cameras, Games
- LCD displays

BENEFITS

- Time to Market
- Lower cost of compliance
- Programmable EMI reduction
- No degradation in Rise/Fall times
- Lower component and PCB layer count

GENERAL DESCRIPTION

The IMI SM530 is a Spectrum Spread Clock Modulator designed for the purpose of reducing the Electro- Magnetic Interference (EMI) found in today's high speed digital systems. The SM530 is well suited for a wide range of digital system applications that require a reduction of radiated energy. This unwanted radiated energy is usually found in the odd harmonics of digital system clocks. By increasing the bandwidth of the digital clock, measured EMI at the fundamental and harmonic frequencies is greatly reduced. This reduction in radiated energy can significantly reduce the cost of complying with regulatory requirements and time to market, without degrading clock and timing signals.

The IMI SM530 is extremely versatile and flexible in that program control is available for each of the operating modes. Program control is provided for Input Frequency, Output Frequency Multiplication, Output Bandwidth, Center/Down Spread of Fout, Modulation ON/OFF and Fout state during Power Down Mode
Depending on the range of operation, the output clock, Fout, can be a multiple (1, 2, 4) or a fraction (1, 1/2, 1/4) of the input frequency. The SM530 can synchronously stop the modulated output at the low logic level. The power-down mode adds the flexibility of operating in a completely static mode for reduced standby current and simplified system board testing.

There are many benefits to using the SM530 Low EMI Clock Modulator. The most important benefit is reducing the amount of clock related EMI by as much as 12 - 18 dB., depending on the application. Refer to SM532 datasheet for the 16 pin SOIC version, which only supports Center-Spread operation.

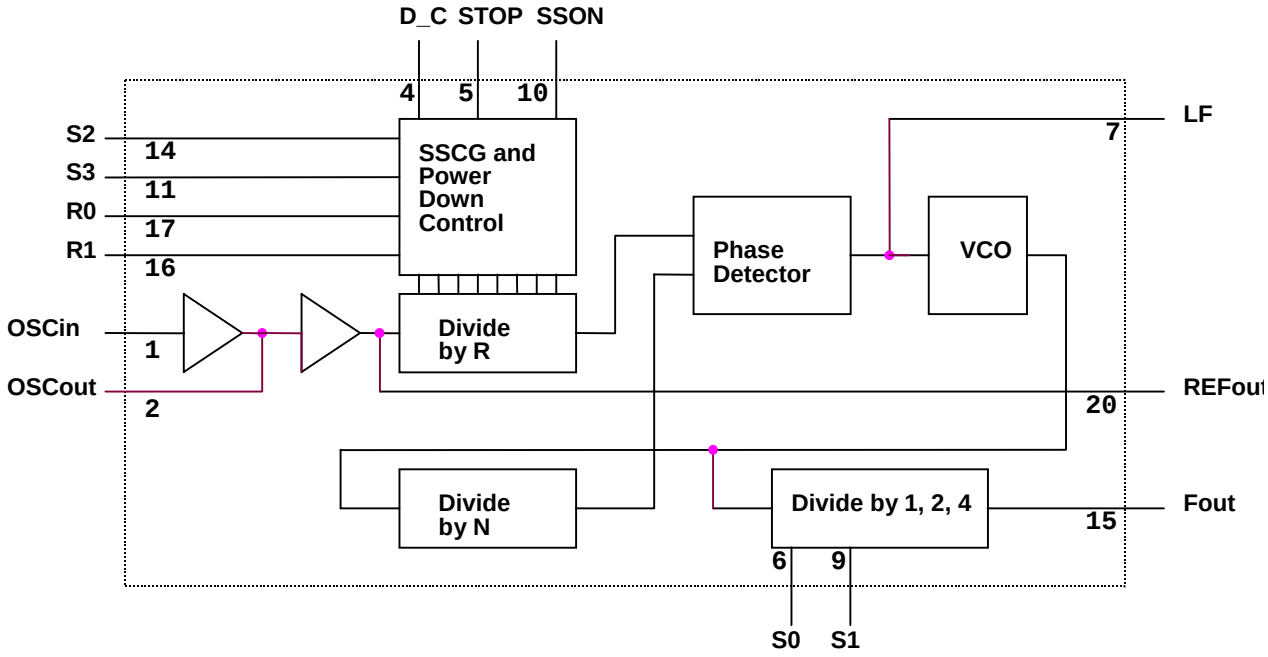


Figure 1. Block Diagram

ORDERING INFORMATION

Part No.	Package	Operating Temperature Range
IMISM530AYB	20 pin SSOP	0^0C to 70^0C
IMISM530ATB	20 pin TSSOP	0^0C to 70^0C

Marking Example: IMI
SM530AYB
Date Code, Lot#

IMISM530AYB

- Flow
  - B = Commercial
- Package
  - Y = SSOP
  - T = TSSOP
- Revisions
- IMI Device Number

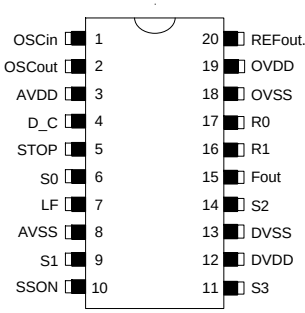


Figure 2. SM530, SSOP/TSSOP Package Pin Assignment

Pin Descriptions				
Pin No.	**Pin Name**	**I/O**	**TYPE**	**Description**
1,2	OSCin, OSCout	I/O	CMOS	Pins form an on-chip reference oscillator when connected to terminals of an external parallel resonant crystal. OSCin may be connected to a TTL/CMOS external clock source. AC coupling may be required. If OSCin is connected to an external clock other than crystal, leave OSCout (pin 2) unconnected. The input frequency range is 14 to 120 Mhz @ 5.0 VDC
3	AVDD	Power	Power	Analog circuit positive power supply.
4	D_C	I	TTL	Input selection pin used to determine the center frequency position of modulated Fout (pin 15). Pin 4 has internal pull-down resistor. D_C = 0: Down Spread. D_C = 1: Center Spread.
5	STOP	I	TTL	When = 1, synchronously stops Fout clock at a logic low state. Pin 5 has internal pull-down resistor.
6,9	S0, S1	I	TTL	Input control used to select the frequency multiplication at Fout, relative to the reference clock. See table on page 5. S0 has internal pull-down, S1 has internal pull-up.
7	LF	O	Analog	Single ended tri-state output of the phase detector. A two pole passive loop filter is connected to LF. See table on page 7 for proper values.
8	AVSS	Ground	Ground	Analog circuit ground.
10	SSON	I	TTL	Input control pin used to enable modulation at the Fout pin. SSON = 0 = Modulation ON, SSON = 1 = Modulation OFF. Has internal pull-down.
11, 14	S3, S2	I	TTL	Input control pins, set the amount of modulation at Fout. See table on page 6 for settings. S2 has internal pull-up, S3 has internal pull-down.
12	DVDD	Power	Power	Digital positive power supply. Should be kept separate from analog power for best performance.
13	DVSS	Ground	Ground	Digital circuit ground.
15	Fout	O	TTL	Modulated clock output.
16, 17	R1, R0	I	TTL	Input pins control the input frequency range as described in table on page 5. R0 and R1 have internal pull-up.
18	OVSS	Ground	Ground	Oscillator circuit ground. Can be common to DVSS.
19	OVDD	Power	Power	Oscillator circuit positive power supply. Can be common to DVDD.
20	REFout	O	TTL	Buffered output of the crystal or external clock input. (Unmodulated)

Table 1.

ABSOLUTE MAXIMUM RATINGS

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, precautions should be taken to avoid application of any voltage higher than the absolute maximum rated voltages to this circuit. For proper operation, Vin and Vout should be constrained to the range, VSS < (Vin or Vout) < VDD. All digital inputs are tied high or low internally. Refers to electrical specifications for operating supply range.

Item	*Symbol*	*Min.*	*Max.*	*Units*
Supply Voltage	VDD	0	6.0	VDC
Input, relative to VSS	VIRvss	-0.3	VDD +0.3	VDC
Output, relative to VSS	VORvss	-0.3	VDD +0.3	VDC
AVDD relative to DVDD	ΔVpp	-100	+100	mv
AVSS relative to DVSS	ΔVss	-100	+100	mv
Temperature, Operating	TOP	0	+ 70	^{0} C
Temperature, Storage	TST	- 65	+ 150	^{0} C

Table 2.

Electrical Characteristics					
Characteristic	***Symbol***	***Min.***	***Typ.***	***Max.***	***Units***
Input Low Voltage	VIL	-	-	0.8	Vdc
Input High Voltage	VIH	2.0	-	-	Vdc
Input Low Current	IIL	-	-	100	μA
Input High Current	IIH	-	-	100	μA
Output Low Voltage IOL= 8mA, VDD = 5V	VOL	-	-	0.4	Vdc
Output High Voltage IOH = 8mA, VDD = 5V	VOH	VDD-1.0	-	-	Vdc
Output Low Voltage IOL= 5mA, VDD = 3.3V	VOL	-	-	0.4	Vdc
Output High Voltage IOH = 3mA,VDD = 3.3V	VOH	2.4	-	-	Vdc
Input Capacitance (Pin-1)	C_{in1}	-	3	-	pf
Output Capacitance (Pin-2)	C_{in2}	-	5	-	pf
Pull-Up Resistor values (pins 9, 14, 16 and 17)	Rpu	100K	167K	300K	Ohms
Pull-Down resistor values (pins 4, 5, 6, 10, 11)	Rpd	150K	250K	350K	Ohms
Tri-State Leakage Current (pins 7, 15 and 20)	IOZ	-	5.0	-	μA
Static Supply Current (Power Down mode)	IDD	-	-	250	μA
5 Volt Dynamic Supply Current (Operating mode)	ICC	-	25	30	ma
3 Volt Dynamic Supply Current (Operating mode)	ICC	-	18	20	ma
Short Circuit Current (Fout)	ISC	-	-	30	ma
Test measurements performed at VDD = 3.3V +/-5% and 5V +/-10%, TA = 0°C to 70°C					

Table 3.

Timing Characteristics					
Characteristic	**Symbol**	**Min**	**Typ**	**Max**	**Units**
Output Rise Time Measured at 10% - 90% @ 5 VDC	tTLH	3.3	3.5	3.8	ns
Output Fall Time Measured at 10% - 90% @ 5 VDC	tTHL	2.1	2.3	2.5	ns
Output Rise Time Measured at 0.8V - 2.0V @ 5 VDC	tTLH	0.7	0.75	0.8	ns
Output Fall Time Measured at 0.8V - 2.0 V @ 5 VDC	tTHL	0.6	0.7	0.8	ns
Output Rise Time Measured at 10% - 90% @ 3.3 VDC	tTLH	4.8	5.0	5.4	ns
Output Fall Time Measured at 10% - 90% @ 3.3 VDC	tTHL	2.9	3.2	3.4	ns
Output Rise Time Measured at 0.8V - 2.0V @ 3.3 VDC	tTLH	1.6	1.75	1.9	ns
Output Fall Time Measured at 0.8V - 2.0 V @ 3.3 VDC	tTHL	1.1	1.3	1.5	ns
Output Duty Cycle	TsymF1	45	50	55	%
Peak-to Peak Jitter One Sigma (SSON = 1)	tj1s	-	250	500	ps
Measurements performed at VDD = 3.3V +/-5% and 5V +/-10%, TA = 0°C to 70°C, CL = 15pF, Fout = 50.0 MHz.					

Table 4.

FREQUENCY SELECTION TABLE

The following table provides the necessary information for setting the control lines for proper operation of the SM530 and for any frequency within its operating range. Note that the table includes operating frequencies at 3.3 and 5.0 VDC. The 3.3 VDC columns are lower in frequency than the 5.0 VDC operation due to the characteristics of the VCO.

VDD = 5 Volts +/- 10%					Multiplier Settings		Input Range Settings		VDD = 3.3 Volts +/- 5%				
Fin (Range) (MHz)		Fout/ Fin	Fout (Range) (MHz)						Fin (Range) (MHz)		Fout/ Fin	Fout (Range) (MHz)	
MIN	**MAX**	**X**	**MIN**	**MAX**	**S1**	**S0**	**R1**	**R0**	**MIN**	**MAX**	**X**	**MIN**	**MAX**
	See	Note			0	0	X	X		See	Note		
14	30	1	14	30	0	1	0	1	14	22.5	1	14	22.5
14	30	2	28	60	1	0	0	1	14	22.5	2	28	45
14	30	4	56	120	1	1	0	1	14	22.5	4	56	90
30	60	0.5	15	30	0	1	1	0	25	45	0.5	12.5	22.5
30	60	1	30	60	1	0	1	0	25	45	1	25	45
30	60	2	60	120	1	1	1	0	25	45	2	50	90
60	120	0.25	15	30	0	1	1	1	50	90	0.25	12.5	22.5
60	120	0.5	30	60	1	0	1	1	50	90	0.5	25	45
60	120	1	60	120	1	1	1	1	50	90	1	50	90

Note: Selects Power Down state, see table 7 below. X = don't care condition.

Table 5. Frequency Selection Table

MODULATION AND POWER DOWN SELECTIONS

The bandwidth of the modulation applied to Fout is controlled by two input control lines, S2 and S3. Also, S2 and S3 control the state the SM530 will go to when the Power Down mode is selected. The Power Down mode is selected when both S0 and S1 are set to a logic state 0. Refer to the tables below for the proper selection of Modulation Bandwidth and Power Down state.

Modulation Selection Table						
	Modulation Settings\		D_C = 0 Down Spread		D_C = 1 Center Spread	
Total Bandwidth	S3	S2	Low	High	Low	High
1.25 %	0	0	98.75 %	100 %	99.375 %	100.625 %
2.50 %	0	1	97.50 %	100 %	98.75 %	101.25 %
5.00 %	1	0	95.00 %	100 %	97.50 %	102.50 %
10.0 %	1	1	90.00 %	100 %	95.00 %	105.00 %

Table 6. Modulation Selection Table

Power Down Selection Table				
Fout State	S0	S1	S2	S3
Factory Test	0	0	0	1
Hi-Z	0	0	1	1
0	0	0	0	0
1	0	0	1	0

Table 7. Power Down Selection Table

Note:

The STOP and POWER DOWN functions are two separate operations. Selecting STOP does not place the SM530 in the power down mode. POWER DOWN is selected by setting S0 = 0 and S1 = 0.

Loop Filters

The SM530 requires an external loop filter to provide the proper operation and modulation profile for a given input frequency. The loop filter is connected to pin 7 (LF) of the SM530 and is a typical 2 pole low pass filter. Since the SM530 operates over such a wide range of frequencies, the loop filter will change depending on the frequency of operation. The following loop filter values are recommended for best performance and modulation profile at 3.0 volts and 5.0 volts VDD. Operating voltage is measured at the VDD pin of the SM530.

Notice that the selection of Loop Filter values only depends on the input frequency and VDD voltage, and does not depend on the R and S settings.

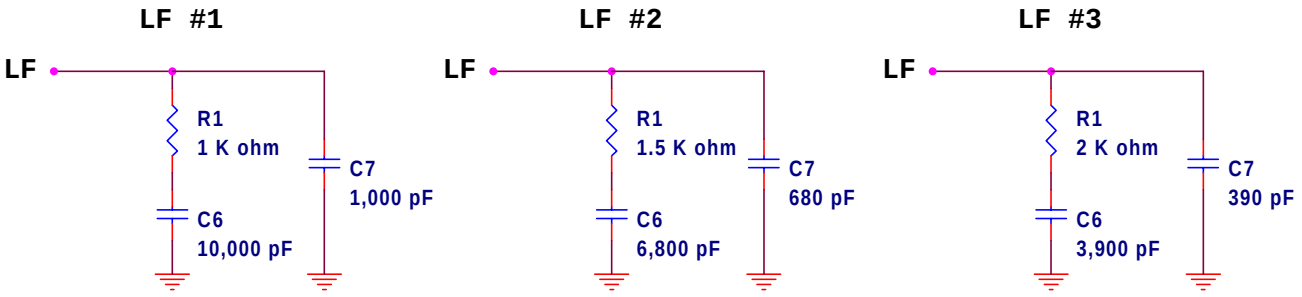


Figure 3. Recommended Loop Filter

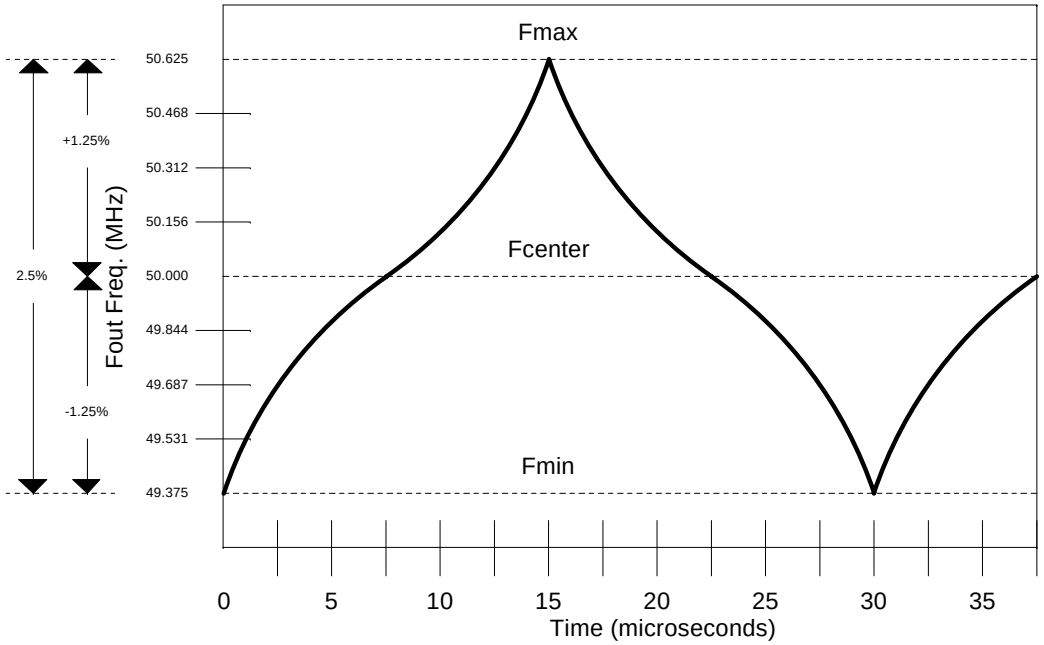
Recommended Loop Filter Values						
Input Range	**VDD +/-5%**	**Input Frequency Range (MHz)**	**R1 (KΩ)**	**C6 (pF)**	**C7 (pF)**	**Loop Filter #**
Low	3.3	14.0 to 22.5	1.0	10,000	1,000	1
Middle	3.3	25.0 to 45.0	1.0	10,000	1,000	1
High	3.3	50.0 to 90.0	1.0	10,000	1,000	1
Input Range	**VDD +/-10%**	**Input Frequency Range (MHz)**	**R1 (KΩ)**	**C6 (pF)**	**C7 (pF)**	**Loop Filter #**
Low	5.0	14.0 to 19.9	1.0	10,000	1,000	1
Low	5.0	20.0 to 24.9	1.5	6,800	680	2
Low	5.0	25.0 to 29.9	2.0	3,900	390	3
Middle	5.0	30.0 to 39.9	1.0	10,000	1,000	1
Middle	5.0	40.0 to 49.9	1.5	6,800	680	2
Middle	5.0	50.0 to 59.9	2.0	3,900	390	3
High	5.0	60.0 to 79.9	1.0	10,000	1,000	1
High	5.0	80.0 to 99.9	1.5	6,800	680	2
High	5.0	100.0 to 120.0	2.0	3,900	390	3

Table 8.

The component values listed in Table 8 are recommended values using commonly manufactured components. Note that there are actually 3 different sets of loop filter values. Due to the VCO characteristics, the table is divided in to 3 volt operation and 5 volt operation. Referring to the table above, it is apparent that one set of loop filter values is all that is needed in the 3 volt operation. In the 5 volt operation, each input operating range is divided into 3 sections which require a different loop filter for optimal performance. The best loop filter for any application is the one that, provides the required EMI reduction, maintains system integrity, has a modulation profile shown on page 8 and uses commonly available components.

SSCG Modulation Profile

The modulation rate of the SM530 within any range is typically 20 - 40 kHz. With the correct loop filter connected to pin 7, the following profile will provide the best EMI reduction. This profile can be seen on a Time Domain



Analyzer.

Figure 4. Modulation Profile

THEORY OF OPERATION

The SM530 is a Phase Lock Loop (PLL) type clock generator using Direct Digital Synthesis (DDS). By precisely controlling the bandwidth of the output clock, the SM530 becomes a Low EMI clock generator. The theory and detailed operation of the SM530 will be discussed in the following sections.

EMI

All digital clocks generate unwanted energy in their harmonics. Conventional digital clocks are square waves with a duty cycle that is very close to 50 %. Because of the 50/50 duty cycle, digital clocks generate most of their harmonic energy in the odd harmonics, i.e.; 3^{rd}, 5^{th}, 7^{th} etc. It is possible to reduce the amount of energy contained in the fundamental and harmonics by increasing the bandwidth of the fundamental clock frequency. Conventional digital clocks have a very high Q factor, which means that all of the energy at that frequency is concentrated in a very narrow bandwidth, consequently, higher energy peaks. Regulatory agencies test electronic equipment by the amount of peak energy radiated from the equipment. By reducing the peak energy at the fundamental and harmonic frequencies, the equipment under test is able to satisfy agency requirements for Electro-Magnetic Interference (EMI). Conventional methods of reducing EMI have been to use shielding, filtering, multi-layer PCB's etc. The SM530 uses the approach of reducing the peak energy in the clock by increasing the clock bandwidth, and lowering the Q.

SSCG

SSCG uses a patented technology of modulating the clock over a very narrow bandwidth and controlled rate of change, both peak and cycle to cycle. The SM530 takes a narrow band digital reference clock in the range of 14 - 120 MHz and produces a clock that sweeps between a controlled start and stop frequency and precise rate of change. The bandwidth of the output clock is programmable. Using two control lines on the SM530, the bandwidth of the modulated clock can be controlled over four descrete settings, 1.25, 2.50, 5.0 and 10%. To understand what happens to an SSCG clock, consider that we have a 50 MHz clock with a 50 % duty cycle. From a 50 MHz clock we know the following;

Clock Frequency = Fc = 50 MHz.
Clock Period = Tc = 1/50 MHz = 20 ns.

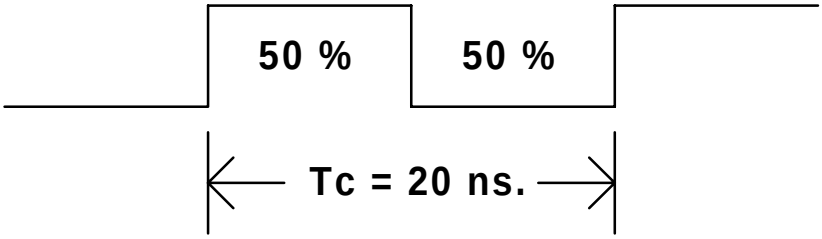


Figure 5. Unmodulated Clock

Consider that this 50 MHz clock is applied to the OSCin input of the SM530, either as an externally driven clock or as the result of a parallel resonant crystal connected to pins 1 and 2 of the SM530. Also consider that the SM530 is programmed for the following operation;

Range (R0, R1) =	0, 1	Mid Range
Multiplier (S0, S1) =	0, 1	X1
D_C =	1	Center Spread
SSON =	1	Modulation is OFF
% Modulation (S2, S3) =	1, 0	2.50 % Spread

From the above parameters, the output clock at Fout will be 50.625 MHz. With modulation turned off, the frequency of Fout will always rest at the high end of the programmed spectrum. In this case, +1.25 % of 50 MHz is .625 MHz, equals 50.625 MHz.

When modulation is turned ON, the clock at Fout begins sweeping downward to the minimum extreme of -1.25 % of 50 MHz which is 50 MHz - .625 MHz = 49.375 MHz. When the clock reaches 49.375, the SM530 begins sweeping back up to the maximum extreme of 50.625 MHz. If we were to look at this clock on a spectrum analyzer we would see the following picture. Keep in mind that this is a drawing of a perfect clock with no noise.

We see that the original 50 MHz reference clock is at the center Frequency, Cf, and the minimum and maximum extremes are positioned symmetrically about the center frequency. This type of modulation is called **Center-Spread**. Diagram 6 illustrates this as it is seen on a spectrum analyzer. Note that when modulation is turned off, the Fout clock is at the maximum extreme of the bandwidth.

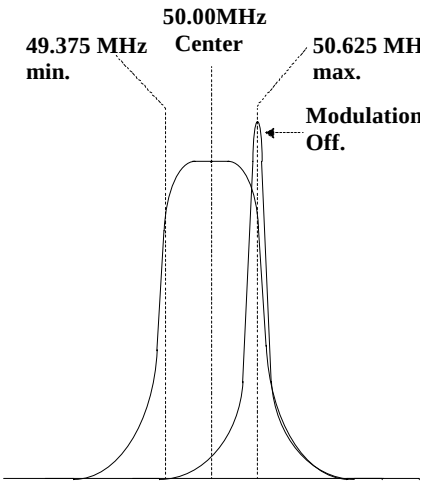


Figure 6.

Diagram 7 below shows our 50 MHz clock as it would be seen on an oscilloscope. The top trace is the non-modulated reference clock, or the REFout clock at pin 20. The bottom trace is the modulated clock at pin 15. From this comparison chart you can see that the frequency is decreasing and the period of each successive clock is increasing. The Tc measurements on the left and right of the bottom trace indicate the period of the clock as it moves from the center frequency at 50 Mhz and the minimum frequency at 49.375 MHz. extremes of the clock. Intermediate clock changes are small and accumulate to achieve the total period deviation. The reverse of this diagram would show the clock period gettting smaller as the frequency increases.

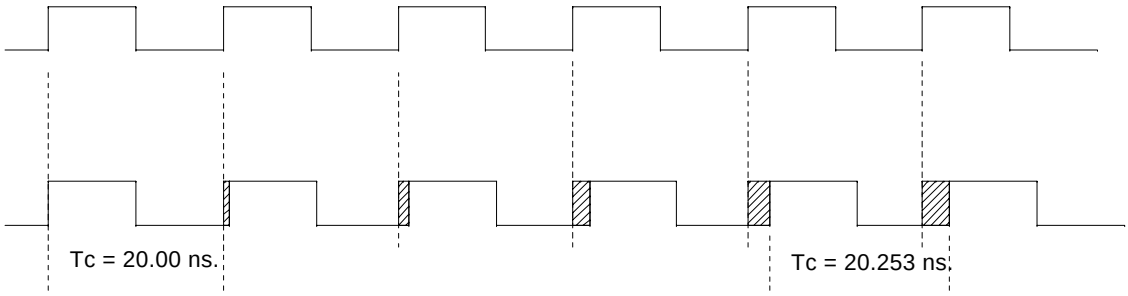


Figure 7. Period Comparison Chart

There are certain cases where center spread modulation is not applicable. If the maximum design frequency of the intended application is 50 MHz and becomes unstable above 50 MHz, then increasing the clock to 50.625 MHz might cause unwanted system problems.

To accommodate this situation, the SM530 has an operating mode where the maximum Fout frequency never exceeds the reference frequency, not including any multiplier that might be applied. This type of modulation is called **Down Spread**. The effective center frequency of the Fout clock is shifted down by one-half the amount of the applied modulation.

If the amount of clock spread is set for 2.50%, the effective center frequency of Fout is now 1.25 % less than 50 MHz or 49.375 MHz, when modulation is turned on. When modulation is turned off, the Fout frequency will go to 50.0 MHz, since this is the maximum extreme of the applied modulation settings. The one drawback to down spread modulation is that the effective center frequency of the clock is, in this case, 1.25 % slower, which means that the performance of the system may be 1.25 % slower.

Using the above operating parameters for the SM530 and selecting Down Spread, the operating bandwidth will be as follows;

Range (R0, R1) =	0, 1	Mid Range
Multiplier (S0, S1) =	0, 1	X1
D_C =	0	Down Spread
SSON =	0	Modulation is ON
% Modulation (S2, S3) =	1, 0	2.50 % Spread

To calculate the frequency extremes for these conditions in Down Spread mode, first determine the effective center frequency, Cf. In this case Cf is;

Cf = OSCin - (OSCin X % Spread)
Cf = 50 MHz - (50 MHz X .0125)
Cf = 50 MHz - 0.625 MHz
Cf = 49.375 MHz

With the effective center frequency at 49.375 MHz, we can now determine the minimum and maximum extremes.

Fmax = Cf + (Cf X % Spread)
Fmax = 49.375 + (49.375 X .0125)
Fmax = 49.375 + .617
Fmax = 49.99 MHz

Fmin = Cf - (Cf X % Spread)
Fmin = 49.375 - (49.375 X .0125)
Fmin = 49.375 - .617
Fmin = 48.758 MHz

Another way of calculating the bandwidth in the Down Spread mode is to use the OSCin frequency as the starting point and multiplying the % Spread by 2. This assumes that the multiplier is 1. If the multiplier is 2, then you would use 2 times the OSCin in the formula.

Fmax = OSCin
Fmin = OSCin - (OSCin X (2 X % Spread))
Fmin = 50 MHz - (50 X (2 X .0125))
Fmin = 50 - 1.25
Fmin = 48.75 MHz

This is illustrated in the diagram to the right. You can see that the effective center frequency is 49.375 MHz and the min and max extremes are 1.25 % on either side of the center. Or using the second approach, the OSCin frequency is the max frequency and the min frequency is 2.5 % down from the reference.

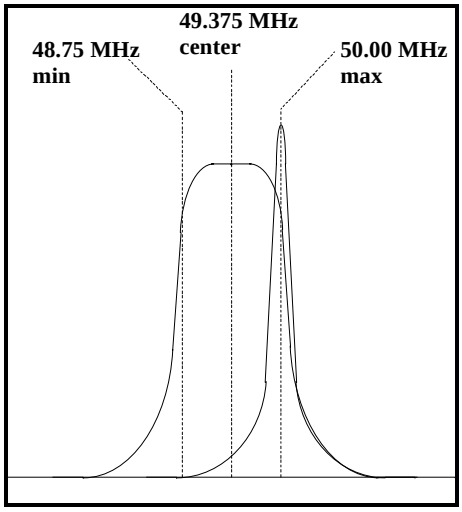


Figure 8.

Looking at diagram 8, you will note that the peak amplitude of the 50 MHz non-modulated clock is higher than the wideband modulated clock. This difference in peak amplitudes between modulated and unmodulated clocks is the reason why SSCG clocks are so effective in digital systems. This and the previous illustrations refer to the fundamental frequency of a clock. A very important characteristic of the SSCG clock is that the bandwidth of the harmonics is multiplied by the harmonic number. In other words, if the bandwidth of a 50 MHz clock is 1.35 MHz, the bandwidth of the 3rd harmonic will be 3 times 1.35, or 4.05 MHz. The amount of bandwidth is relative to the amount of peak energy in the clock. Consequently, the wider the bandwidth, the greater the energy reduction of the clock.

Most applications will not have a problem meeting agency specifications at the fundamental frequency. It is the higher harmonics that usually cause the most problems. With an SSCG clock, the bandwidth and peak energy reduction increases with the harmonic number. Consider that the 11th harmonic of our 50 MHz clock is 550 MHz. With a total spread of 1.35 MHz at 50 MHz, the spread at the 11th harmonic would be 14.85 MHz which greatly reduces the peak energy content. It is typical to see as much as 12 to 18 dB. of reduction at the higher harmonics, due to a modulated clock.

Referring to diagram 6 on page 10 and diagram 8 above, you can see that the peak amplitude of the non-modulated clock is much higher than the peak amplitude of the modulated clock. This is the reason the SM530 is used for EMI reduction. The amount of EMI reduction is dependent on the application. The difference in the peak energy of the modulated clock and the non-modulated clock in typical applications will see a 2 - 3 db. reduction at the fundamental and as much as 8 - 10 db. reduction at the intermediate harmonics, 3rd, 5th, 7th etc. At the higher harmonics, it is quite possible to reduce the peak harmonic energy, compared to the unmodulated clock, by as much as 12 to 18 db.

The dB reduction for a give frequency and spread can be calculated using a simple formula. This formula is only helpful in determining a relative dB reduction for a given application. This formula assumes an ideal clock with 50% duty cycle and therfore only predicts the EMI reduction of even harmonics. Other circumstances such as non-ideal clock and noise will affect the actual dB reduction. The formula is as follows;

dB = 6.5 + 9(Log10(F)) + 9(Log10(P))

Where; F = Frequency in Mhz, P = total % spread (2.5% = .025)

Using a 50 Mhz clock with a 2.5% spread, the theoretical dB reduction would be;

db @ 50 Mhz (Fund) = 6.5 + 15.29 - 14.42 = 7.37

dB @ 150 Mhz (3rd) = 6.5 + 19.58 - 14.42 = 11.66

dB @ 550 Mhz (11th) = 6.5 + 24.66 - 14.42 = 16.74

Modulation Profile

The SM530 moves from max. to min. frequencies of its bandwidth at a pre-determined rate and profile. The modulation frequency is determined by the input frequency and an internal divider. All 3 operating ranges modulate the Fout clock at from 20 to 40 kHz. The three operating ranges are 14 - 30 MHz, 30 - 60 MHz and 60 to 120 MHz. If OSCin = 15 MHz, the modulation rate is 20 kHz. If OSCin is 60 MHz, in mid-range, the modulation rate would be 40 kHz. To provide the proper modulation rate the input reference frequency is divided by a fixed number in each range. The input reference frequency is divided by 750 in Low Range, 1500 in Mid Range and 3000 in the High Range. From these numbers, the modulation rate can be determined for any input frequency.

Example:

OSCin = 45.378 MHz, Input Range = Mid, Input divisor = 1500

Fmod = OSCin /1500

Fmod = 30.252 kHz

If you have a clock frequency that was on the boundary of the Mid-range and the High range of operation, the choice of selecting which range to use would be determined by which modulation rate is desired. If you choose the Mid-range, the modulation rate would be 40 kHz, while choosing the High range would yield a 20 kHz modulation rate. There is some operational overlap between ranges, such that 58 MHz in the Mid-Range would give the same results as 58 MHz in the High-Range, except for the modulation rate. This type of operation is not recommended unless it is thoroughly tested.

The modulation profile of the SM530 is not a linear sweep from max to min and back. The OSCin reference clock determines the modulation frequency but the internal SSCG control logic determines the actual modulation profile. The modulation profile can best be described by comparing the instantaneous frequency at Fout with time. The illustration in diagram 9 below is a representation of the modulation profile of the SM530 as displayed on a Time Domain Analyzer.

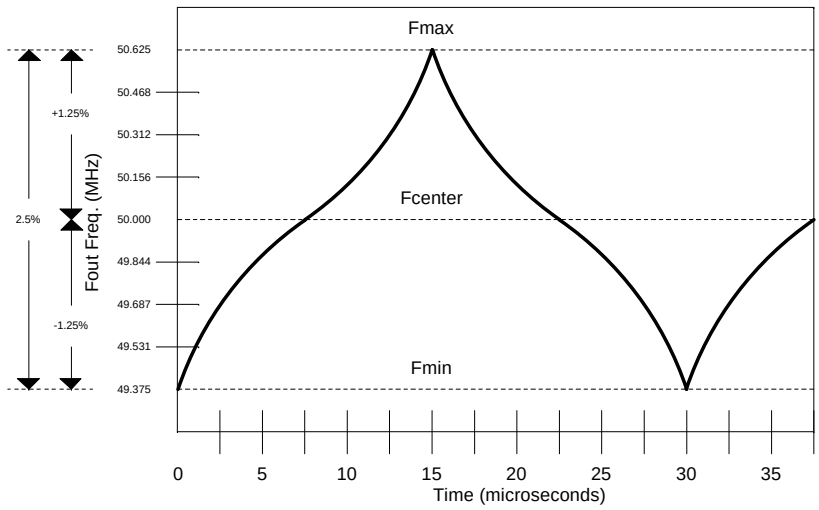


Figure 9. Frequency Profile in Time Domain

As can be seen from the diagram above, the Fout/Time profile progresses through frequencies depending on where it is in the sweep. If the frequency is in the middle of the sweep, the rate of change is slower compared to the rate at the extremes of the band. When the frequency is nearing the end of the band, it is moving through these frequencies faster, since it has to sweep through these same frequencies again after reversing direction. This modulation profile is one of the key elements to the SM530. Using a linear sweep through all frequencies would not give as good of results in EMI reduction.

APPLICATION NOTES AND SCHEMATICS

The schematic diagram shown below is a simple minimum component application example of an SM530 design. In the case shown below, the control lines are configured for the following parameters;

Input Frequency: Mid-Range Multiplier: X1 Modulation: 2.50 % SSON: On

Refer to loop filter values on Table 8, page 7, for operation at 3.3 Volts DC.

* L1 and C9 are required when Y1 is a 3rd. overtone crystal.

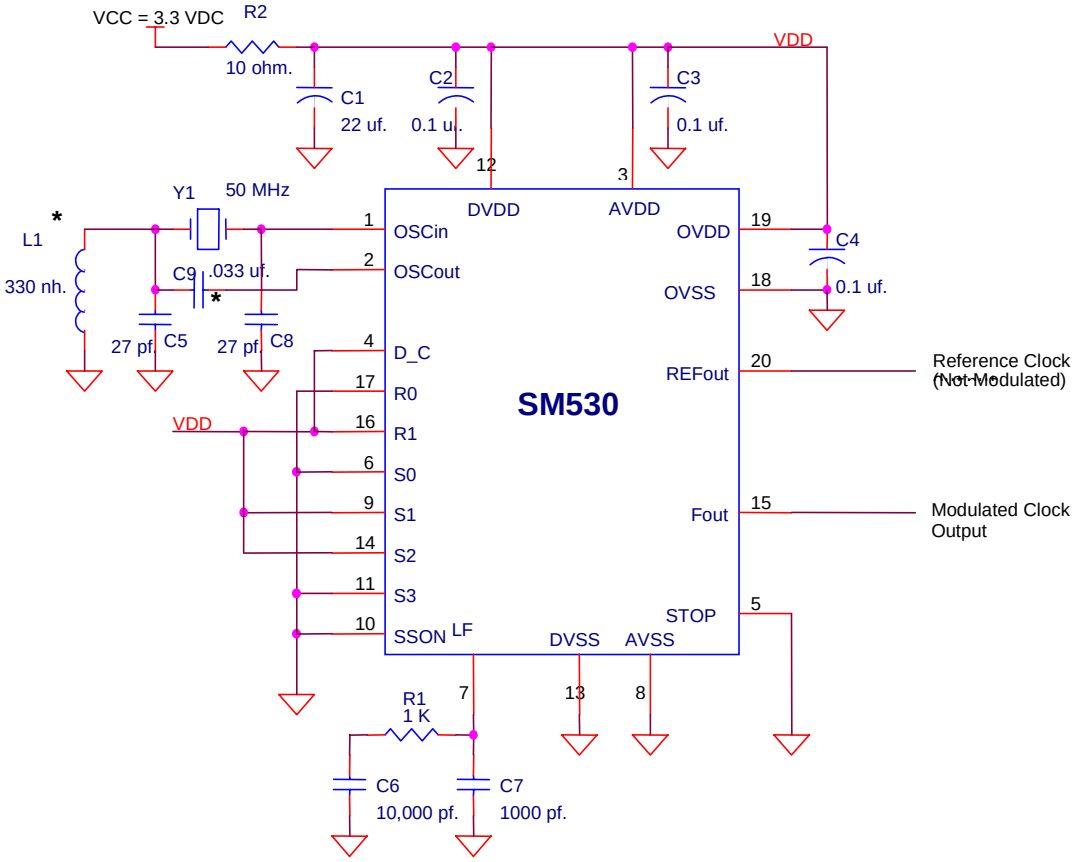


Figure 10. Application Schematic

The SM530 has an internal Analog Power and Ground and a Digital Power and Ground. In the example above, the digital and analog circuits are connected together. If noise is a concern, it is recommended that the Analog and Digital Power and Grounds be separated. The loop filter shown above is recommended for operation at 3.14 - 3.47 VDC. This filter can also be used in 5.0 VDC operations when operating in the low frequency end of each of the three input frequency ranges. Refer to table 8 on page 7 for loop filter information. Also note, the crystal, Y1, is a third overtone 50 Mhz crystal, which requires an inductor and decoupling capacitor to OSCout.

Diagram 11 below shows the equivalent internal oscillator circuit for the SM530.

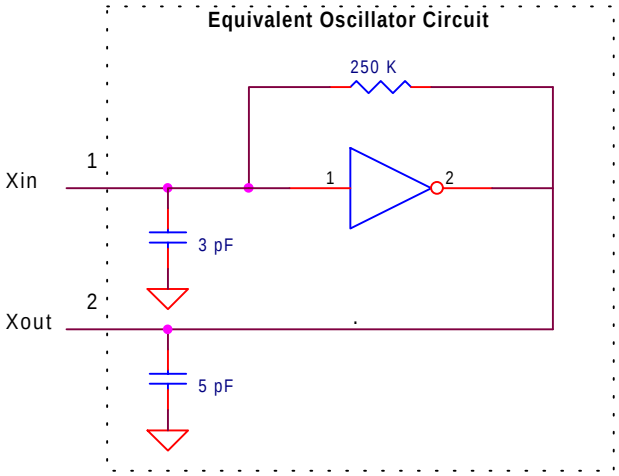


Figure 11. Equivalent Oscillator Circuit.

PCB Layout Example

The SM530 Spectrum Spread Clock is a PLL type hybrid circuit. This means that is contains both digital and analog circuits on the same die. The Phase Detector, Loop Filter and VCO are analog circuits that must operate in a very low noise environment for best performance. There are several ways to keep this noise to a minimum, such as bypass capacitors on all power pins and separating the analog and digital power and ground planes. The diagram below uses the first approach of placing bypass capacitors as close to every power pin as possible. In addition, all ground pins should be connected directly to the ground plane with little or no trace length. Note also that only the power and ground circuits of the SM530 have been shown. Other circuits such as the Loop Filter components must be located as close to the Loop Filter pin as possible, for best performance.

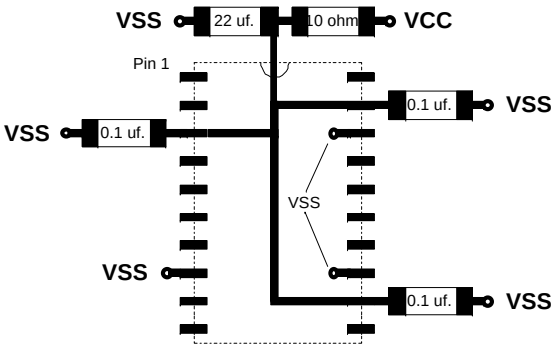
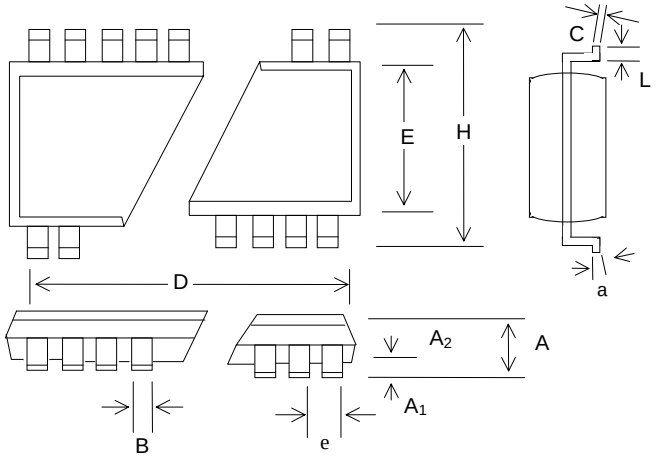
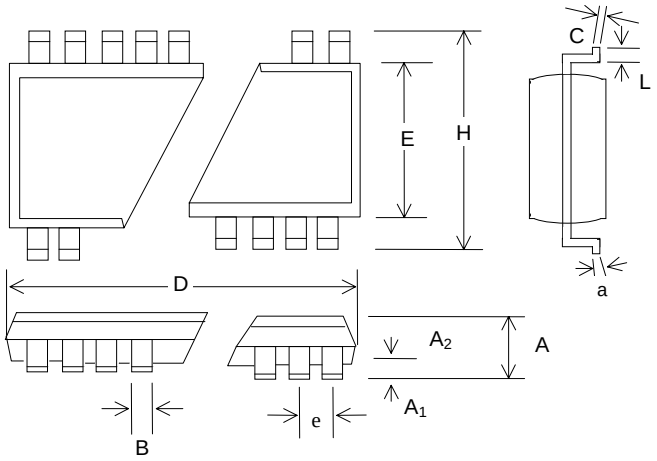


Figure 12. SM530 Single Power Plane PCB Layout

PACKAGE DIMENSIONS AND DRAWINGS



20 PIN SSOP OUTLINE DIMENSIONS						
	INCHES			MILLIMETERS		
SYMBOL	MIN	NOM	MAX	MIN	NOM	MAX
A	0.068	0.073	0.078	1.73	1.86	1.99
A_1	0.002	0.005	0.008	0.05	0.13	0.21
A_2	0.066	0.068	0.070	1.68	1.73	1.78
B	0.010	0.012	0.015	0.25	0.30	0.38
C	0.005	0.006	0.009	0.13	0.15	0.22
D	0.278	0.284	0.289	7.07	7.20	7.33
E	0.205	0.209	0.212	5.20	5.30	5.38
e	0.0256 BSC			0.65 BSC		
H	0.301	0.307	0.311	7.65	7.80	7.90
a	0°	4°	8°	0°	4°	8°
L	0.022	0.030	0.037	0.55	0.75	0.95



20 PIN TSSOP OUTLINE DIMENSIONS						
	INCHES			MILLIMETERS		
SYMBOL	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	.047	-	-	1.20
A_1	.002	.004	.006	0.05	0.10	0.15
A_2	-	-	.035	-	-	0.90
B	.007	0.95	.012	0.19	.245	0.30
C	-	-	-	-	-	-
D	.252	.256	.260	6.40	6.50	6.60
E	.169	.173	.177	4.30	4.40	4.50
e	.026 BSC			0.65 BSC		
H	.246	.252	.258	6.25	6.40	6.55
a	0^0	4^0	8^0	0^0	4^0	8^0
L	.020	.025	.030	0.50	0.625	0.75