



MOTOROLA

Semiconductors

MC1558 MC1558N

MC1458 MC1458N

MC1458C

DUAL MC1741

INTERNALLY COMPENSATED, HIGH PERFORMANCE MONOLITHIC OPERATIONAL AMPLIFIERS

... designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components.

- No Frequency Compensation Required
- Short-Circuit Protection
- Wide Common-Mode and Differential Voltage Ranges
- Low-Power Consumption
- No Latch Up
- Low Noise Selections Offered – N Suffix

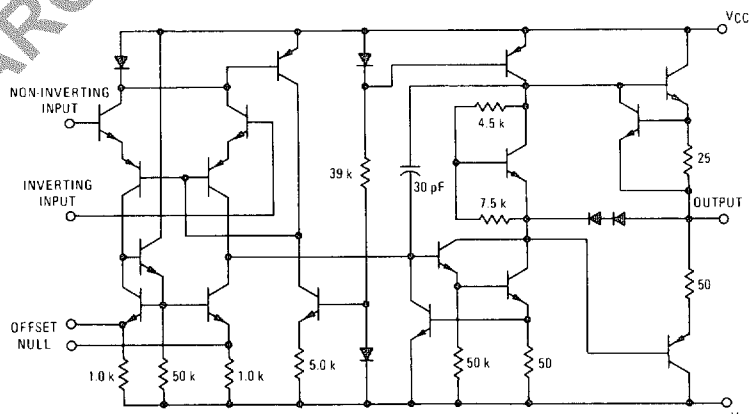
MAXIMUM RATINGS ($T_A = +25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	MC1458	MC1558	Unit
Power Supply Voltage	V_{CC} V_{EE}	+18 18	+22 -22	Vdc Vdc
Input Differential Voltage	V_{ID}	± 30		Volts
Input Common Mode Voltage (Note 1)	V_{ICM}	± 15		Volts
Output Short Circuit Duration (Note 2)	t_S	Continuous		
Operating Ambient Temperature Range	T_A	0 to +70	-55 to +125	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to +150		$^\circ\text{C}$
Metal, Flat and Ceramic Packages		-55 to +125		
Junction Temperature	T_J	175		$^\circ\text{C}$
Metal and Ceramic Package		150		
Plastic Package				

Note 1. For supply voltages less than ± 15 V, the absolute maximum input voltage is equal to the supply voltage.

Note 2. Supply voltage equal to or less than 15 V.

EQUIVALENT CIRCUIT SCHEMATIC

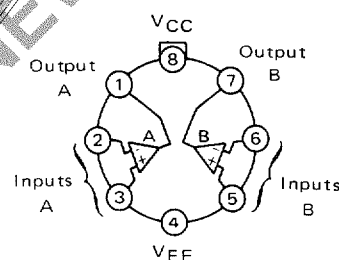


(DUAL MC1741)

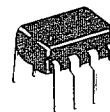
DUAL OPERATIONAL AMPLIFIER

SILICON MONOLITHIC INTEGRATED CIRCUIT

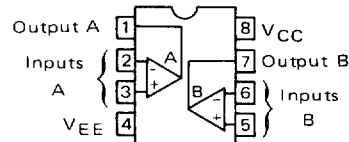
G SUFFIX
METAL PACKAGE
CASE 601



P1 SUFFIX
PLASTIC PACKAGE
CASE 626
(MC1458, MC1458C, MC1458N)



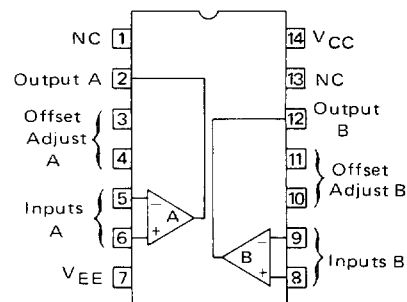
U SUFFIX
CERAMIC PACKAGE
CASE 693



L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116



P2 SUFFIX
PLASTIC PACKAGE
CASE 646
(MC1458, MC1458C, MC1458N)



ELECTRICAL CHARACTERISTICS ($V_{CC} = 15\text{ V}$, $V_{EE} = 15\text{ V}$, $T_A = 25^\circ\text{C}$ unless otherwise noted).

Characteristic	Symbol	MC1558			MC1458			MC1458C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage ($R_S \leq 10\text{ k}$)	V_{IO}	—	1.0	5.0	—	2.0	6.0	—	2.0	10	mV
Input Offset Current	I_{IO}	—	20	200	—	20	200	—	20	300	nA
Input Bias Current	I_{IB}	—	80	500	—	80	500	—	80	700	nA
Input Resistance	r_i	0.3	2.0	—	0.3	2.0	—	—	2.0	—	M Ω
Input Capacitance	C_i	—	1.4	—	—	1.4	—	—	1.4	—	pF
Offset Voltage Adjustment Range	V_{IOR}	—	± 15	—	—	± 15	—	—	± 15	—	mV
Common Mode Input Voltage Range	V_{ICR}	± 12	± 13	—	± 12	± 13	—	± 11	± 13	—	V
Large Signal Voltage Gain ($V_O = \pm 10\text{ V}$, $R_L = 2.0\text{ k}$) ($V_O = \pm 10\text{ V}$, $R_L = 10\text{ k}$)	A_v	50	200	—	20	200	—	—	200	—	V/mV
Output Resistance	r_o	—	75	—	—	75	—	—	75	—	Ω
Common Mode Rejection Ratio ($R_S \leq 10\text{ k}$)	CMRR	70	90	—	70	90	—	60	90	—	dB
Supply Voltage Rejection Ratio ($R_S \leq 10\text{ k}$)	PSRR	—	30	150	—	30	150	—	30	—	$\mu\text{V/V}$
Output Voltage Swing ($R_L \geq 10\text{ k}$) ($R_L \geq 2\text{ k}$)	V_O	± 12 ± 10	± 14 ± 13	—	± 12 ± 10	± 14 ± 13	—	± 11 ± 9.0	± 14 ± 13	—	V
Output Short-Circuit Current	I_{os}	—	20	—	—	20	—	—	20	—	mA
Supply Currents (Both Amplifiers)	I_D	—	2.3	5.0	—	2.3	5.6	—	2.3	8.0	mA
Power Consumption	P_C	—	70	150	—	70	170	—	70	240	mW
Transient Response (Unity Gain) ($V_i = 20\text{ mV}$, $R_L \geq 2\text{ k}\Omega$, $C_L \leq 100\text{ pF}$) Rise Time ($V_i = 20\text{ mV}$, $R_L \geq 2\text{ k}\Omega$, $C_L \leq 100\text{ pF}$) Overshoot ($V_i = 10\text{ V}$, $R_L \geq 2\text{ k}\Omega$, $C_L \leq 100\text{ pF}$) Slew Rate	t_{TLH} t_{os} SR	— — —	0.3 15 0.5	— — —	— — —	0.3 15 0.5	— — —	— — —	0.3 15 0.5	— — —	μs % V/ μs

ELECTRICAL CHARACTERISTICS ($V_{CC} = 15\text{ V}$, $V_{EE} = 15\text{ V}$, $T_A = *T_{\text{high}}$ to T_{low} unless otherwise noted).

Characteristic	Symbol	MC1558			MC1458			MC1458C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage ($R_S \leq 10\text{ k}\Omega$)	V_{IO}	—	1.0	6.0	—	—	7.5	—	—	12	mV
Input Offset Current ($T_A = 125^\circ\text{C}$) ($T_A = -55^\circ\text{C}$) ($T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$)	I_{IO}	— — —	7.0 85 —	200 500 —	— — —	— — —	— — 300	— — —	— — 400	—	nA
Input Bias Current ($T_A = 125^\circ\text{C}$) ($T_A = -55^\circ\text{C}$) ($T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$)	I_{IB}	— — —	30 300 —	500 1500 —	— — —	— — —	— — 800	— — —	— — 1000	—	nA
Common Mode Input Voltage Range	V_{ICR}	± 12	± 13	—	—	—	—	—	—	—	V
Common Mode Rejection Ratio ($R_S \leq 10\text{ k}$)	CMRR	70	90	—	—	—	—	—	—	—	dB
Supply Voltage Rejection Ratio ($R_S \leq 10\text{ k}$)	PSRR	—	30	150	—	—	—	—	—	—	$\mu\text{V/V}$
Output Voltage Swing ($R_L \geq 10\text{ k}$) ($R_L \geq 2\text{ k}$)	V_O	± 12 ± 10	± 14 ± 13	—	± 12 ± 10	± 14 ± 13	—	— ± 9.0	— ± 13	—	V
Large Signal Voltage Gain ($V_O = \pm 10\text{ V}$, $R_L = 2\text{ k}$) ($V_O = \pm 10\text{ V}$, $R_L = 10\text{ k}$)	A_v	25 —	— —	— —	15 —	— —	— —	— 15	— —	—	V/mV
Supply Currents (Both Amplifiers) ($T_A = 125^\circ\text{C}$) ($T_A = -55^\circ\text{C}$)	I_D	— —	— —	4.5 6.0	— —	— —	— —	— —	— —	—	mA
Power Consumption ($T_A = 125^\circ\text{C}$) ($T_A = -55^\circ\text{C}$)	P_C	— —	— —	135 180	— —	— —	— —	— —	— —	—	mW

* $T_{\text{high}} = 125^\circ\text{C}$ for MC1558 and 70°C for MC1458, MC1458C

$T_{\text{low}} = -55^\circ\text{C}$ for MC1558 and 0°C for MC1458, MC1458C



MOTOROLA Semiconductor Products Inc.

FIGURE 12 – NON-INVERTING PULSE RESPONSE

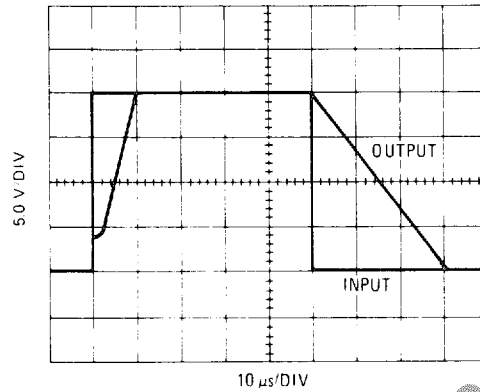


FIGURE 13 – TRANSIENT RESPONSE TEST CIRCUIT

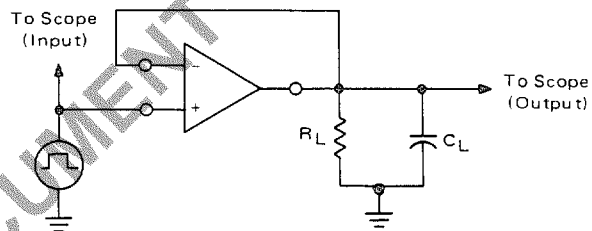
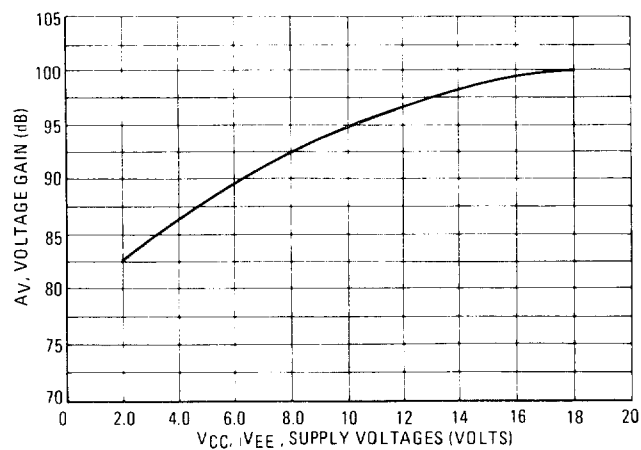


FIGURE 14 – OPEN LOOP VOLTAGE GAIN
versus SUPPLY VOLTAGE



TYPICAL CHARACTERISTICS

($V_{CC} = +15\text{ Vdc}$, $V_{EE} = -15\text{ Vdc}$, $T_A = +25^\circ\text{C}$ unless otherwise noted).

**FIGURE 6 – POWER BANDWIDTH
(LARGE SIGNAL SWING versus FREQUENCY)**

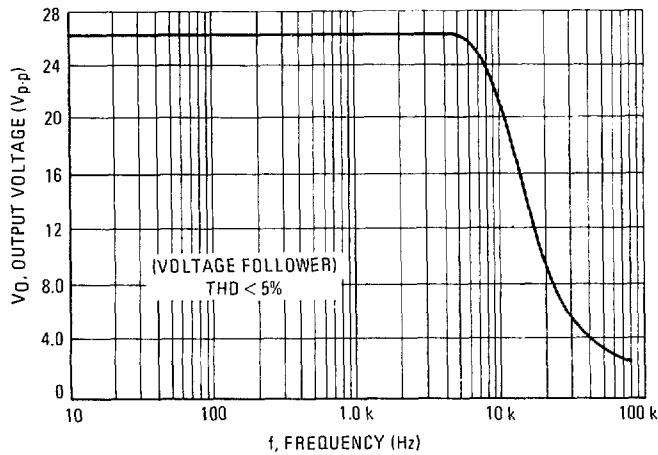
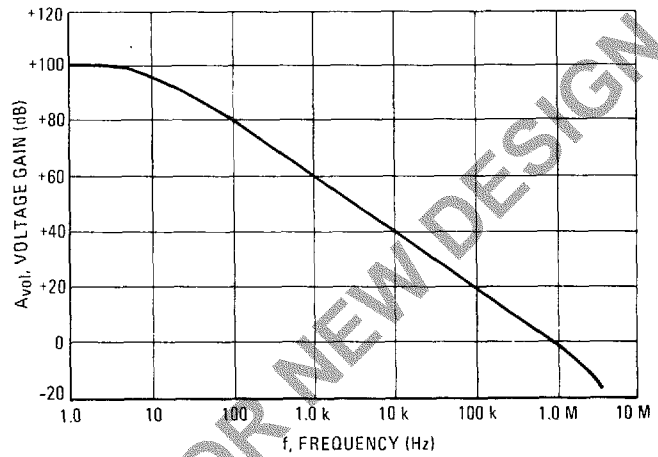
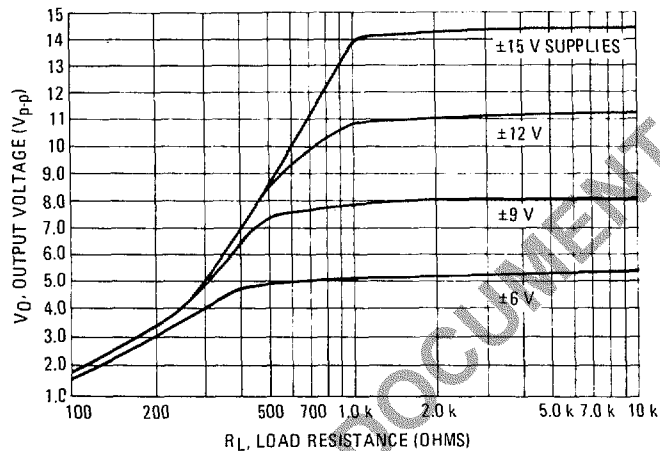


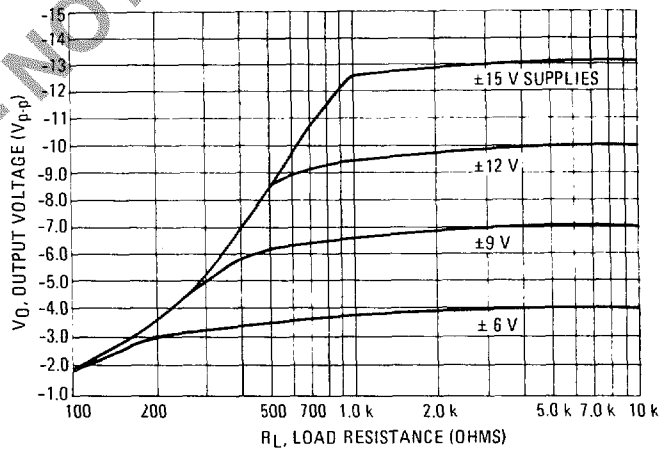
FIGURE 7 – OPEN LOOP FREQUENCY RESPONSE



**FIGURE 8 – POSITIVE OUTPUT VOLTAGE SWING
versus LOAD RESISTANCE**



**FIGURE 9 – NEGATIVE OUTPUT VOLTAGE SWING
versus LOAD RESISTANCE**



**FIGURE 10 – OUTPUT VOLTAGE SWING versus
LOAD RESISTANCE (Single Supply Operation)**

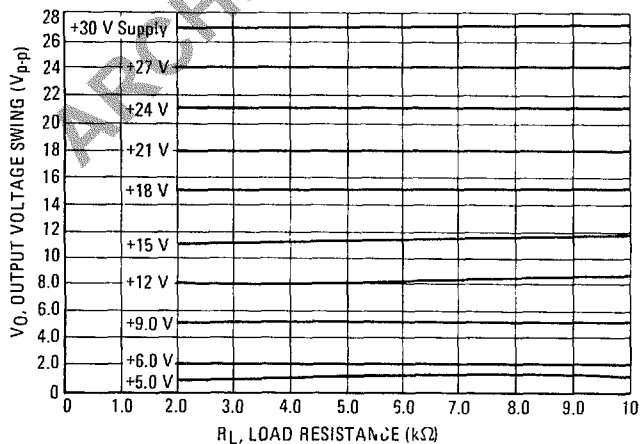
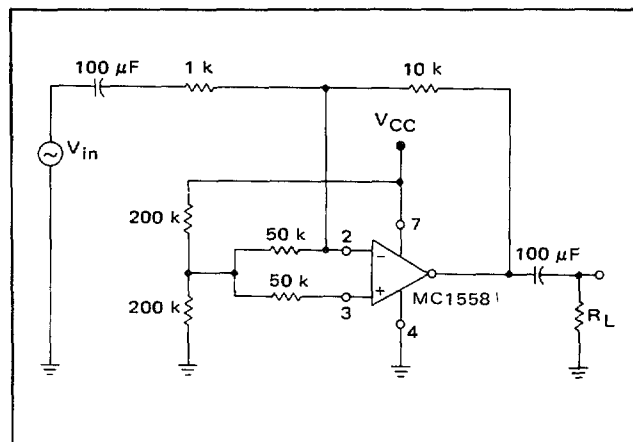


FIGURE 11 – SINGLE SUPPLY INVERTING AMPLIFIER



NOISE CHARACTERISTICS (Applies for MC1558N and MC1458N only, $V_{CC} = 15\text{ V}$, $V_{EE} = -15\text{ V}$, $T_A = 25^\circ\text{C}$)

Characteristic	Symbol	MC1558N			MC1458N			Unit
		Min	Typ	Max	Min	Typ	Max	
Burst Noise (Popcorn Noise) (BW = 1.0 Hz to 1.0 kHz, $t = 10\text{ s}$, $R_S = 100\text{ k}\Omega$) (Input Referenced)	E_n	—	—	20	—	—	20	$\mu\text{V}_{\text{peak}}$

FIGURE 1 – BURST NOISE versus SOURCE RESISTANCE

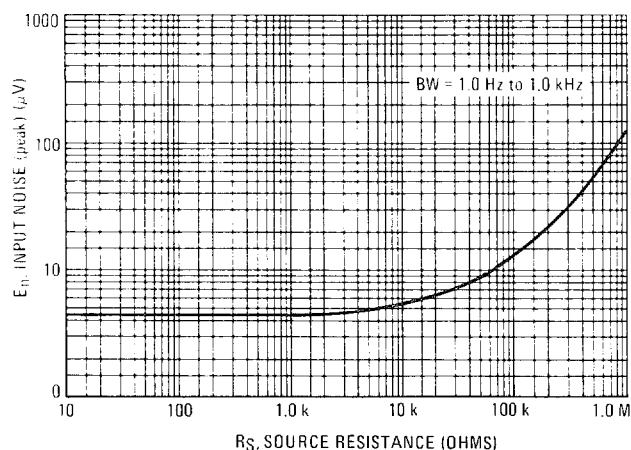


FIGURE 2 – RMS NOISE versus SOURCE RESISTANCE

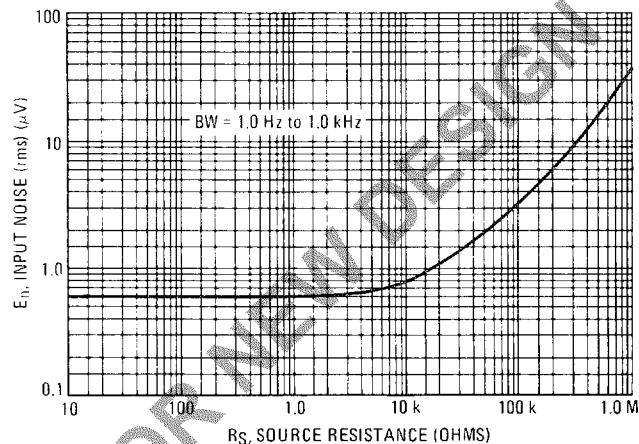


FIGURE 3 – OUTPUT NOISE versus SOURCE RESISTANCE

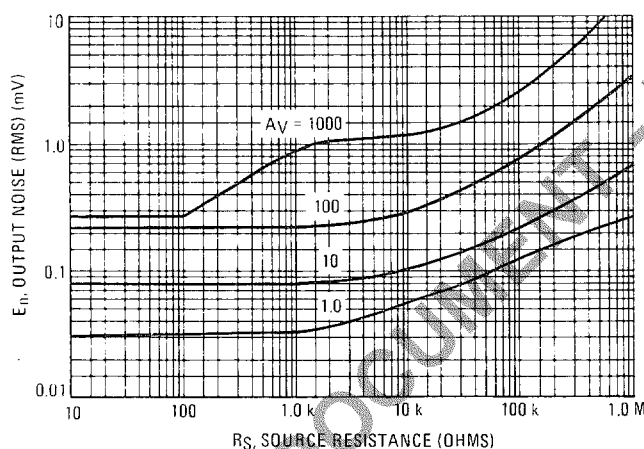


FIGURE 4 – SPECTRAL NOISE DENSITY

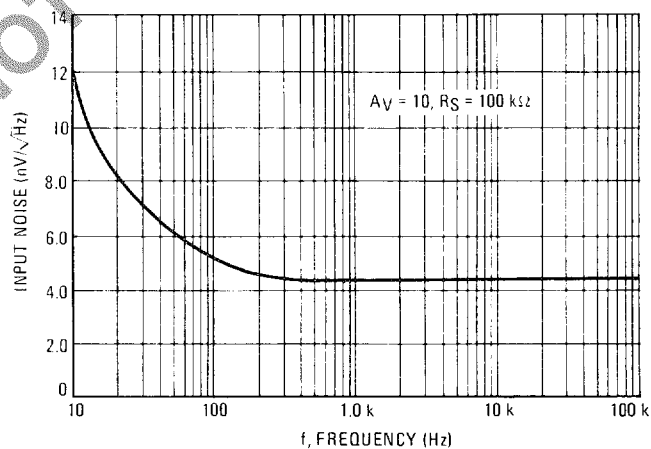
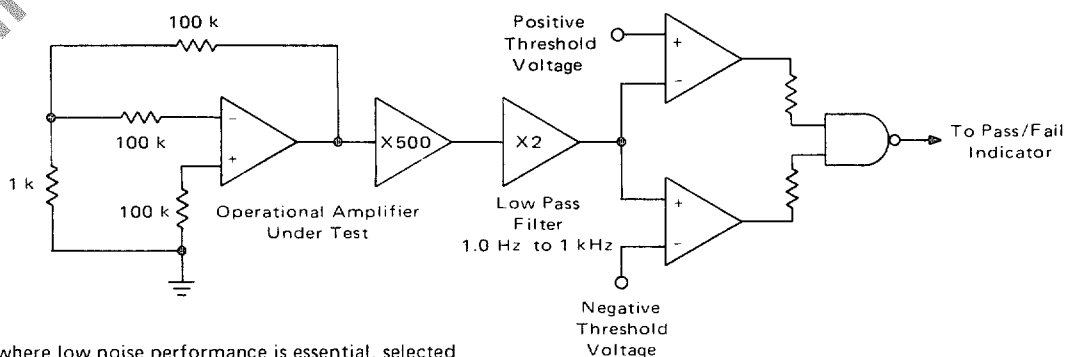


FIGURE 5 – BURST NOISE TEST CIRCUIT (N Suffixed Devices Only)



For applications where low noise performance is essential, selected devices denoted by an N suffix are offered. These units have been 100% tested for burst noise pulses on a special noise test system. Unlike conventional peak reading or RMS meters, this system was especially designed to provide the quick response time essential to burst (popcorn) noise testing.

The test time employed is 10 seconds and the 20 μV peak limit refers to the operational amplifier input thus eliminating errors in the closed-loop gain factor of the operational amplifier under test.



THERMAL INFORMATION

The maximum power consumption an integrated circuit can tolerate at a given operating ambient temperature, can be found from the equation:

$$P_D(T_A) = \frac{T_{J(max)} - T_A}{R_{\theta JA}(Typ)}$$

Where: $P_D(T_A)$ = Power Dissipation allowable at a given operating ambient temperature. This must be greater than

the sum of the products of the supply voltages and supply currents at the worst case operating condition.

$T_{J(max)}$ = Maximum Operating Junction Temperature
as listed in the Maximum Ratings Section

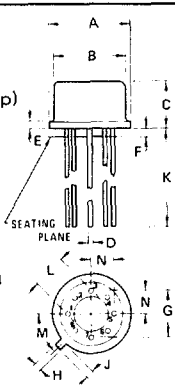
T_A = Maximum Desired Operating Ambient
Temperature

$R_{\theta JA}(Typ)$ = Typical Thermal Resistance Junction to
Ambient

G SUFFIX
METAL PACKAGE
CASE 601
 $R_{\theta JC} = 160^\circ\text{C/W (Typ)}$

NOTE:
1. LEADS WITHIN 0.25 mm (0.010)
DIA OF TRUE POSITION AT
SEATING PLANE AT MAXIMUM
MATERIAL CONDITION.

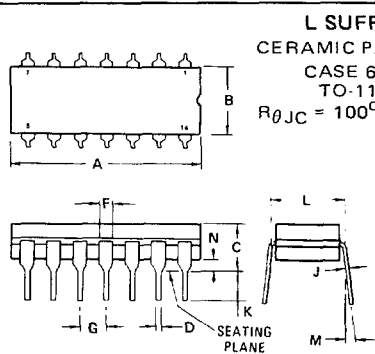
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.51	9.40	0.335	0.370
B	7.75	8.51	0.305	0.335
C	4.19	4.70	0.165	0.185
D	0.41	0.48	0.016	0.019
E	0.25	1.02	0.010	0.040
F	0.25	1.02	0.010	0.040
G	5.08	BSC	0.200	BSC
H	0.71	0.86	0.028	0.034
J	0.74	1.14	0.029	0.045
K	12.70	-	0.500	-
L	3.05	4.06	0.120	0.160
M	45°	BSC	45°	BSC
N	2.41	2.67	0.095	0.105



L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116
 $R_{\theta JC} = 100^\circ\text{C/W (Typ)}$

NOTE:
1. DIMENSION "L" TO CENTER OF
LEADS WHEN FORMED PARALLEL

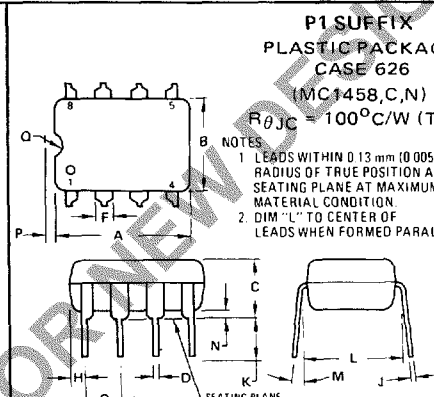
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	19.05	19.81	0.750	0.780
B	6.22	6.99	0.245	0.275
C	4.32	5.08	0.170	0.200
D	0.41	0.51	0.016	0.020
E	1.45	1.60	0.057	0.063
F	2.54	BSC	0.100	BSC
G	1.91	2.29	0.075	0.090
H	0.20	0.30	0.008	0.012
J	3.18	4.06	0.125	0.160
K	7.62	BSC	0.300	BSC
L	-	15°	-	15°
M	0.51	0.76	0.020	0.030



P1 SUFFIX
PLASTIC PACKAGE
CASE 626
(MC1458, C, N)
 $R_{\theta JC} = 100^\circ\text{C/W (Typ)}$

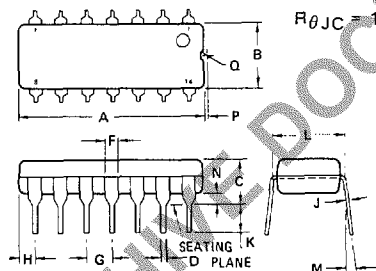
NOTES:
1. LEADS WITHIN 0.13 mm (0.005)
RADIUS OF TRUE POSITION AT
SEATING PLANE AT MAXIMUM
MATERIAL CONDITION.
2. DIM "L" TO CENTER OF
LEADS WHEN FORMED PARALLEL

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.40	10.16	0.370	0.400
B	5.10	6.60	0.240	0.260
C	3.94	4.45	0.155	0.175
D	0.38	0.51	0.015	0.020
E	1.02	1.52	0.040	0.060
F	2.54	BSC	0.100	BSC
G	0.76	1.27	0.030	0.050
H	0.20	0.30	0.008	0.012
J	2.92	3.43	0.115	0.135
K	7.37	7.87	0.290	0.310
L	-	10°	-	10°
M	0.51	0.76	0.020	0.030
N	0.13	0.38	0.005	0.015
P	0.76	1.02	0.030	0.040



P2 SUFFIX
PLASTIC PACKAGE
CASE 646
(MC1458, C, N)
 $R_{\theta JC} = 100^\circ\text{C/W (Typ)}$

$R_{\theta JC} = 100^\circ\text{C/W (Typ)}$

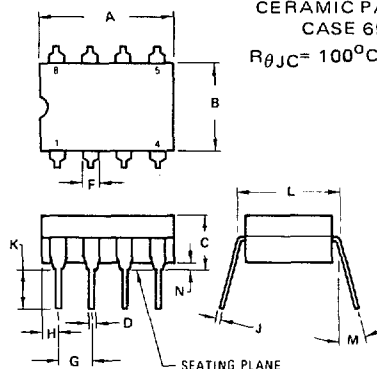


NOTES:
1. LEADS WITHIN 0.13 mm
(0.005) RADIUS OF TRUE
POSITION AT SEATING
PLANE AT MAXIMUM
MATERIAL CONDITION.
2. DIMENSION "L" TO
CENTER OF LEADS
WHEN FORMED
PARALLEL

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.16	18.80	0.715	0.740
B	6.10	6.60	0.240	0.260
C	4.06	4.57	0.160	0.180
D	0.38	0.51	0.015	0.020
E	1.02	1.52	0.040	0.060
F	2.54	BSC	0.100	BSC
G	1.32	1.83	0.052	0.072
H	0.20	0.30	0.008	0.012
J	2.92	3.43	0.115	0.135
K	7.37	7.87	0.290	0.310
L	-	10°	-	10°
M	0.51	1.02	0.020	0.040
N	0.13	0.38	0.005	0.015
P	0.51	0.76	0.020	0.030

U SUFFIX
CERAMIC PACKAGE
CASE 693
 $R_{\theta JC} = 100^\circ\text{C/W (Typ)}$

$R_{\theta JC} = 100^\circ\text{C/W (Typ)}$



NOTES:
1. LEADS WITHIN 0.13 mm (0.005)
RAD OF TRUE POSITION AT
SEATING PLANE AT MAXIMUM
MATERIAL CONDITION
2. DIMENSION "L" TO CENTER
OF LEADS WHEN FORMED
PARALLEL

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.91	10.92	0.390	0.430
B	6.22	6.99	0.245	0.275
C	4.32	5.08	0.170	0.200
D	0.41	0.51	0.016	0.020
E	1.40	1.65	0.055	0.065
F	2.54	BSC	0.100	BSC
G	1.14	1.65	0.045	0.065
H	0.20	0.30	0.008	0.012
J	3.18	4.06	0.125	0.160
K	7.37	7.87	0.290	0.310
L	-	15°	-	15°
M	0.51	1.02	0.020	0.040

Circuit diagrams utilizing Motorola products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and

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