Ordering number : EN3093A

2SA1707/2SC4487

Bipolar Transistor
(-)50V, (-)3A, Low VCE(sat), (PNP)NPN Single NMP

ON Semiconductor®

http://onsemi.com

Features

- Adoption of FBET, MBIT processes
- Low collector-to-emitter saturation voltage
- Large current capacity, wide ASO
- Fast switching speed

( )2SA1707

Specifications

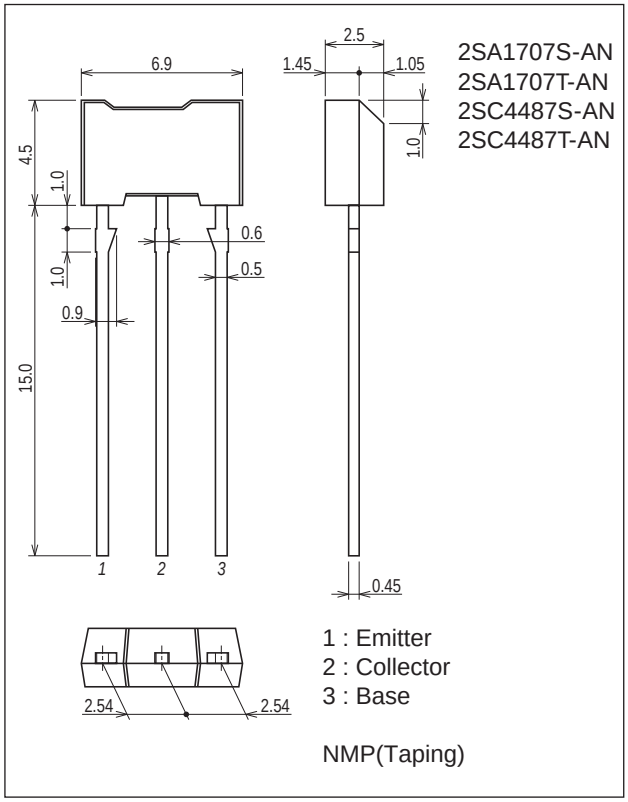
Absolute Maximum Ratings at Ta=25°C

Parameter	Symbol	Conditions	Ratings	Unit
Collector-to-Base Voltage	V_{CBO}		(–)60	V
Collector-to-Emitter Voltage	V_{CEO}		(–)50	V
Emitter-to-Base Voltage	V_{EBO}		(–)6	V
Collector Current	I_C		(–)3	A
Collector Current (Pulse)	I_{CP}		(–)6	A
Collector Dissipation	P_C		1	W
Junction Temperature	Tj		150	°C
Storage Temperature	Tstg		–55 to +150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Package Dimensions

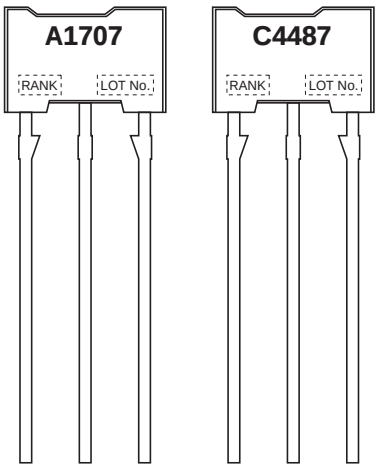
unit : mm (typ)
7540-001



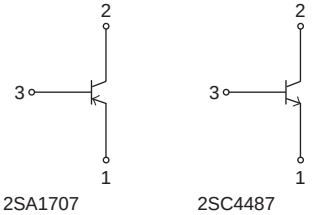
Product & Package Information

- Package : NMP(Taping)
- JEITA, JEDEC : SC-71
- Minimum Packing Quantity : 2,500 pcs./box

Marking(NMP(Taping))



Electrical Connection



Electrical Characteristics at Ta=25°C

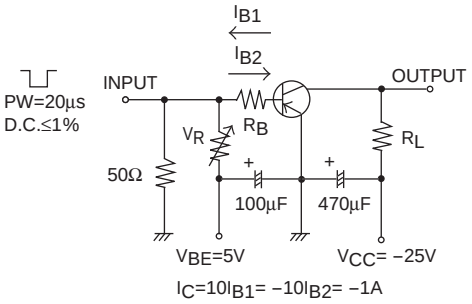
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Collector Cutoff Current	I_{CBO}	V_{CB}=(−)40V, I_E=0A			(−)1	μA
Emitter Cutoff Current	I_{EBO}	V_{EB}=(−)4V, I_C=0A			(−)1	μA
DC Current Gain	$h_{FE}1$	V_{CE}=(−)2V, I_C=(−)100mA	140*		400*	
	$h_{FE}2$	V_{CE}=(−)2V, I_C=(−)3A	35			
Gain-Bandwidth Product	f_T	V_{CE}=(−)10V, I_C=(−)50mA		150		MHz
Output Capacitance	Cob	V_{CB}=(−)10V, f=1MHz		(39)25		pF
Collector-to-Emitter Saturation Voltage	V_{CE}(sat)	I_C=(−)2A, I_B=(−)100mA		(−0.35)0.2	(−0.7)0.5	V
Base-to-Emitter Saturation Voltage	VBE(sat)			(−)0.95	(−)1.2	V
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C=(−)10μA, I_E=0A	(−)60			V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C=(−)1mA, R_{BE}=∞	(−)50			V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E=(−)10μA, I_C=0A	(−)6			V
Turn-On Time	t_{on}	See specified Test Circuit.		70		ns
Storage Time	t_{stg}			(450)650		ns
Fall Time	t_f			35		ns

* : The 2SA1707/2SC4487 are classified by 100mA h_{FE} as follows :

Rank	S	T
h_{FE}	140 to 280	200 to 400

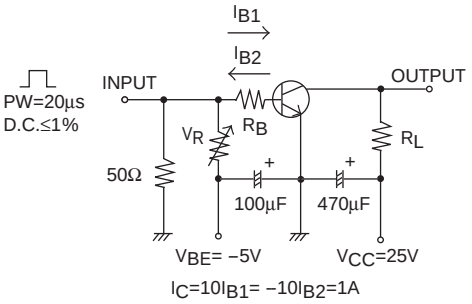
Switching Time Test Circuit

2SA1707



I_C=10I_{B1}= −10I_{B2}= −1A

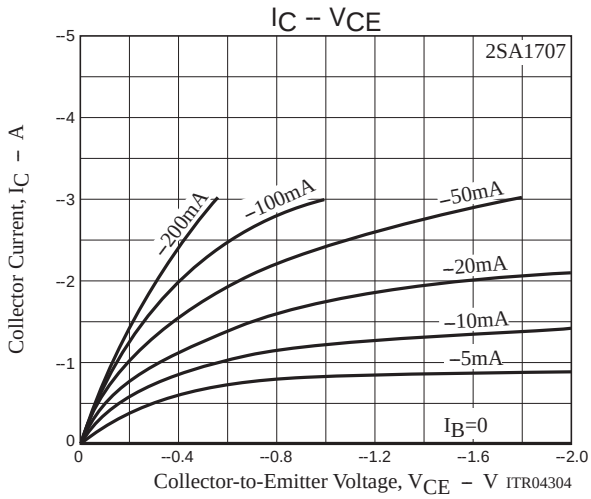
2SC4487

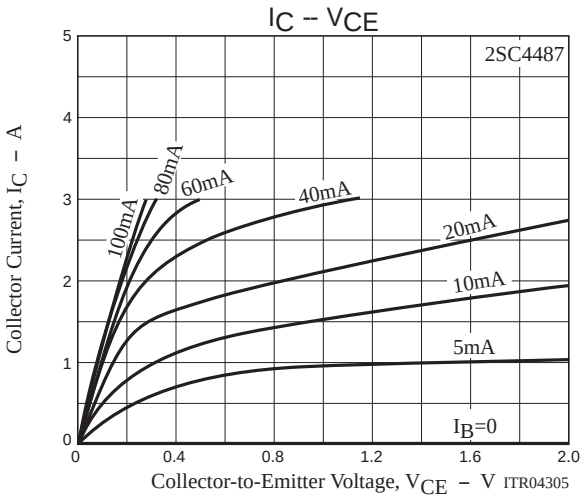


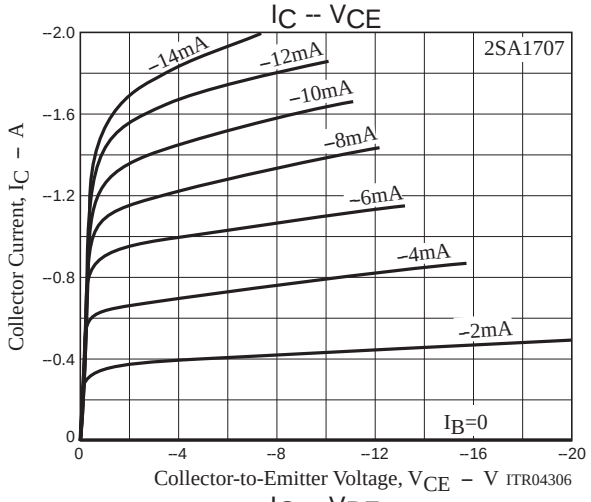
I_C=10I_{B1}= −10I_{B2}=1A

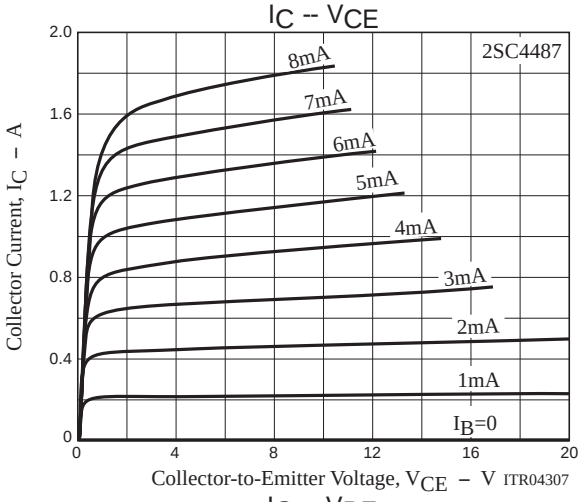
Ordering Information

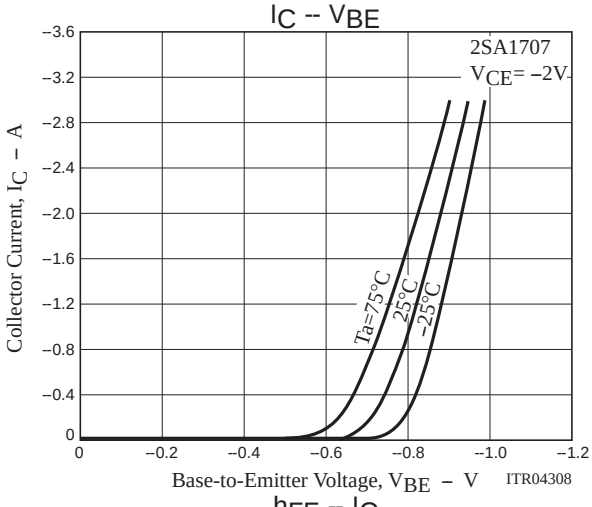
Device	Package	Shipping	memo
2SA1707S-AN	NMP(Taping)	2,500pcs./box	Pb Free
2SA1707T-AN	NMP(Taping)	2,500pcs./box	
2SC4487S-AN	NMP(Taping)	2,500pcs./box	
2SC4487T-AN	NMP(Taping)	2,500pcs./box	

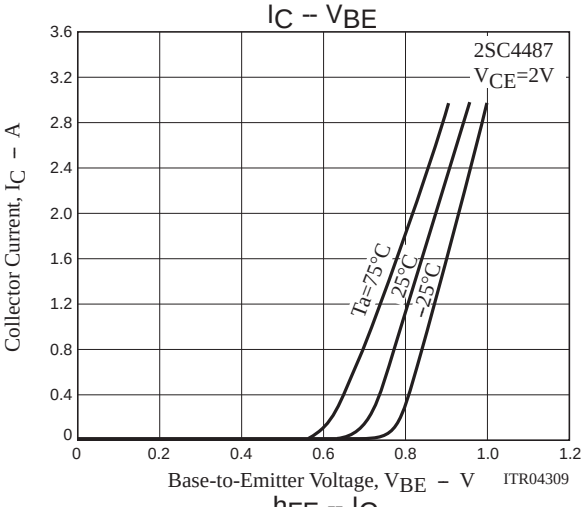

IC -- VCE
2SA1707
Collector Current, IC – A
−200mA
−100mA
−50mA
−20mA
−10mA
−5mA
IB=0
Collector-to-Emitter Voltage, VCE – V
ITR04304

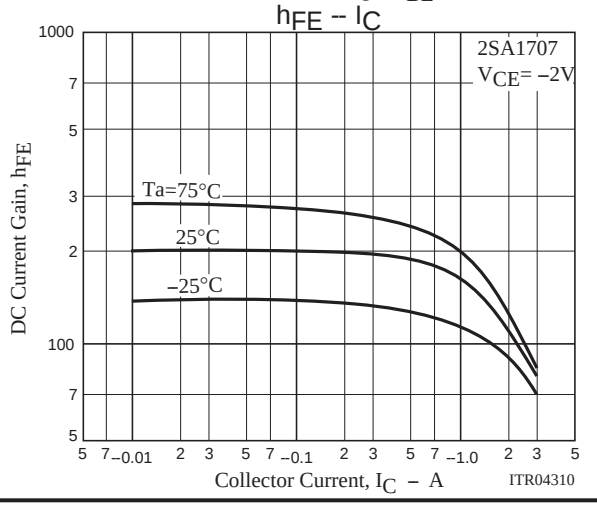

IC -- VCE
2SC4487
Collector Current, IC – A
100mA
80mA
60mA
40mA
20mA
10mA
5mA
IB=0
Collector-to-Emitter Voltage, VCE – V
ITR04305

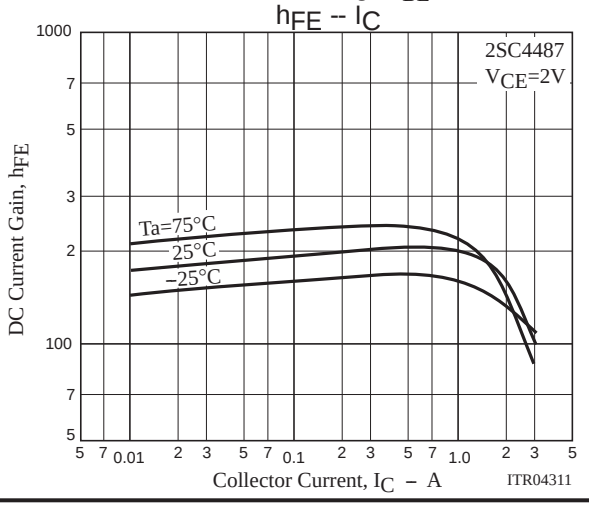

IC -- VCE
2SA1707
Collector Current, IC – A
−14mA
−12mA
−10mA
−8mA
−6mA
−4mA
−2mA
IB=0
Collector-to-Emitter Voltage, VCE – V
ITR04306

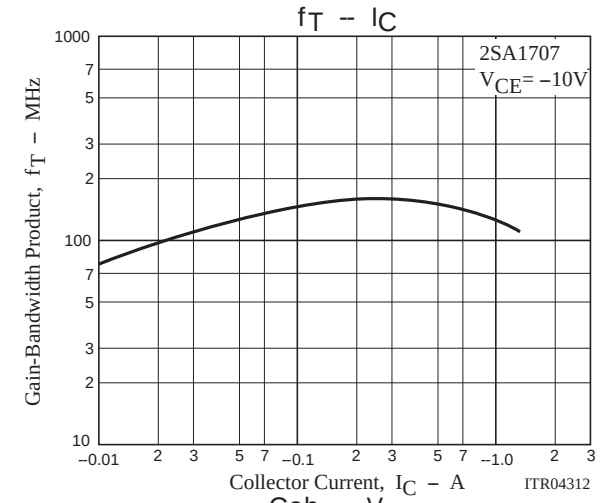

IC -- VCE
2SC4487
Collector Current, IC – A
8mA
7mA
6mA
5mA
4mA
3mA
2mA
1mA
IB=0
Collector-to-Emitter Voltage, VCE – V
ITR04307

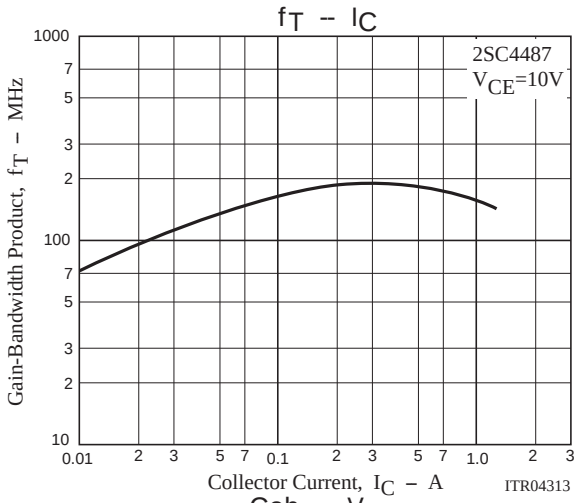

IC -- VBE
2SA1707
VCE= −2V
Collector Current, IC – A
Ta=75°C
25°C
−25°C
Base-to-Emitter Voltage, VBE – V
ITR04308

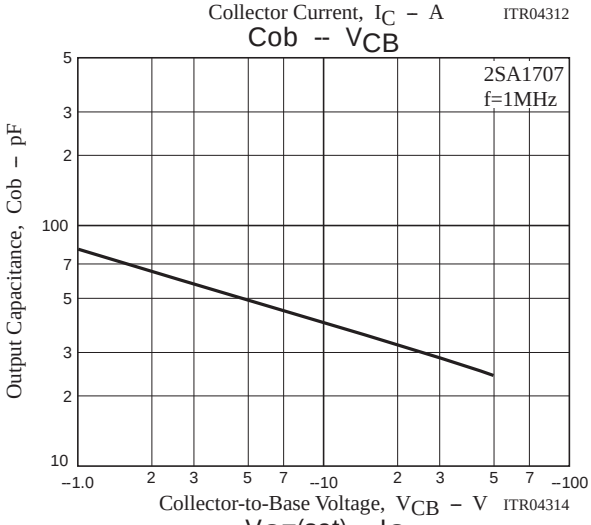

IC -- VBE
2SC4487
VCE=2V
Collector Current, IC – A
Ta=75°C
25°C
−25°C
Base-to-Emitter Voltage, VBE – V
ITR04309

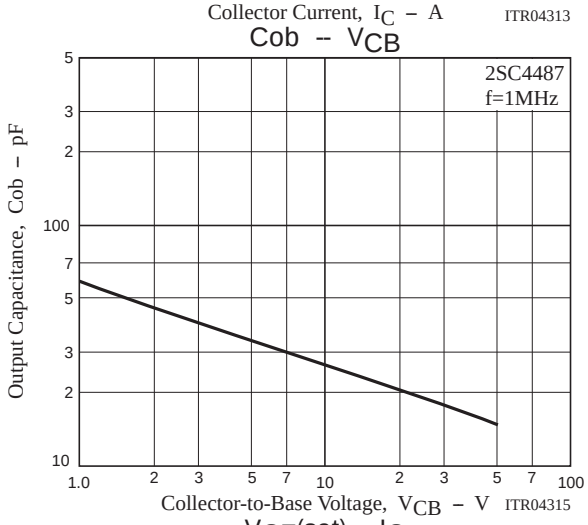

hFE -- IC
2SA1707
VCE= −2V
DC Current Gain, hFE
Ta=75°C
25°C
−25°C
Collector Current, IC – A
ITR04310

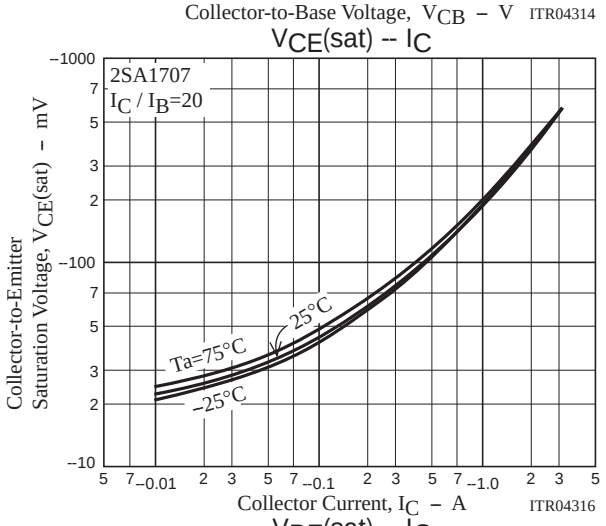

hFE -- IC
2SC4487
VCE=2V
DC Current Gain, hFE
Ta=75°C
25°C
−25°C
Collector Current, IC – A
ITR04311

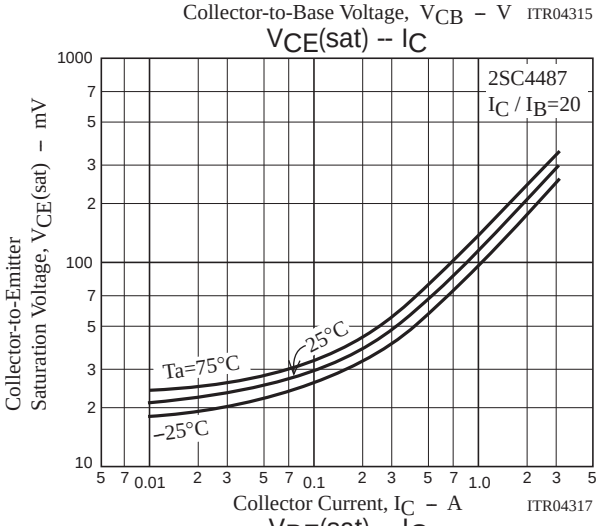

fT -- IC
2SA1707
VCE= −10V
Gain-Bandwidth Product, fT – MHz
Collector Current, IC – A
ITR04312

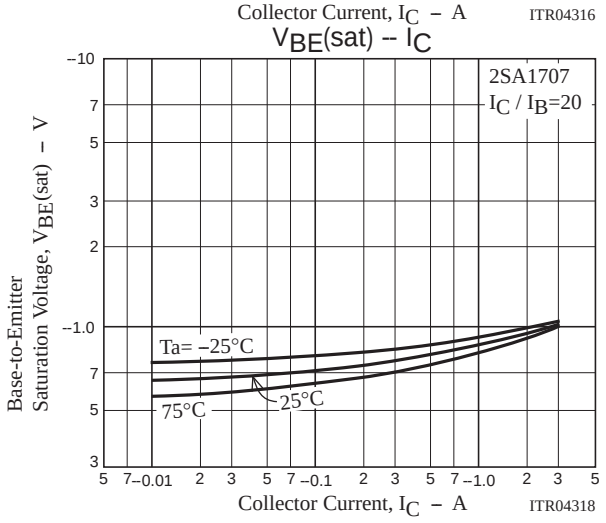

fT -- IC
2SC4487
VCE=10V
Gain-Bandwidth Product, fT – MHz
Collector Current, IC – A
ITR04313

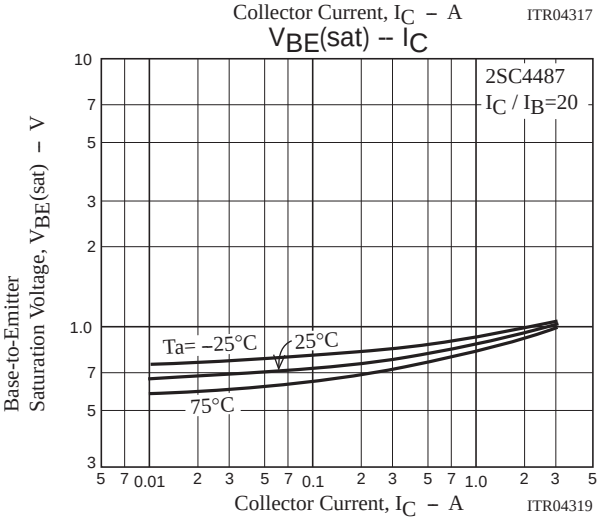

Cob -- VCB
2SA1707
f=1MHz
Output Capacitance, Cob – pF
Collector-to-Base Voltage, VCB – V
ITR04314

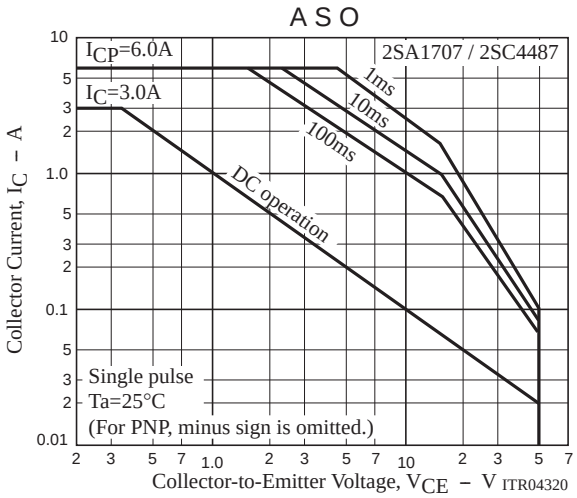

Cob -- VCB
2SC4487
f=1MHz
Output Capacitance, Cob – pF
Collector-to-Base Voltage, VCB – V
ITR04315

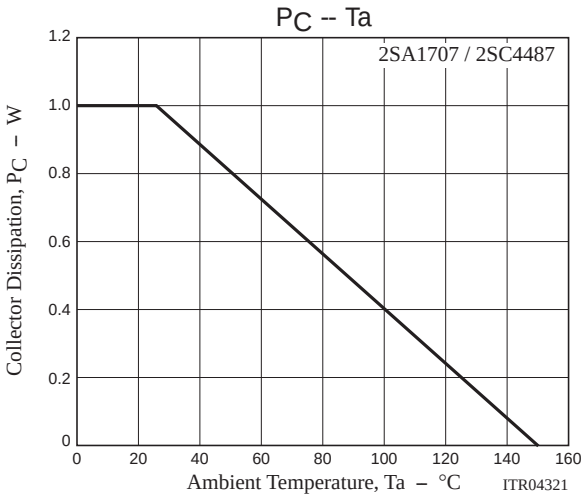

VCE(sat) -- IC
2SA1707
IC / IB=20
Ta=75°C
25°C
−25°C
Collector-to-Emitter Saturation Voltage, VCE(sat) – mV
Collector Current, IC – A
ITR04316


VCE(sat) -- IC
2SC4487
IC / IB=20
Ta=75°C
25°C
−25°C
Collector-to-Emitter Saturation Voltage, VCE(sat) – mV
Collector Current, IC – A
ITR04317


VBE(sat) -- IC
2SA1707
IC / IB=20
Ta= −25°C
75°C
25°C
Base-to-Emitter Saturation Voltage, VBE(sat) – V
Collector Current, IC – A
ITR04318


VBE(sat) -- IC
2SC4487
IC / IB=20
Ta= −25°C
75°C
25°C
Base-to-Emitter Saturation Voltage, VBE(sat) – V
Collector Current, IC – A
ITR04319


A S O
2SA1707 / 2SC4487
I_{CP}=6.0A
I_C=3.0A
1ms
10ms
100ms
DC operation
Single pulse
Ta=25°C
(For PNP, minus sign is omitted.)
Collector Current, I_C – A
Collector-to-Emitter Voltage, V_{CE} – V
ITR04320


P_C -- Ta
2SA1707 / 2SC4487
Collector Dissipation, P_C – W
Ambient Temperature, Ta – °C
ITR04321

Bag Packing Specification

2SA1707S-AN, 2SA1707T-AN, 2SC4487S-AN, 2SC4487T-AN

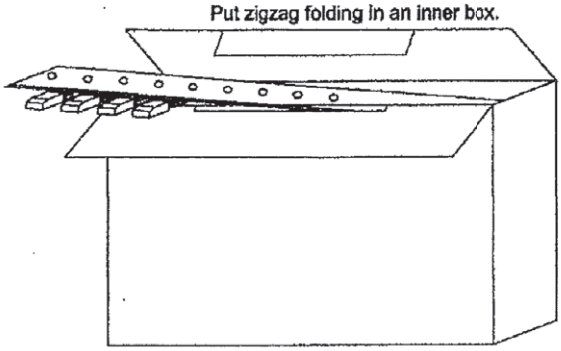
NMP (Zigzag folding)

Storage package Outline name	Package type	Maximum Number of devices contained (pcs.)		Packing format	
		Inner box No.	Storage quantity	Outer box (C—6)	Outer box (C—8)
NMP	AN/AZ	C—3 Inner box Dimensions :mm(external) 330×45×125	2,500	8 inner boxes contained(20,000pcs.) Outer box Dimensions:mm(external) 585×345×195	4 inner boxes contained(10,000pcs.) Outer box Dimensions:mm(external) 345×300×195

1. Packing format

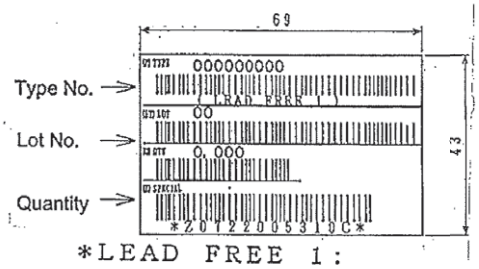
Packing method

Put zigzag folding in an inner box.



2. Bar code label

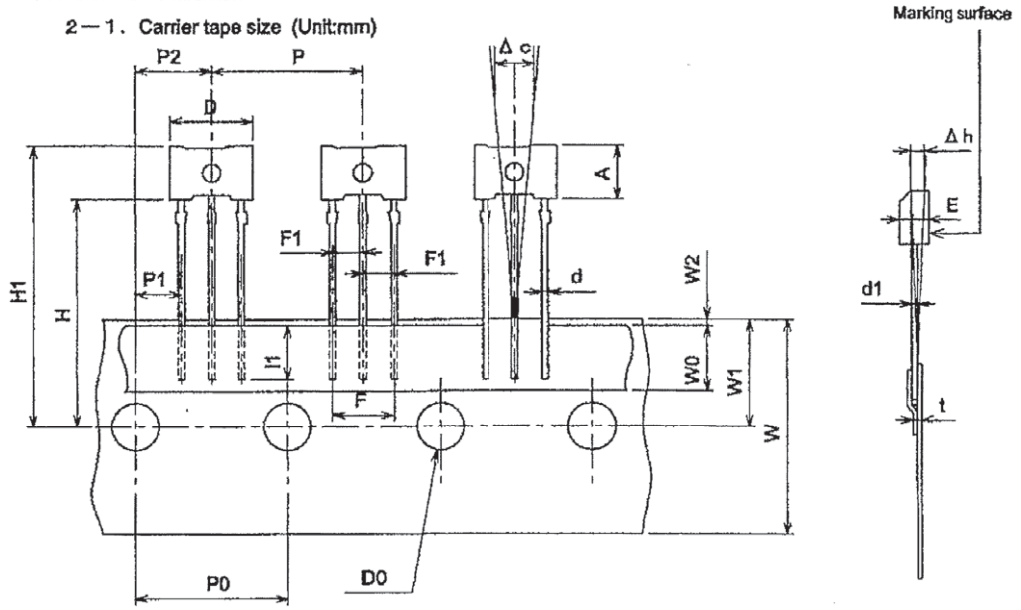
(Unit : mm)



*LEAD FREE 1 :
Lead-free External terminal surface treatment product.

2. Taping specifications

2—1. Carrier tape size (Unit:mm)



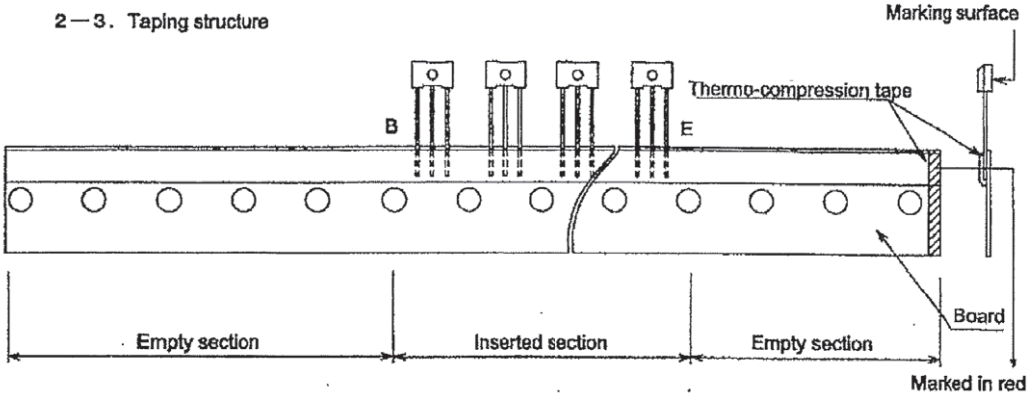
2—2. Taping size standard

Unit:mm

Item	Symbol	Standard	Tolerance
Work piece outside diameter	D	6.9	±0.2
	E	2.5	±0.2
Work piece height	A	4.5	±0.2
Lead wire diameter	d	0.5	±0.1
Lead wire thickness	d1	0.45	±0.1
Bonded lead wire	l1	3.0MIN	
Pitch between products	P	12.7	±0.5
Pitch between perforations	P0	12.7	±0.2
Total pitch for 21 perforations	P0×20	254.0	±1.0
Distance between lead wire	F	5.0	+0.8 -0.2
Lead wire pitch distance	F1	2.54	+0.4 -0.1
Displacement of perforations	P1	3.81	±0.3
	P2	6.35	±0.3
Displacement of tape	W2	0～0.5	

Item	Symbol	Standard	Tolerance
Tape width	W	18.0	±0.5
Adhesive tape	W0	6.0	±0.5
Displacement of perforations	W1	9.0	±0.5
Work piece bottom surface position	H	19.0	+1.0 -0.5
Work piece upper limit position	H1	23.5	±1.0
Perforations diameter	D0	φ4.0	±0.2
Tape thickness (total thickness)	t	0.6	±0.2
Product inclination	Δc	0	±0.7
Product inclination	Δh	0	±1.0

2—3. Taping structure



- Provide an empty section for about three to five pieces in leading and end portions of the tape.
- Provide an empty section in the fold-back portion.
- Provide marking in red to the E-side end of the board.

Outline Drawing

2SA1707S-AN, 2SA1707T-AN, 2SC4487S-AN, 2SC4487T-AN