3A, 23V, 340kHz Synchronous Step-Down Converter

General Description

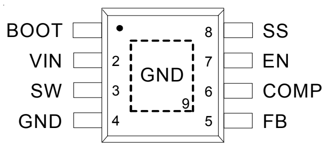
The RT8290 is a high efficiency synchronous step-down DC/DC converter that can deliver up to 3A output current from 4.5V to 23V input supply. The RT8290's current mode architecture and external compensation allow the transient response to be optimized over a wide range of loads and output capacitors. Cycle-by-cycle current limit provides protection against shorted outputs and soft-start eliminates input current surge during start-up. The RT8290 also provides output under voltage protection and thermal shutdown protection. The low current (<3μA) shutdown mode provides output disconnection, enabling easy power management in battery-powered systems. The RT8290 is availablein an SOP-8 (Exposed Pad) package.

Applications

- Industrial and Commercial Low Power Systems
- Computer Peripherals
- LCD Monitors and TVs
- Green Electronics/Appliances
- Point of Load Regulation of High-Performance DSPs, FPGAs and ASICs.

Pin Configurations

(TOP VIEW)



SOP-8 (Exposed Pad)

Features

- **4.5V to 23V Input Voltage Range**
- **1.5% High Accuracy Feedback Voltage**
- **3A Output Current**
- **Integrated N-MOSFET Switches**
- **Current Mode Control**
- **Fixed Frequency Operation : 340kHz**
- **Output Adjustable from 0.925V to 20V**
- **Up to 95% Efficiency**
- **Programmable Soft-Start**
- **Stable with Low-ESR Ceramic Output Capacitors**
- **Cycle-by-Cycle Over Current Protection**
- **Input Under Voltage Lockout**
- **Output Under Voltage Protection**
- **Thermal Shutdown Protection**
- **Thermally Enhanced SOP-8 (Exposed Pad) Package**
- **RoHS Compliant and Halogen Free**

Ordering Information

RT8290□□

Package Type
SP : SOP-8 (Exposed Pad-Option 1)

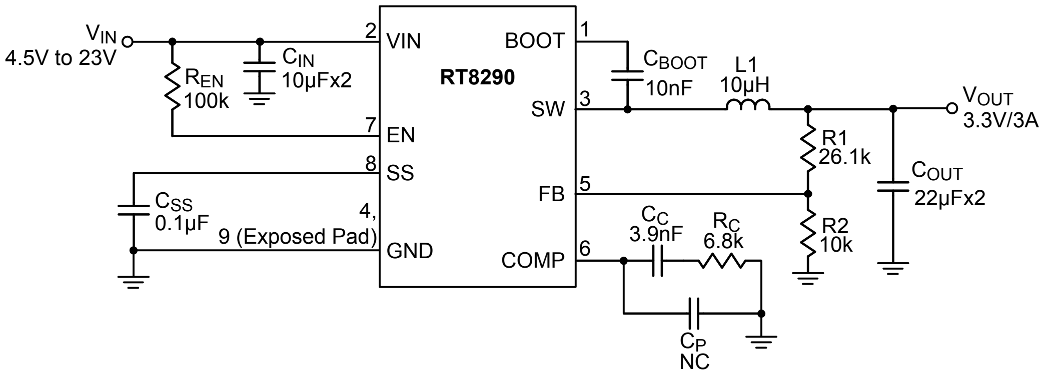
Lead Plating System
G : Green (Halogen Free and Pb Free)
Z : ECO (Ecological Element with Halogen Free and Pb free)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Typical Application Circuit



Marking Information

RT8290 GSPYMDNN •

RT8290GSP : Product Number

YMDNN : Date Code

RT8290 ZSPYMDNN •

RT8290ZSP : Product Number

YMDNN : Date Code

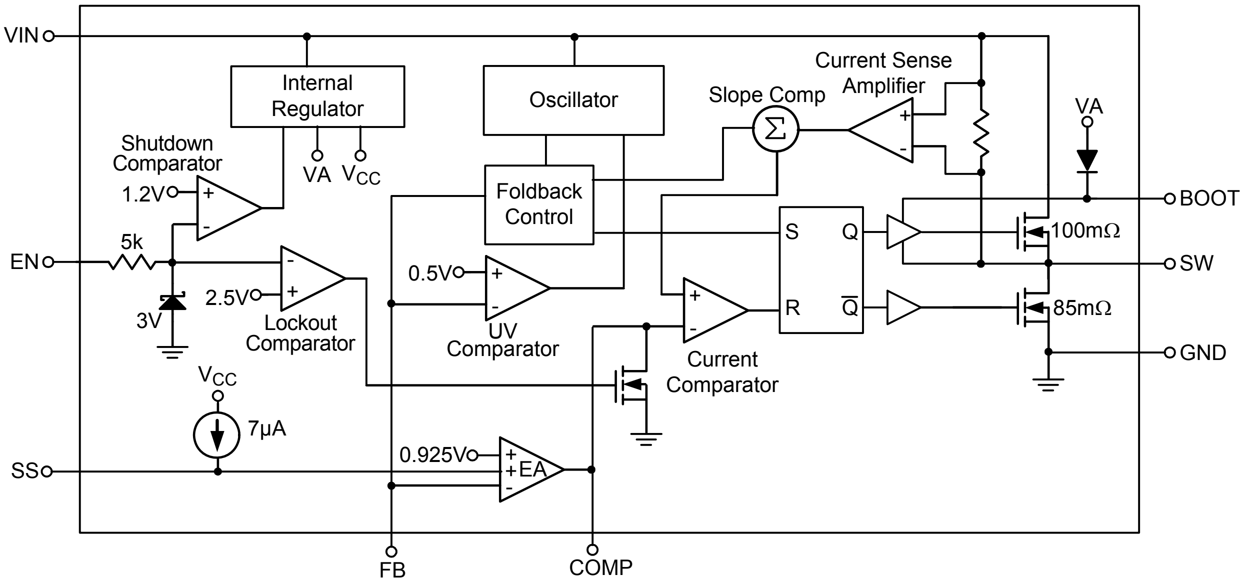
Table 1. Recommended Component Selection

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	R_C (kΩ)	C_C (nF)	L (μH)	C_{OUT} (μF)
15	153	10	30	3.9	33	22 x 2
10	97.6	10	20	3.9	22	22 x 2
8	76.8	10	15	3.9	22	22 x 2
5	45.3	10	13	3.9	15	22 x 2
3.3	26.1	10	6.8	3.9	10	22 x 2
2.5	16.9	10	6.2	3.9	6.8	22 x 2
1.8	9.53	10	4.3	3.9	4.7	22 x 2
1.2	3	10	3	3.9	3.6	22 x 2

Functional Pin Description

Pin No.	Pin Name	Pin Function
1	BOOT	Bootstrap for High Side Gate Driver. Connect a 10nF or greater ceramic capacitor from the BOOT pin to SW pin.
2	VIN	Voltage Supply Input. The input voltage range is from 4.5V to 23V. A suitable large capacitor must be bypassed with this pin.
3	SW	Switching Node. Connect the output LC filter between the SW pin and output load.
4, 9 (Exposed Pad)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.
5	FB	Output Voltage Feedback Input. The feedback reference voltage is 0.925V typically.
6	COMP	Compensation Node. This pin is used for compensating the regulation control loop. A series RC network is required to be connected from COMP to GND. If needed, an additional capacitor can be connected from COMP to GND.
7	EN	Enable Input. A logic high enables the converter, a logic low forces the converter into shutdown mode reducing the supply current to less than 3μA. For automatic startup, connect this pin to VIN with a 100kΩ pull up resistor.
8	SS	Soft-Start Control Input. The soft-start period can be set by connecting a capacitor from SS to GND. A 0.1μF capacitor sets the soft-start period to 15.5ms typically.

Function Block Diagram



Absolute Maximum Ratings (Note 1)

- Supply Voltage, V_{IN} -- −0.3V to 25V
- Switching Voltage, SW -- −0.3V to (V_{IN} + 0.3V)
- SW (AC) 30ns -- −5V to 30V
- BOOT Voltage -- (V_{SW} − 0.3V) to (V_{SW} + 6V)
- The Other Pins -- −0.3V to 6V
- Power Dissipation, P_D @ T_A = 25°C

  SOP-8 (Exposed Pad) -- 1.333W
- Package Thermal Resistance (Note 2)

  SOP-8 (Exposed Pad), θ_{JA} -- 75°C/W

  SOP-8 (Exposed Pad), θ_{JC} -- 15°C/W
- Junction Temperature -- 150°C
- Lead Temperature (Soldering, 10 sec.) -- 260°C
- Storage Temperature Range -- −65°C to 150°C
- ESD Susceptibility (Note 3)

  HBM (Human Body Model) -- 2kV

  MM (Machine Model) -- 200V

Recommended Operating Conditions (Note 4)

- Supply Voltage, V_{IN} -- 4.5V to 23V
- Enable Voltage, V_{EN} -- 0V to 5.5V
- Junction Temperature Range -- −40°C to 125°C
- Ambient Temperature Range -- −40°C to 85°C

Electrical Characteristics

(V_{IN} = 12V, T_A = 25°C unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Shutdown Supply Current			V_{EN} = 0V	--	0.3	3	μA
Supply Current			V_{EN} = 3V, V_{FB} = 1V	--	0.8	1.2	mA
Feedback Voltage		V_{FB}	4.5V ≤ V_{IN} ≤ 23V	0.911	0.925	0.939	V
Error Amplifier Transconductance		G_{EA}	ΔI_C = ±10μA	--	940	--	μA/V
High Side Switch On-Resistance		$R_{DS(ON)1}$		--	100	--	mΩ
Low Side Switch On-Resistance		$R_{DS(ON)2}$		--	85	--	mΩ
High Side Switch Leakage Current			V_{EN} = 0V, V_{SW} = 0V	--	0	10	μA
Upper Switch Current Limit			Min. Duty Cycle $V_{BOOT} - V_{SW}$ = 4.8V	--	5.1	--	A
Lower Switch Current Limit			From Drain to Source	--	1.5	--	A
COMP to Current Sense Transconductance		G_{CS}		--	5.4	--	A/V
Oscillation Frequency		f_{OSC1}		300	340	380	kHz
Short Circuit Oscillation Frequency		f_{OSC2}	V_{FB} = 0V	--	100	--	kHz
Maximum Duty Cycle		D_{MAX}	V_{FB} = 0.8V	--	90	--	%
Minimum On Time		t_{ON}		--	100	--	ns
EN Input Threshold Voltage	Logic-High	V_{IH}		2.7	--	--	V
	Logic-Low	V_{IL}		--	--	0.4	
Input Under Voltage Lockout Threshold		V_{UVLO}	V_{IN} Rising	3.8	4.2	4.5	V
Input Under Voltage Lockout Threshold Hysteresis		ΔV_{UVLO}		--	320	--	mV
Soft-Start Current		I_{SS}	V_{SS} = 0V	--	6	--	μA
Soft-Start Period		t_{SS}	C_{SS} = 0.1μF	--	15.5	--	ms
Thermal Shutdown		T_{SD}		--	150	--	°C

Note 1. Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

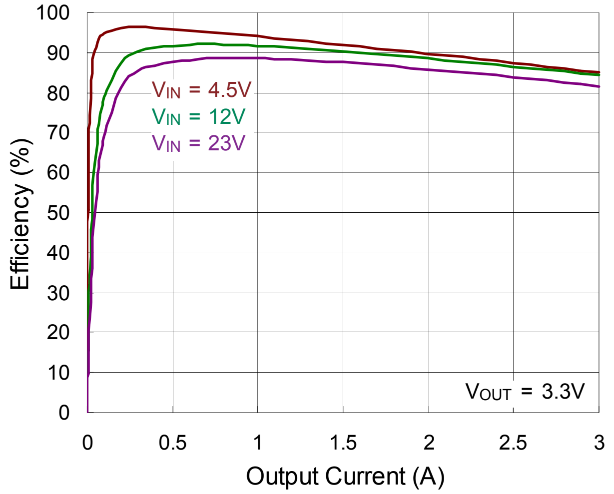
Note 2. θ_{JA} is measured at T_A = 25°C on a high effective thermal conductivity four-layer test board per JEDEC 51-7. θ_{JC} is measured at the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

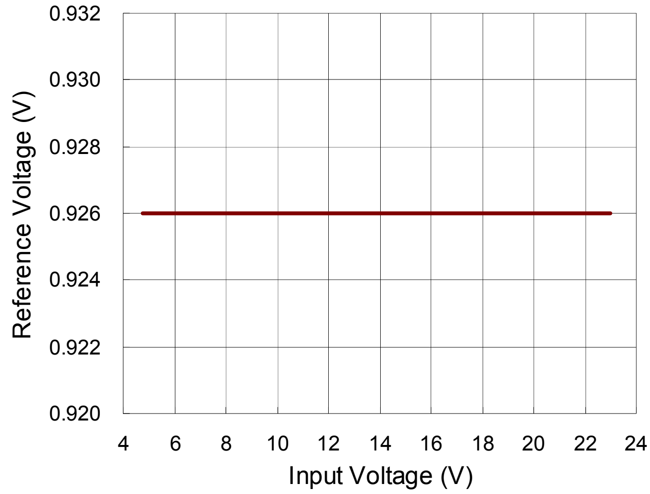
Note 4. The device is not guaranteed to function outside its operating conditions.

Typical Operating Characteristics

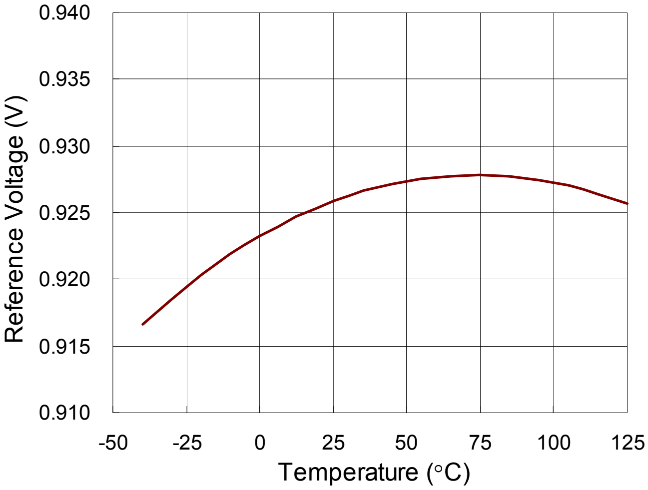
Efficiency vs. Output Current



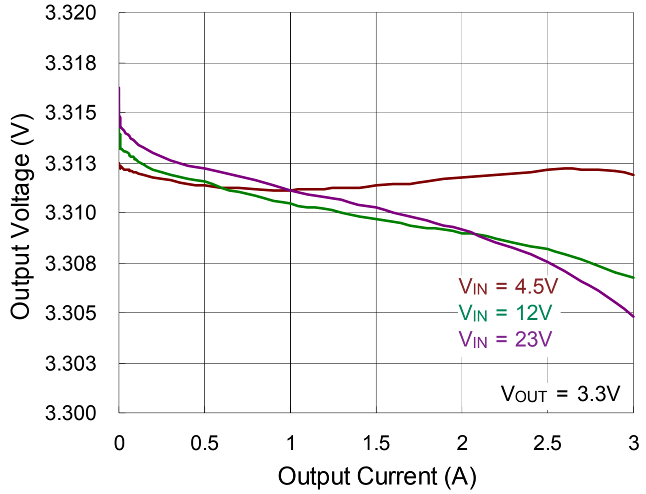
Reference Voltage vs. Input Voltage



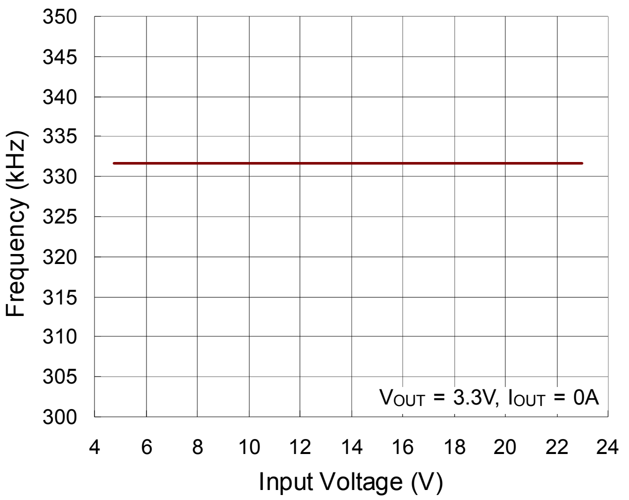
Reference Voltage vs. Temperature



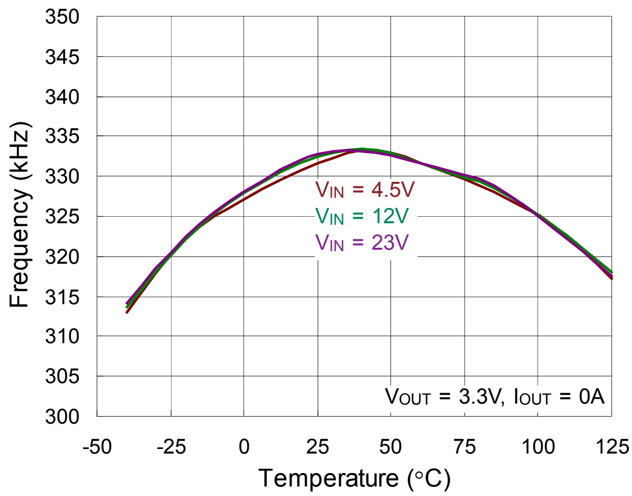
Output Voltage vs. Output Current

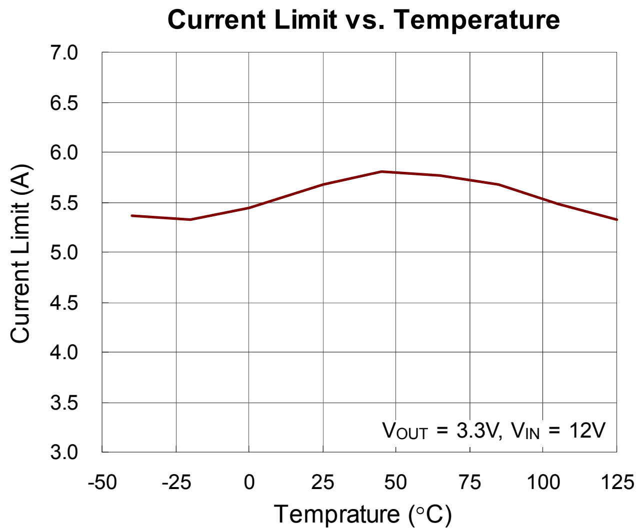


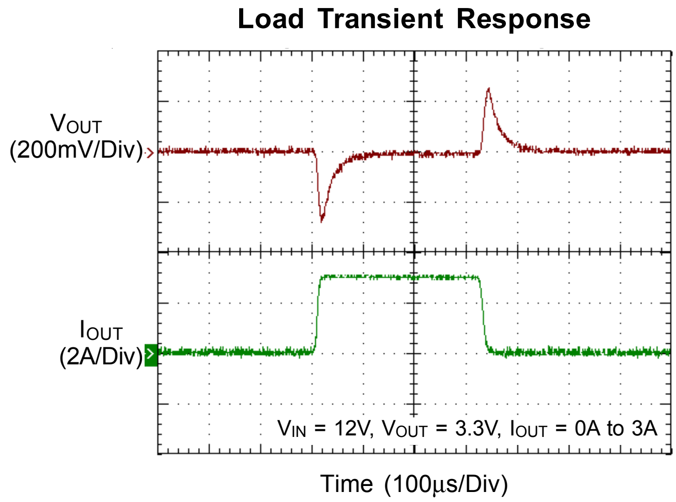
Frequency vs. Input Voltage

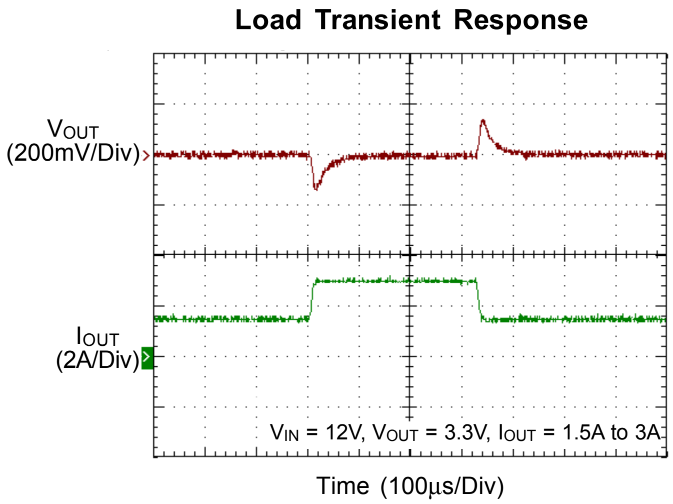


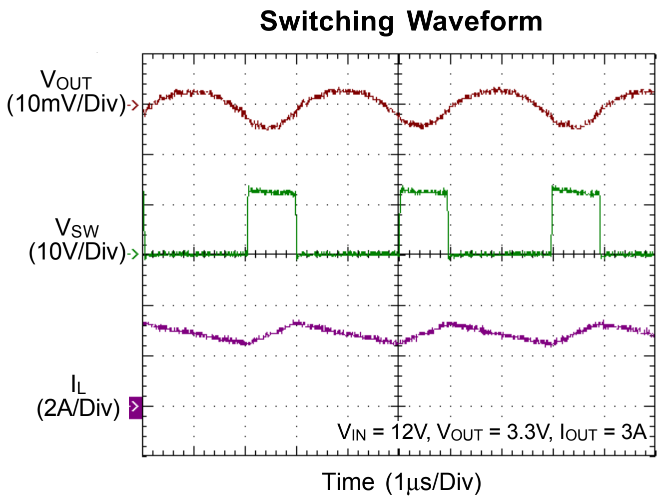
Frequency vs. Temperature

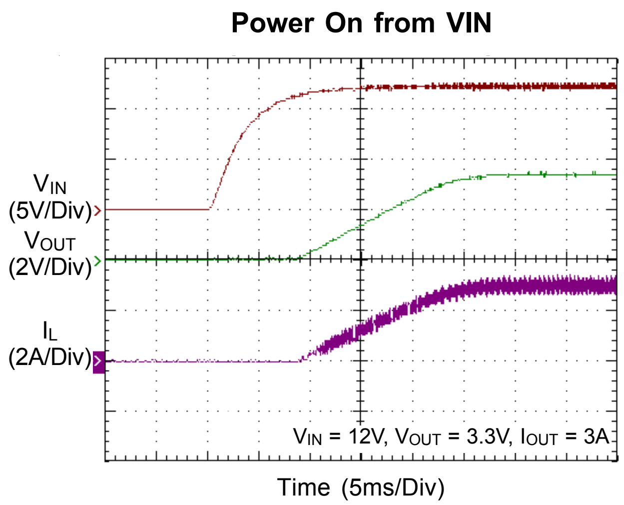


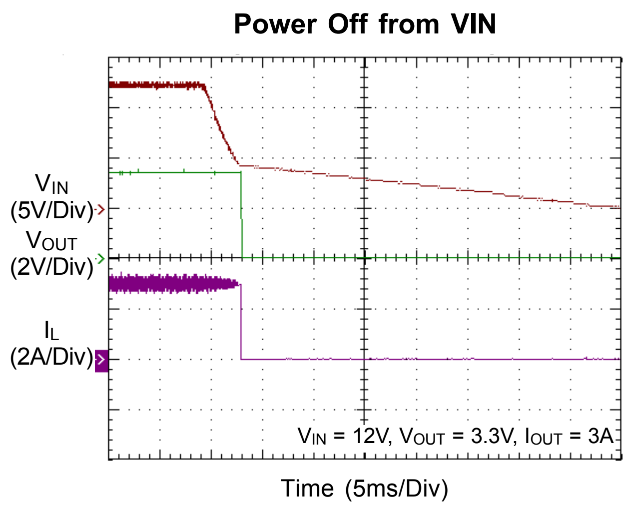

Current Limit vs. Temperature
7.0
6.5
6.0
5.5
5.0
4.5
4.0
3.5
3.0
Current Limit (A)
VOUT = 3.3V, VIN = 12V
-50
-25
0
25
50
75
100
125
Temprature (°C)


Load Transient Response
VOUT
(200mV/Div)
IOUT
(2A/Div)
VIN = 12V, VOUT = 3.3V, IOUT = 0A to 3A
Time (100μs/Div)

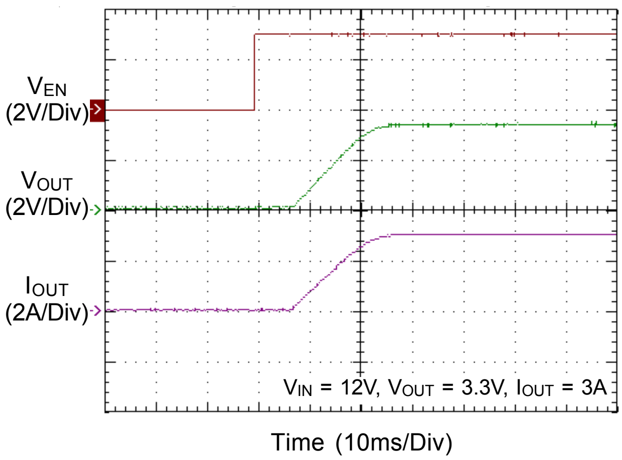

Load Transient Response
VOUT
(200mV/Div)
IOUT
(2A/Div)
VIN = 12V, VOUT = 3.3V, IOUT = 1.5A to 3A
Time (100μs/Div)


Switching Waveform
VOUT
(10mV/Div)
VSW
(10V/Div)
IL
(2A/Div)
VIN = 12V, VOUT = 3.3V, IOUT = 3A
Time (1μs/Div)

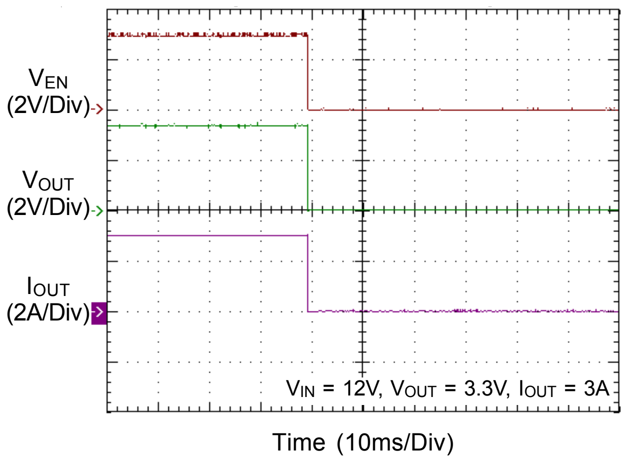

Power On from VIN
VIN
(5V/Div)
VOUT
(2V/Div)
IL
(2A/Div)
VIN = 12V, VOUT = 3.3V, IOUT = 3A
Time (5ms/Div)


Power Off from VIN
VIN
(5V/Div)
VOUT
(2V/Div)
IL
(2A/Div)
VIN = 12V, VOUT = 3.3V, IOUT = 3A
Time (5ms/Div)

Power On from EN



Power Off from EN



Application Information

The RT8290 is a synchronous high voltage buck converter that can support the input voltage range from 4.5V to 23V and the output current can be up to 3A.

Output Voltage Setting

The resistive voltage divider allows the FB pin to sense the output voltage as shown in Figure 1.

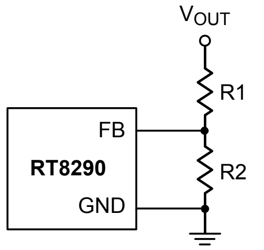


Figure 1. Output Voltage Setting

The output voltage is set by an external resistive voltage divider according to the following equation :

$$V_{OUT} = V_{FB}\left(1+\frac{R1}{R2}\right)$$

where V_{FB} is the feedback reference voltage (0.925V typ.).

External Bootstrap Diode

Connect a 10nF low ESR ceramic capacitor between the BOOT pin and SW pin. This capacitor provides the gate driver voltage for the high side MOSFET.

It is recommended to add an external bootstrap diode between an external 5V and the BOOT pin for efficiency improvement when input voltage is lower than 5.5V or duty ratio is higher than 65%. The bootstrap diode can be a low cost one such as 1N4148 or BAT54.

The external 5V can be a 5V fixed input from system or a 5V output of the RT8290. Note that the external boot voltage must be lower than 5.5V.

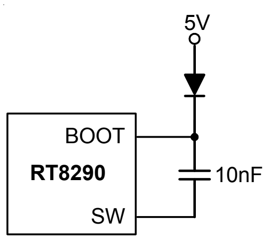


Figure 2. External Bootstrap Diode

Soft-Start

The RT8290 contains an external soft-start clamp that gradually raises the output voltage. The soft-start timing can be programmed by the external capacitor between SS pin and GND. The chip provides a 6μA charge current for the external capacitor. If a 0.1μF capacitor is used to set the soft-start, the period will be 15.5ms (typ.).

Inductor Selection

The inductor value and operating frequency determine the ripple current according to a specific input and output voltage. The ripple current ΔI_L increases with higher V_{IN} and decreases with higher inductance.

$$\Delta I_L = \left[\frac{V_{OUT}}{f \times L}\right] \times \left[1 - \frac{V_{OUT}}{V_{IN}}\right]$$

Having a lower ripple current reduces not only the ESR losses in the output capacitors but also the output voltage ripple. High frequency with small ripple current can achieve highest efficiency operation. However, it requires a large inductor to achieve this goal.

For the ripple current selection, the value of ΔI_L = 0.2375 (I_{MAX}) will be a reasonable starting point. The largest ripple current occurs at the highest V_{IN}. To guarantee that the ripple current stays below the specified maximum, the inductor value should be chosen according to the following equation :

$$L = \left[\frac{V_{OUT}}{f \times \Delta I_{L(MAX)}}\right] \times \left[1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right]$$

Inductor Core Selection

The inductor type must be selected once the value for L is known. Generally speaking, high efficiency converters can not afford the core loss found in low cost powdered iron cores. So, the more expensive ferrite or mollypermalloy cores will be a better choice.

The selected inductance rather than the core size for a fixed inductor value is the key for actual core loss. As the inductance increases, core losses decrease. Unfortunately, increase of the inductance requires more turns of wire and therefore the copper losses will increase.

Ferrite designs are preferred at high switching frequency due to the characteristics of very low core losses. So, design goals can focus on the reduction of copper loss and the saturation prevention.

Ferrite core material saturates "hard", which means that inductance collapses abruptly when the peak design current is exceeded. The previous situation results in an abrupt increase in inductor ripple current and consequent output voltage ripple.

Do not allow the core to saturate!

Different core materials and shapes will change the size/current and price/current relationship of an inductor.

Toroid or shielded pot cores in ferrite or permalloy materials are small and do not radiate energy. However, they are usually more expensive than the similar powdered iron inductors. The rule for inductor choice mainly depends on the price vs. size requirement and any radiated field/EMI requirements.

C_{IN} and C_{OUT} Selection

The input capacitance, $C_{IN,}$ is needed to filter the trapezoidal current at the source of the high side MOSFET. To prevent large ripple current, a low ESR input capacitor sized for the maximum RMS current should be used. The RMS current is given by :

$$I_{RMS} = I_{OUT(MAX)} \frac{V_{OUT}}{V_{IN}} \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief.

Choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design.

For the input capacitor, a 10µF x 2 low ESR ceramic capacitor is recommended. For the recommended capacitor, please refer to table 3 for more detail.

The selection of C_{OUT} is determined by the required ESR to minimize voltage ripple.

Moreover, the amount of bulk capacitance is also a key for C_{OUT} selection to ensure that the control loop is stable. Loop stability can be checked by viewing the load transient response as described in a later section.

The output ripple, ΔV_{OUT} , is determined by :

$$\Delta V_{OUT} \leq \Delta I_L \left[ESR + \frac{1}{8fC_{OUT}} \right]$$

The output ripple will be highest at the maximum input voltage since ΔI_L increases with input voltage. Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirement. Dry tantalum, special polymer, aluminum electrolytic and ceramic capacitors are all available in surface mount packages. Special polymer capacitors offer very low ESR value. However, it provides lower capacitance density than other types. Although Tantalum capacitors have the highest capacitance density, it is important to only use types that pass the surge test for use in switching power supplies. Aluminum electrolytic capacitors have significantly higher ESR. However, it can be used in cost-sensitive applications for ripple current rating and long term reliability considerations. Ceramic capacitors have excellent low ESR characteristics but can have a high voltage coefficient and audible piezoelectric effects. The high Q of ceramic capacitors with trace inductance can also lead to significant ringing.

Higher values, lower cost ceramic capacitors are now becoming available in smaller case sizes. Their high ripple current, high voltage rating and low ESR make them ideal for switching regulator applications. However, care must be taken when these capacitors are used at input and output. When a ceramic capacitor is used at the input and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the input, V_{IN}. At best, this ringing can couple to the output and be mistaken as loop instability. At worst, a sudden inrush of current through the long wires can potentially cause a voltage spike at V_{IN} large enough to damage the part.

Checking Transient Response

The regulator loop response can be checked by looking at the load transient response. Switching regulators take several cycles to respond to a step in load current. When a load step occurs, V_{OUT} immediately shifts by an amount equal to ΔI_{LOAD} (ESR) and C_{OUT} also begins to be charged or discharged to generate a feedback error signal for the regulator to return V_{OUT} to its steady-state value. During this recovery time, V_{OUT} can be monitored for overshoot or ringing that would indicate a stability problem.

Thermal Considerations

For continuous operation, do not exceed the maximum operation junction temperature 125°C. The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, the rate of surroundings airflow and temperature difference between junction to ambient. The maximum power dissipation can be calculated by following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum operation junction temperature, T_A is the ambient temperature and the θ_{JA} is the junction to ambient thermal resistance.

For recommended operating conditions specification, the maximum junction temperature is 125°C. The junction to ambient thermal resistance θ_{JA} is layout dependent. For SOP-8 (Exposed Pad) package, the thermal resistance θ_{JA} is 75°C/W on the standard JEDEC 51-7 four-layers thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by following formula :

$P_{D(MAX)}$ = (125°C − 25°C) / (75°C/W) = 1.333W for SOP-8 (Exposed Pad) package

The maximum power dissipation depends on operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance θ_{JA}. The derating curve in Figure 3 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

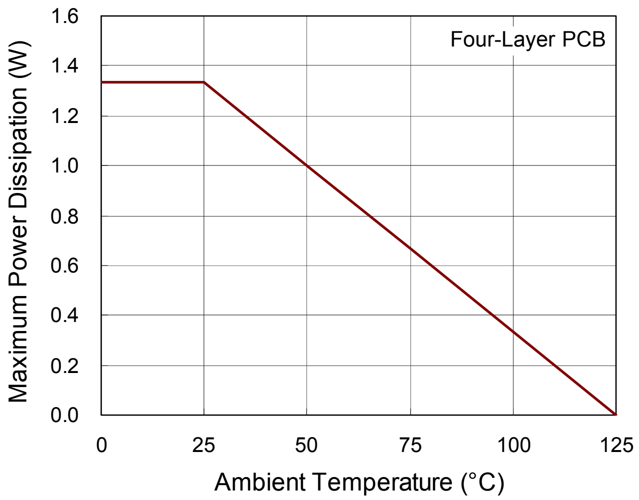


Figure 3. Derating Curve of Maximum Power Dissipation

Layout Considerations

Follow the PCB layout guidelines for optimal performance of the RT8290.

- Keep the traces of the main current paths as short and wide as possible.
- Put the input capacitor as close as possible to the device pins (VIN and GND).
- SW node is with high frequency voltage swing and should be kept in a small area. Keep sensitive components away from the SW node to prevent stray capacitive noise pick-up.
- Place the feedback components as close to the FB pin and COMP pin as possible.
- The GND pin and Exposed Pad should be connected to a strong ground plane for heat sinking and noise protection.

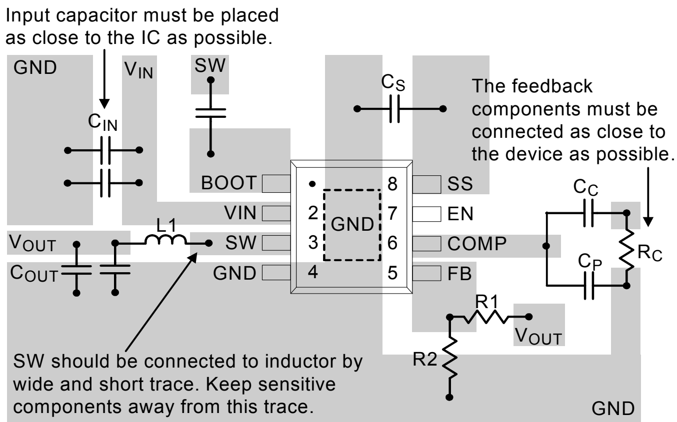


Figure 4. PCB Layout Guide

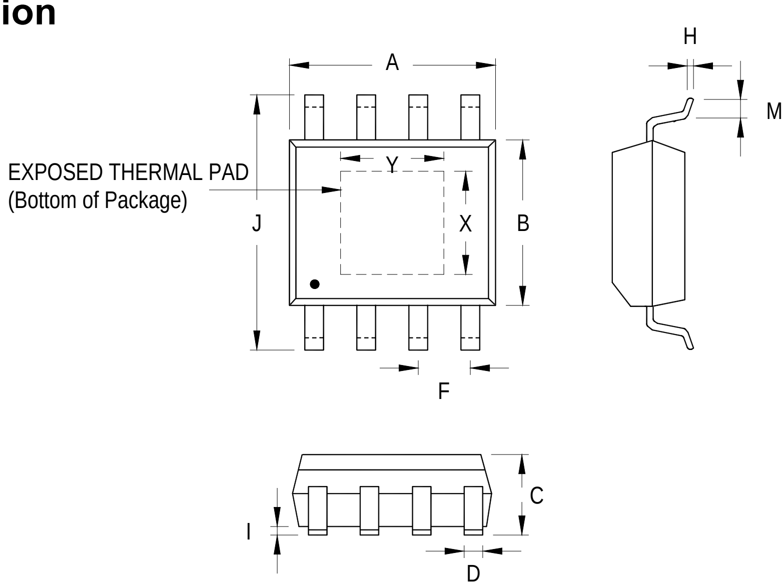
Table 2. Suggested Inductors for Typical Application Circuit

Component Supplier	Series	Dimensions (mm)
TDK	VLF10045	10 x 9.7 x 4.5
TAIYO YUDEN	NR8040	8x8x4

Table 3. Suggested Capacitors for C_{IN} and C_{OUT}

Component Supplier	Part No.	Capacitance (μF)	Case Size
MURATA	GRM31CR61E106K	10	1206
TDK	C3225X5R1E106K	10	1206
TAIYO YUDEN	TMK316BJ106ML	10	1206
MURATA	GRM31CR60J476M	47	1206
TDK	C3225X5R0J476M	47	1210
TAIYO YUDEN	EMK325BJ476MM	47	1210
MURATA	GRM32ER71C226M	22	1210
TDK	C3225X5R1C226M	22	1210

Outline Dimension



Symbol		Dimensions In Millimeters		Dimensions In Inches	
		Min	Max	Min	Max
A		4.801	5.004	0.189	0.197
B		3.810	4.000	0.150	0.157
C		1.346	1.753	0.053	0.069
D		0.330	0.510	0.013	0.020
F		1.194	1.346	0.047	0.053
H		0.170	0.254	0.007	0.010
I		0.000	0.152	0.000	0.006
J		5.791	6.200	0.228	0.244
M		0.406	1.270	0.016	0.050
Option 1	X	2.000	2.300	0.079	0.091
	Y	2.000	2.300	0.079	0.091
Option 2	X	2.100	2.500	0.083	0.098
	Y	3.000	3.500	0.118	0.138

8-Lead SOP (Exposed Pad) Plastic Package

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