Atmel AT93C56B and AT93C66B

3-wire Automotive Temperature Serial EEPROM

2K (256 x 8 or 128 x 16) and 4K (512 x 8 or 256 x 16)

DATASHEET

Features

- Medium-voltage and standard-voltage operation
  - V_{CC} = 2.5V to 5.5V
- Automotive temperature range –40°C to 125°C
- User-selectable internal organization
  - 2K: 256 x 8 or 128 x 16
  - 4K: 512 x 8 or 256 x 16
- 3-wire serial interface
- Sequential Read operation
- 2MHz clock rate
- Self-timed write cycle (5ms max)
- High reliability
  - Endurance: 1 million write cycles
  - Data retention: 100 years
- Lead-free/Halogen-free devices available
- 8-lead JEDEC SOIC and 8-lead TSSOP packages

Description

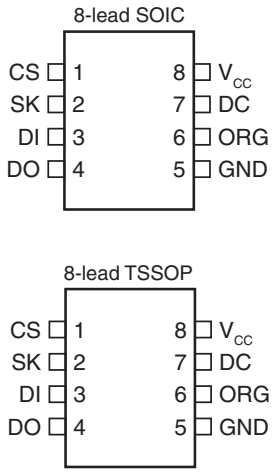
The Atmel® AT93C56B/66B provides 2048/4096 bits of Serial Electrically Erasable Programmable Read-Only Memory (EEPROM). The EEPROM is organized as 128/256 words of 16 bits each when the ORG pin is connected to V_{CC} and 256/512 words of eight bits each when it is tied to ground. The device is optimized for use in many automotive applications where low-power and low-voltage operations are essential. AT93C56B/66B is available in space-saving 8-lead JEDEC SOIC and 8-lead TSSOP packages.

AT93C56B/66B is enabled through the Chip Select (CS) pin and accessed via a 3-wire serial interface consisting of Data Input (DI), Data Output (DO), and Shift Clock (SK). Upon receiving a Read instruction at DI, the address is decoded and the data is clocked out serially on the data output pin DO. The write cycle is completely self-timed and no separate erase cycle is required before write. The write cycle is only enabled when the part is in the Erase/Write Enable state. When CS is brought high following the initiation of a write cycle, the DO pin outputs the Ready/Busy status of the part.

AT93C56B/66B operates from 2.5V to 5.5V.

Figure 1. Pin Configurations

Pin Name	Function
CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
V_{CC}	Power Supply
ORG	Internal Organization
DC	Don't Connect

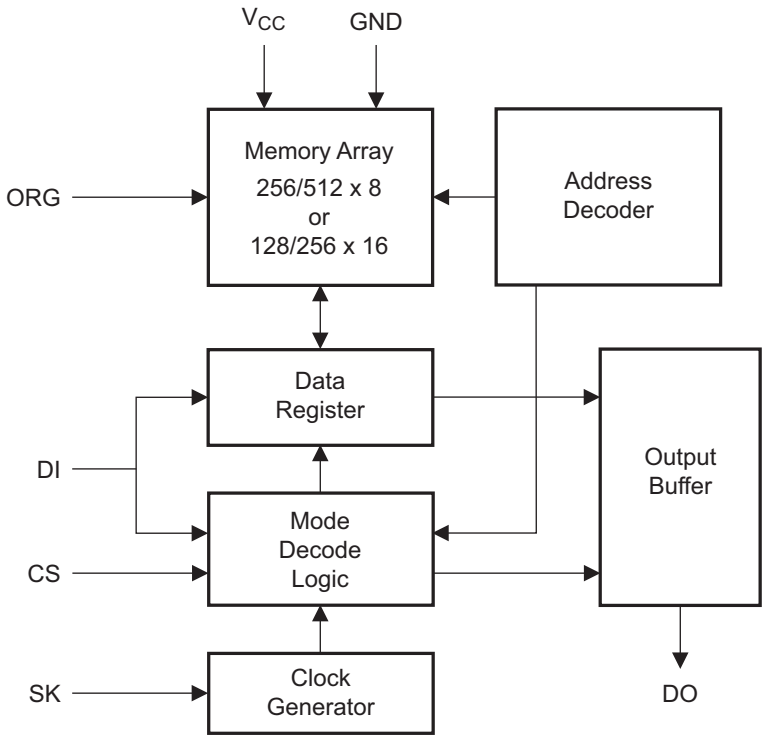


1. Absolute Maximum Ratings*

Operating Temperature	–55°C to +125°C
Storage Temperature	–65°C to +150°C
Voltage on any pin with respect to ground	–1.0V to +7.0V
Maximum Operating Voltage	6.25V
DC Output Current	5.0mA

*Notice: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

2. Block Diagram



Note: When the ORG pin is connected to V_{CC}, the “x 16” organization is selected. When it is connected to ground, the “x 8” organization is selected. If the ORG pin is left unconnected and the application does not load the input beyond the capability of the internal 1mΩ pullup, then the “x 16” organization is selected.

3. Electrical Characteristics

3.1 Pin Capacitance[1]

Applicable over recommended operating range from T_A = 25°C, f = 1.0MHz, V_{CC} = +5.0V (unless otherwise noted).

Symbol	Test Conditions	Max	Units	Conditions
C_{OUT}	Output Capacitance (DO)	5	pF	V_{OUT} = 0V
C_{IN}	Input Capacitance (CS, SK, DI)	5	pF	V_{IN} = 0V

Note: 1. This parameter is characterized and is not 100% tested.

3.2 DC Characteristics

Applicable over recommended operating range from: T_A = –40°C to +125°C,
V_{CC} = +2.5V to +5.5V (unless otherwise noted).

Symbol	Parameter	Test Condition		Min	Typ	Max	Unit
V_{CC1}	Supply Voltage			2.5		5.5	V
V_{CC2}	Supply Voltage			4.5		5.5	V
I_{CC}	Supply Current	V_{CC} = 5.0V	Read at 1.0MHz		0.5	2.0	mA
			Write at 1.0MHz		0.5	2.0	mA
I_{SB1}	Standby Current	V_{CC} = 2.5V	CS = 0V		3.0	10.0	µA
I_{SB2}	Standby Current	V_{CC} = 5.0V	CS = 0V		10.0	15.0	µA
I_{IL}	Input Leakage	V_{IN} = 0V to V_{CC}			0.1	3.0	µA
I_{OL}	Output Leakage	V_{IN} = 0V to V_{CC}			0.1	3.0	µA
V_{IL1}[1]	Input Low Voltage	2.5V ≤ V_{CC} ≤ 5.5V		–0.6		0.8	V
V_{IH1}[1]	Input High Voltage			2.0		V_{CC} + 1	
V_{OL1}	Output Low Voltage	2.5V ≤ V_{CC} ≤ 5.5V	I_{OL} = 2.1m			0.4	V
V_{OH1}	Output High Voltage		I_{OH} = –0.4mA	2.4			V

Note: 1. V_{IL} min and V_{IH} max are reference only and are not tested.

3.3 AC Characteristics

Applicable over recommended operating range from T_A = –40°C to + 125°C, V_{CC} = As Specified, CL = 1 TTL Gate and 100pF (unless otherwise noted)

Symbol	Parameter	Test Condition		Min	Typ	Max	Units
f_{SK}	SK Clock Frequency	$4.5V \le V_{CC} \le 5.5V$ $2.5V \le V_{CC} \le 5.5V$		0 0		2 1	MHz
t_{SKH}	SK High Time	$4.5V \le V_{CC} \le 5.5V$ $2.5V \le V_{CC} \le 5.5V$		250 250			ns
t_{SKL}	SK Low Time	$4.5V \le V_{CC} \le 5.5V$ $2.5V \le V_{CC} \le 5.5V$		250 250			ns
t_{CS}	Minimum CS Low Time	$4.5V \le V_{CC} \le 5.5V$ $2.5V \le V_{CC} \le 5.5V$		250 250			ns
t_{CSS}	CS Setup Time	Relative to SK	$4.5V \le V_{CC} \le 5.5V$ $2.5V \le V_{CC} \le 5.5V$	50 50			ns
t_{DIS}	DI Setup Time	Relative to SK	$4.5V \le V_{CC} \le 5.5V$ $2.5V \le V_{CC} \le 5.5V$	100 100			ns
t_{CSH}	CS Hold Time	Relative to SK		0			ns
t_{DIH}	DI Hold Time	Relative to SK	$4.5V \le V_{CC} \le 5.5V$ $2.5V \le V_{CC} \le 5.5V$	100 100			ns
t_{PD1}	Output Delay to “1”	AC Test	$4.5V \le V_{CC} \le 5.5V$ $2.5V \le V_{CC} \le 5.5V$			250 500	ns
t_{PD0}	Output Delay to “0”	AC Test	$4.5V \le V_{CC} \le 5.5V$ $2.5V \le V_{CC} \le 5.5V$			250 500	ns
t_{SV}	CS to Status Valid	AC Test	$4.5V \le V_{CC} \le 5.5V$ $2.5V \le V_{CC} \le 5.5V$			250 250	ns
t_{DF}	CS to DO in High Impedance	AC Test CS = V_{IL}	$4.5V \le V_{CC} \le 5.5V$ $2.5V \le V_{CC} \le 5.5V$			100 150	ns
t_{WP}	Write Cycle Time		$2.5V \le V_{CC} \le 5.5V$			5	ms
Endurance(1)	5.0V, 25°C			1M			Write Cycles

Note: 1. This parameter is characterized and is not 100% tested.

4. Functional Description

AT93C56B/66B is accessed via a simple and versatile three-wire serial communication interface. Device operation is controlled by seven instructions issued by the host processor. *A valid instruction starts with a rising edge of CS* and consists of a start bit (Logic 1) followed by the appropriate opcode and the desired memory address location.

Table 4-1. Instruction Set for the Atmel AT93C56B/66B

Instruction	SB	Opcode	Address		Data		Comments
			x 8	x 16	x 8	x 16	
Read	1	10	A8 – A0	A7 – A0			Reads data stored in memory, at specified address.
EWEN	1	00	11XXXXXXX	11XXXXXX			Write enable must precede all programming modes.
Erase	1	11	A8 – A0	A7 – A0			Erase memory location An – A0.
Write	1	01	A8 – A0	A7 – A0	D7 – D0	D15 – D0	Writes memory location An – A0.
ERAL	1	00	10XXXXXXX	10XXXXXX			Erases all memory locations. Valid only at V_{CC} = 4.5V to 5.5V.
WRAL	1	00	01XXXXXXX	01XXXXXX	D7 – D0	D15 – D0	Writes all memory locations. Valid only at V_{CC} = 5.0V ±10% and Disable Register cleared.
EWDS	1	00	00XXXXXXX	00XXXXXX			Disables all programming instructions.

Note: The Xs in the address field represent *don't care* values and must be clocked.

Read: The Read instruction contains the address code for the memory location to be read. After the instruction and address are decoded, data from the selected memory location is available at the serial output pin DO. Output data changes are synchronized with the rising edges of serial clock SK. It should be noted that a dummy bit (Logic 0) precedes the 8- or 16-bit data output string. AT93C56B/66B supports sequential read operations. The device will automatically increment the internal address pointer and clock out the next memory location as long as Chip Select (CS) is held high. In this case, the dummy bit (Logic 0) will not be clocked out between memory locations, thus allowing for a continuous stream of data to be read.

Erase/Write Enable (EWEN): To assure data integrity, the part automatically goes into the Erase/Write Disable (EWDS) state when power is first applied. An Erase/Write Enable (EWEN) instruction must be executed first before any programming instructions can be carried out. Please note that once in the EWEN state, programming remains enabled until an EWDS instruction is executed or V_{CC} power is removed from the part.

Erase: The Erase instruction programs all bits in the specified memory location to the Logical 1 state. The self-timed erase cycle starts once the Erase instruction and address are decoded. The DO pin outputs the Ready/Busy status of the part if CS is brought high after being kept low for a minimum of 250ns (t_{CS}). A Logic 1 at pin DO indicates that the selected memory location has been erased, and the part is ready for another instruction.

Write: The Write instruction contains the 8 or 16 bits of data to be written into the specified memory location. The self-timed programming cycle, t_{WP}, starts after the last bit of data is received at serial data input pin DI. The DO pin outputs the Ready/Busy status of the part if CS is brought high after being kept low for a minimum of 250ns (t_{CS}). A Logic 0 at DO indicates that programming is still in progress. A Logic 1 indicates that the memory location at the specified address has been written with the data pattern contained in the instruction and the part is ready for further instructions. *A Ready/Busy status cannot be obtained if the CS is brought high after the end of the self-timed programming cycle, t_{WP}.*

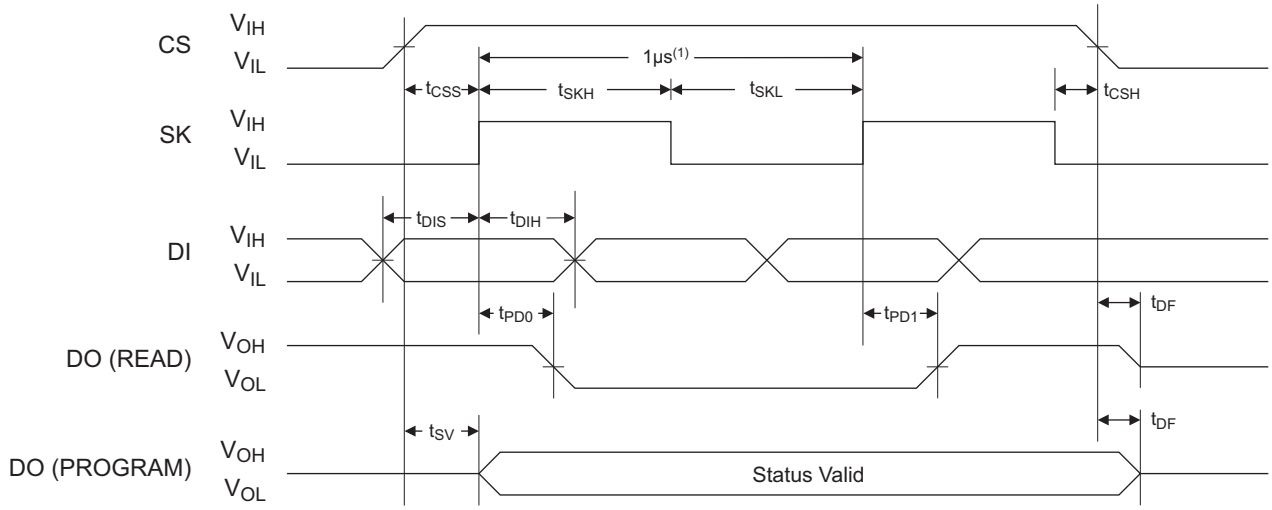
Erase All (ERAL): The Erase All (ERAL) instruction programs every bit in the memory array to the Logic 1 state and is primarily used for testing purposes. The DO pin outputs the ready/busy status of the part if CS is brought high after being kept low for a minimum of 250ns (t_{CS}). The ERAL instruction is valid only at V_{CC} = 5.0V ± 10%.

Write All (WRAL): The Write All (WRAL) instruction programs all memory locations with the data patterns specified in the instruction. The DO pin outputs the Ready/Busy status of the part if CS is brought high after being kept low for a minimum of 250ns (t_{CS}). The WRAL instruction is valid only at V_{CC} = 5.0V ± 10%.

Erase/Write Disable (EWDS): To protect against accidental data disturb, the Erase/Write Disable (EWDS) instruction disables all programming modes and should be executed after all programming operations. The operation of the Read instruction is independent of both the EWEN and EWDS instructions and can be executed at any time.

5. Timing Diagrams

Figure 5-1. Synchronous Data Timing



Note: This is the minimum SK period.

Table 5-1. Organization Key for Timing Diagrams

I/O	Atmel AT93C56B (2K)		Atmel AT93C66B (4K)	
	x 8	x 16	x 8	x 16
AN	A8(1)	A7(2)	A8	A7
DN	D7	D15	D7	D15

Notes: 1. A8 is a *don't care* value, but the extra clock is required.
2. A7 is a *don't care* value, but the extra clock is required.

Figure 5-2. Read Timing

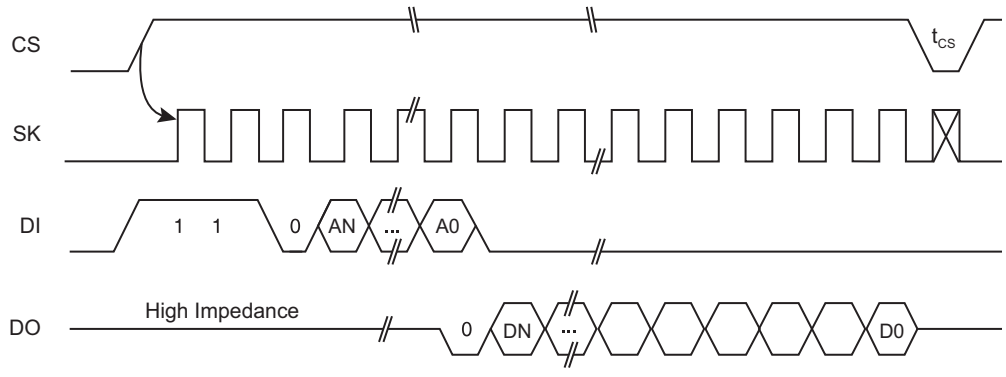


Figure 5-3. EWEN Timing

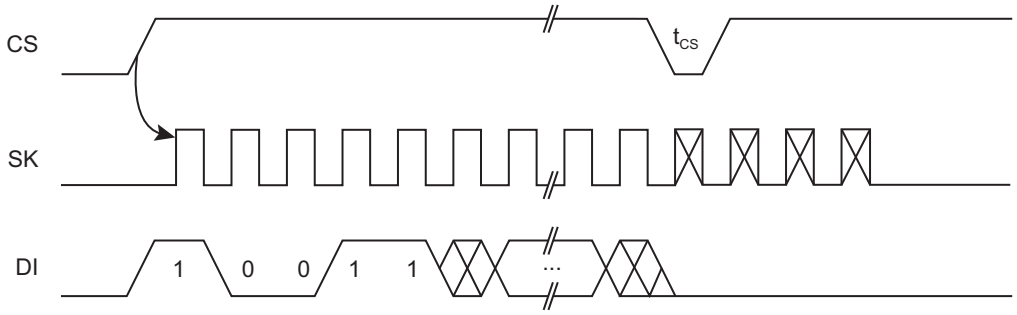


Figure 5-4. EWDS Timing

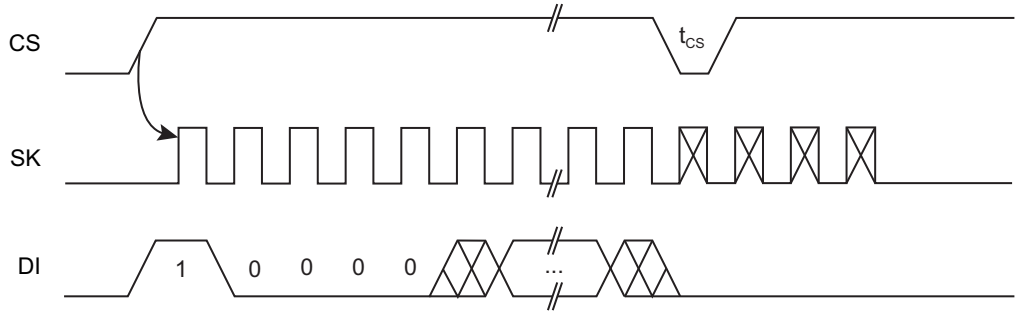


Figure 5-5. Write Timing

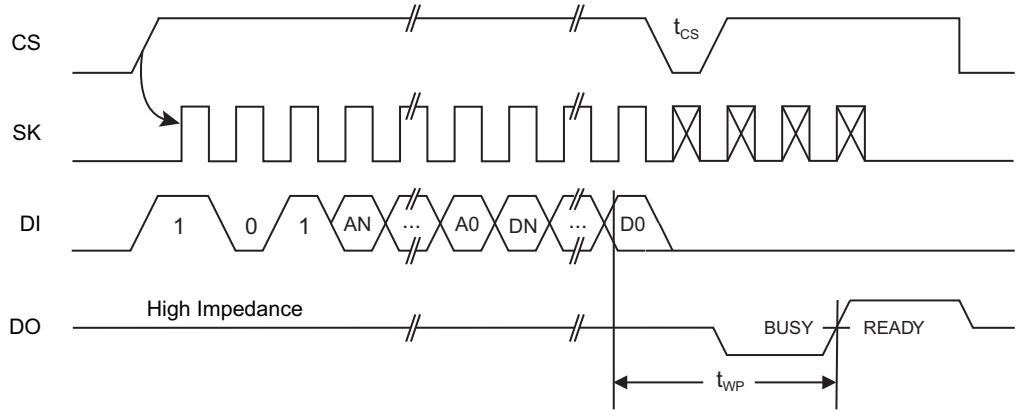
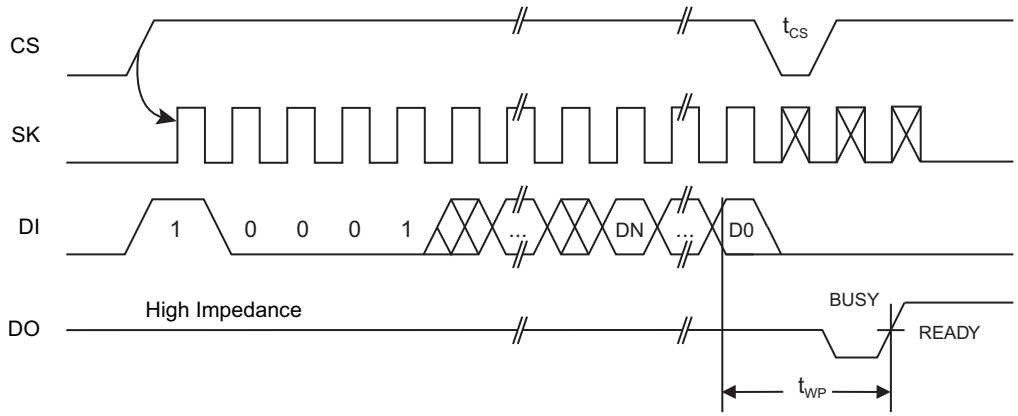


Figure 5-6. WRAL Timing



Note: 1. Valid only at V_{CC} = 4.5V to 5.5V

Figure 5-7. Erase Timing

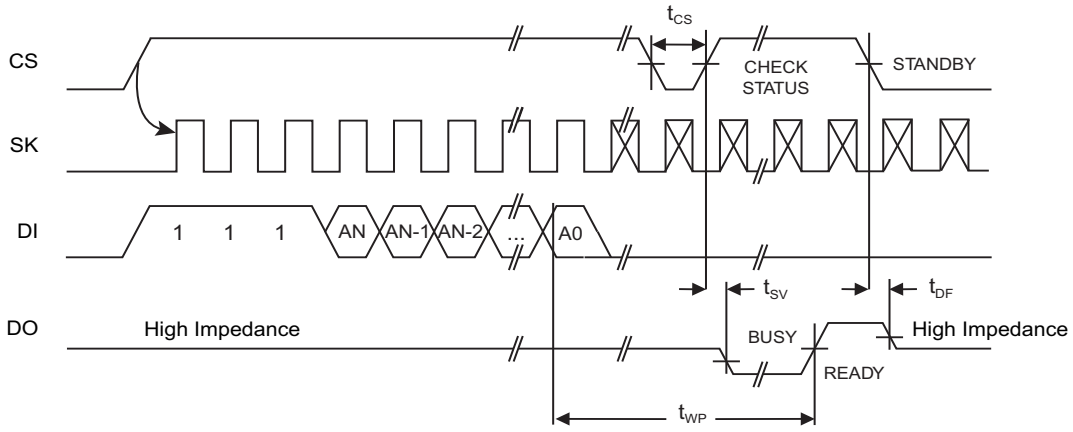
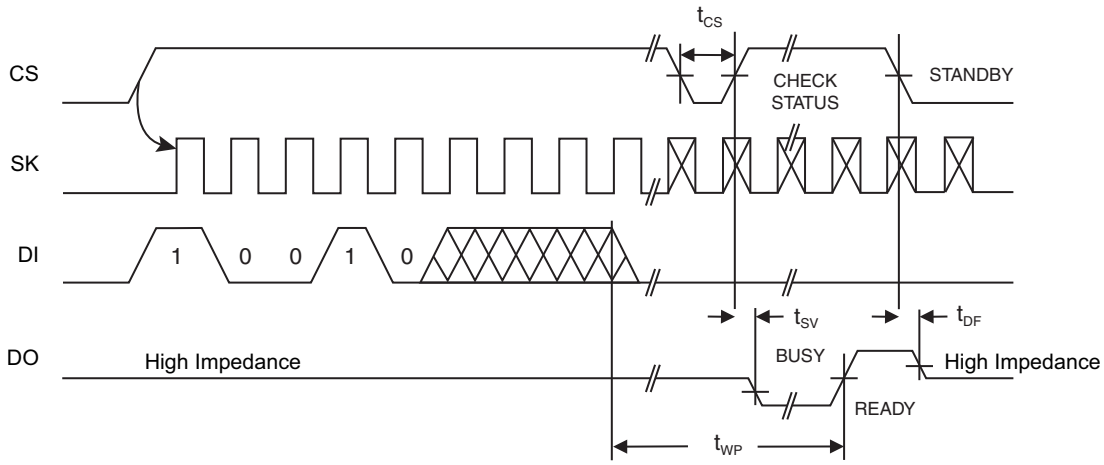


Figure 5-8. ERAL Timing



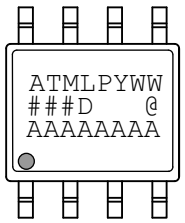
Note: 1. Valid only at V_{CC} = 4.5V to 5.5V.

5.1 Power Recommendation

The device internal POR (Power-On Reset) threshold is just below the minimum device operating voltage. Power shall rise monotonically from 0.0Vdc to full V_{CC} in less than 1ms. Hold at full V_{CC} for at least 100µs before the first operation. Power shall drop from full V_{CC} to 0.0Vdc in less than 1ms. Power dropping to a non-zero level and then slowly going to zero is *not* recommended. Power shall remain off (0.0Vdc) for 0.5s minimum. Please consult Atmel if your power conditions do not meet the above recommendations.

6. Product Markings

AT93C56B and AT93C66B: Package Marking Information

8-lead SOIC	8-lead TSSOP
	

Note 1: ● designates pin 1

Note 2: Package drawings are not to scale

Catalog Number Truncation			
AT93C56B		Truncation Code ###: 56B	
AT93C66B		Truncation Code ###: 66B	
Date Codes			**Voltages**
Y = Year	M = Month	WW = Work Week of Assembly	D: 2.5V min
2: 2012 6: 2016 3: 2013 7: 2017 4: 2014 8: 2018 5: 2015 9: 2019	A: January B: February ... L: December	02: Week 2 04: Week 4 ... 52: Week 52	
Country of Assembly	**Lot Number**		**Grade/Lead Finish Material**
@ = Country of Assembly	AAA...A = Atmel Wafer Lot Number		P: Automotive/NiPdAu
Trace Code			**Atmel Truncation**
XX = Trace Code (Atmel Lot Numbers Correspond to Code) Example: AA, AB.... YZ, ZZ			AT: Atmel ATM: Atmel ATML: Atmel

3/15/12

Atmel Package Mark Contact: DL-CSO-Assy_eng@atmel.com	TITLE	DRAWING NO.	REV.
	93C56-66BAM, AT93C56B and AT93C66B Automotive Package Marking Information	93C56-66BAM	C

7. Ordering Code Information

7.1 Atmel AT93C56B Ordering Information

Atmel Ordering Code	Package	Voltage	Operation Range
AT93C56B-SSPD	8S1	2.5V to 5.5V	Lead-free/Halogen-free Automotive Temperature (–40°C to 125°C)
AT93C56B-SSPD-T[1]			
AT93C56B-XPD	8X		
AT93C56B-XPD-T[1]			

Note: 1. Tape and reel delivery:
- SOIC 4k/reel
- TSSOP 5k/reel

Package Type	
8S1	8-lead, 0.150" wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
8X	8-lead, 4.4mm body, Plastic Thin Shrink Small Outline (TSSOP)

7.2 Atmel AT93C66B Ordering Information

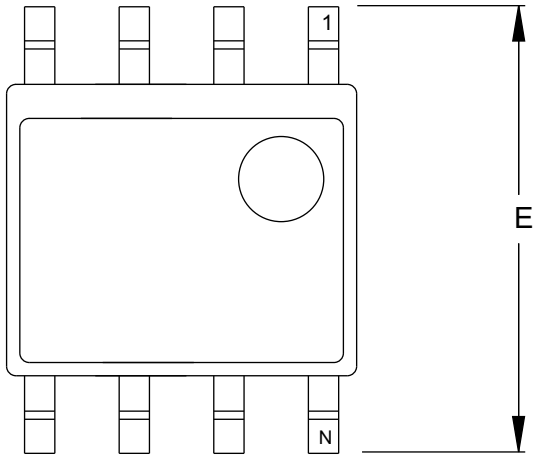
Atmel Ordering Code	Package	Voltage	Operation Range
AT93C66B-SSPD	8S1	2.5V to 5.5V	Lead-free/Halogen-free Automotive Temperature (−40°C to 125°C)
AT93C66B-SSPD-T[1]			
AT93C66B-XPD	8X		
AT93C66B-XPD-T[1]			

Note: 1. Tape and reel delivery:
- SOIC 4k/reel
- TSSOP 5k/reel

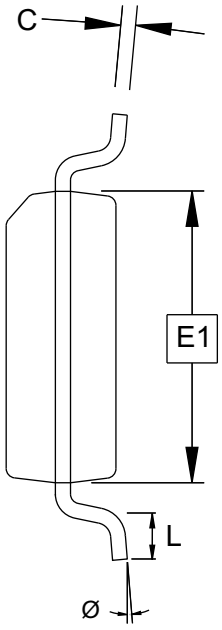
Package Type	
8S1	8-lead, 0.150" wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
8X	8-lead, 4.4mm body, Plastic Thin Shrink Small Outline (TSSOP)

8. Packaging Information

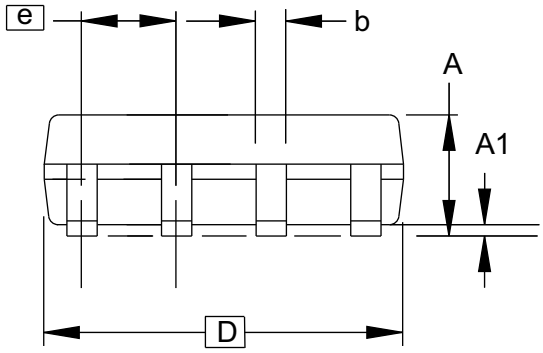
8.1 8S1 — 8-lead JEDEC SOIC



TOP VIEW



END VIEW



SIDE VIEW

Notes: This drawing is for general information only.
Refer to JEDEC Drawing MS-012, Variation AA
for proper dimensions, tolerances, datums, etc.

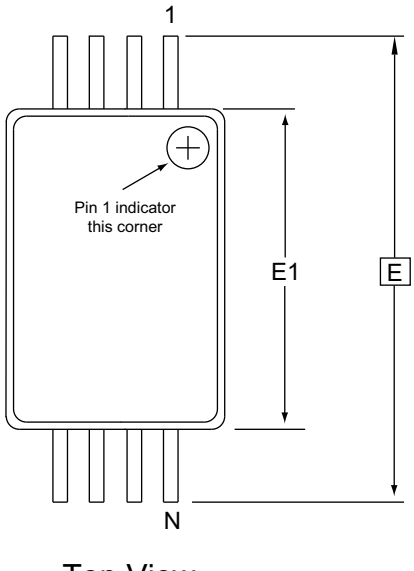
COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	1.35	–	1.75	
A1	0.10	–	0.25	
b	0.31	–	0.51	
C	0.17	–	0.25	
D	4.80	–	5.05	
E1	3.81	–	3.99	
E	5.79	–	6.20	
e	1.27 BSC			
L	0.40	–	1.27	
Ø	0°	–	8°	

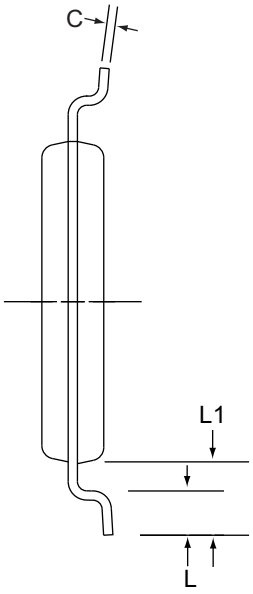
6/22/11

Atmel Package Drawing Contact: packagedrawings@atmel.com	**TITLE** 8S1, 8-lead (0.150” Wide Body), Plastic Gull Wing Small Outline (JEDEC SOIC)	**GPC** SWB	**DRAWING NO.** 8S1	**REV.** G

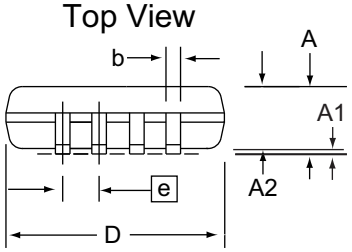
8.2 8X — 8-lead TSSOP



Top View



End View



Side View

Notes:
1. This drawing is for general information only. Refer to JEDEC Drawing MO-153, Variation AA, for proper dimensions, tolerances, datums, etc.
2. Dimension D does not include mold Flash, protrusions or gate burrs. Mold Flash, protrusions and gate burrs shall not exceed 0.15mm (0.006in) per side.
3. Dimension E1 does not include inter-lead Flash or protrusions. Inter-lead Flash and protrusions shall not exceed 0.25mm (0.010in) per side.
4. Dimension b does not include Dambar protrusion. Allowable Dambar protrusion shall be 0.08mm total in excess of the b dimension at maximum material condition. Dambar cannot be located on the lower radius of the foot. Minimum space between protrusion and adjacent lead is 0.07mm.
5. Dimension D and E1 to be determined at Datum Plane H.

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	-	-	1.20	
A1	0.05	-	0.15	
A2	0.80	1.00	1.05	
D	2.90	3.00	3.10	2, 5
E		6.40 BSC		
E1	4.30	4.40	4.50	3, 5
b	0.19	–	0.30	4
e		0.65 BSC		
L	0.45	0.60	0.75	
L1		1.00 REF		
C		0.09	-	0.20

6/22/11

Atmel Package Drawing Contact: packagedrawings@atmel.com	**TITLE** 8X, 8-lead 4.4mm Body, Plastic Thin Shrink Small Outline Package (TSSOP)	**GPC** TNR	**DRAWING NO.** 8X	**REV.** D

9. Revision History

Doc. Rev.	Date	Comments
8811B	08/2012	Remove preliminary status. Update Atmel logos and disclaimer/copy page.
8811A	06/2012	Initial document release

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