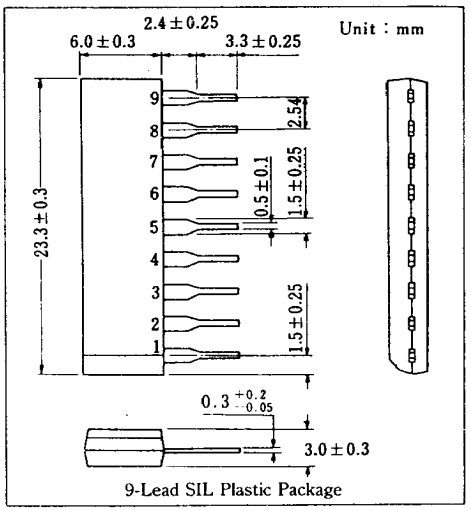
AN5791

Phase Shift Circuit for CRT Displays

■ Qutline

The AN5791 is an integrated circuit designed for phase shift circuit for CRT display.



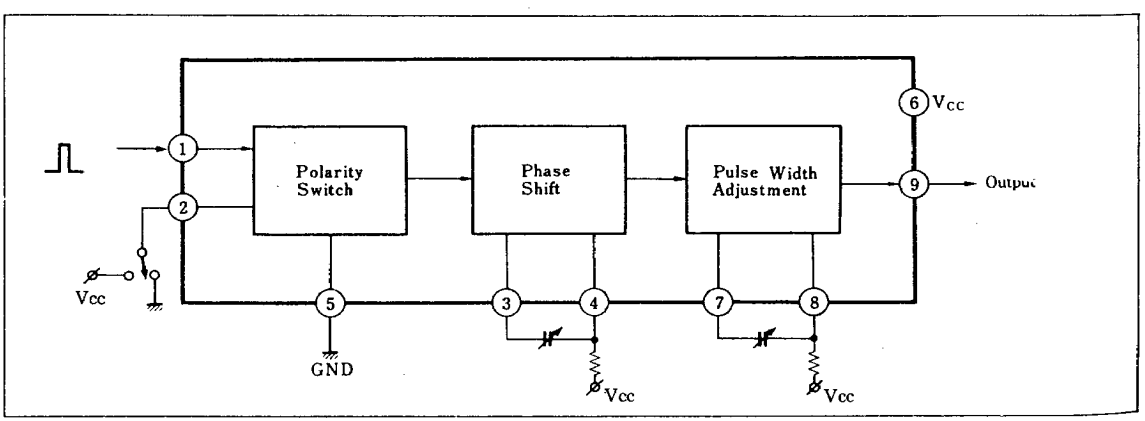
■ Features

- Processing for both negative and positive sync. signals
- Wide range of possible phase shift(1 μ s ~40 μ s)
- Possible output pulse width 2 μ s~40 μ s

■ Pin

Pin No.	Pin Name	Pin No.	Pin Name
1	H. Sync. Input	6	Vcc
2	Polarity Switch	7	Trigger for Pulse Width
3	Trigger for Phase Shift	8	Pulse Width Adj.
4	Phase Shift Adj.	9	Output
5	GND	—	—

■ Block Diagram



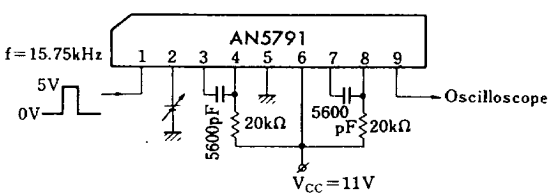
■ Absolute Maximum Ratings(Ta=25℃)

Item		Symbol	Rating	Unit
Supply Voltage		V_{CC}	13.2	V
Power Dissipation		P_D	640	mW
Temperature	Operating Ambient Temperature	T_{opr}	−20～+70	℃
	Storage Temperature	T_{stg}	−40～+150	℃

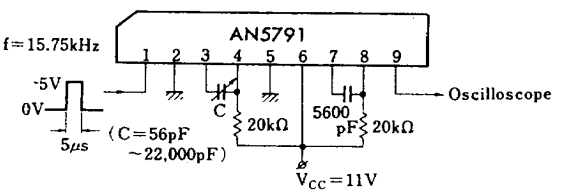
■ Electrical Characteristics(Ta=25℃)

Item	Symbol	Test Circuit	Condition	min.	typ.	max.	Unit
Circuit Current	I_6		V_{CC}=11V	18	25	32	mA
Circuit Voltage(1)	V_{3-5}		V_{CC}=11V	1.3	1.6	1.9	V
Circuit Voltage(2)	V_{7-5}		V_{CC}=11V	1.3	1.6	1.9	V
Polarity Changeover Voltage(1)	V_{2-5}	1	Positive Polarity Signal Input	0		0.4	V
Polarity Changeover Voltage(2)	V_{2-5}	1	Negative Polarity Signal Input	2.5		5.5	V
Phase Shift Time	$t_{(1)}$	2	V_{CC}=11V	4.5	5.0	5.5	μs
Enable Pulse Shift Time	$t_{(2)}$	2	V_{CC}=11V	1		40	μs
Change with Supply Voltage for Phase Modulation Time	$\Delta t_{(1)}/V_{CC}$	3	V_{CC}=9.9V～12.1V			5	%
Change with Ambient Temperature for Phase Modulation Time	$\Delta t_{(1)}/Ta$	3	V_{CC}=11V, Ta=−20℃～60℃			5	%
Output Pulse Width	$\tau_{(HD1)}$	4	V_{CC}=11V	4.4	4.9	5.4	μs
Enable Output Pulse Width	$\tau_{(HD2)}$	4	V_{CC}=11V	2		40	μs
Change with Supply Voltage for Output Pulse Width	$\Delta\tau_{(HD1)}/V_{CC}$	3	V_{CC}=9.9V～12.1V			5	%
Change with Ambient Temperature for Output Pulse Width	$\Delta\tau_{(HD1)}/Ta$	3	V_{CC}=11V, Ta=−20℃～60℃			5	%

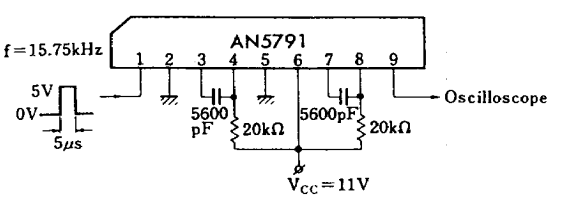
Test Circuit 1 (V_{2-5})



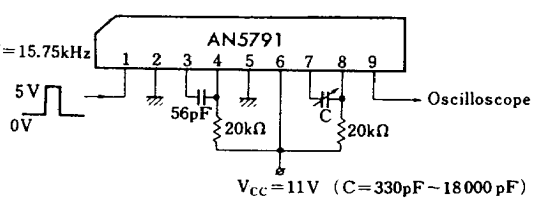
Test Circuit 2 ($t_{(1)}$, $t_{(2)}$)



Test Circuit 3 ($\Delta t_{(1)}/V_{CC}$, $\Delta t_{(1)}/Ta$, $\Delta\tau_{(HD1)}/V_{CC}$, $\Delta\tau_{(HD1)}/Ta$)



Test Circuit 4 ($\tau_{(HD1)}$, $\tau_{(HD2)}$)



■ Application Circuit