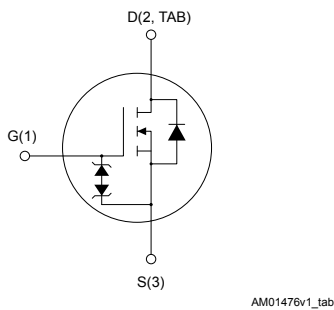
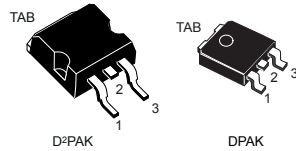




## N-channel 600 V, 1.06 $\Omega$ typ., 4.5 A MDmesh M2 Power MOSFET in a D<sup>2</sup>PAK and DPAK packages



### Features

| Order code | $V_{DS}$ | $R_{DS(on)}$ max. | $I_D$ |
|------------|----------|-------------------|-------|
| STB6N60M2  | 600 V    | 1.2 $\Omega$      | 4.5 A |
| STD6N60M2  |          |                   |       |

- Extremely low gate charge
- Excellent output capacitance ( $C_{oss}$ ) profile
- 100% avalanche tested
- Zener-protected

### Applications

- Switching applications

### Description

These devices are N-channel Power MOSFETs developed using the MDmesh M2 technology. Thanks to their strip layout and improved vertical structure, these devices exhibit low on-resistance and optimized switching characteristics, rendering them suitable for the most demanding high-efficiency converters.



#### Product status links

[STB6N60M2](#)

[STD6N60M2](#)

#### Product summary

| Order code | STB6N60M2          |
|------------|--------------------|
| Marking    | 6N60M2             |
| Package    | D <sup>2</sup> PAK |
| Packing    | Tape and reel      |
| Order code | STD6N60M2          |
| Marking    | 6N60M2             |
| Package    | DPAK               |
| Packing    | Tape and reel      |

# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

| Symbol         | Parameter                                                         | Value      | Unit               |
|----------------|-------------------------------------------------------------------|------------|--------------------|
| $V_{DS}$       | Drain-source voltage                                              | 600        | V                  |
| $V_{GS}$       | Gate-source voltage                                               | $\pm 25$   | V                  |
| $I_D$          | Drain current (continuous) at $T_C = 25\text{ }^{\circ}\text{C}$  | 4.5        | A                  |
| $I_D$          | Drain current (continuous) at $T_C = 100\text{ }^{\circ}\text{C}$ | 2.9        | A                  |
| $I_{DM}^{(1)}$ | Drain current (pulsed)                                            | 18         | A                  |
| $P_{TOT}$      | Total power dissipation at $T_C = 25\text{ }^{\circ}\text{C}$     | 60         | W                  |
| $dv/dt^{(2)}$  | Peak diode recovery voltage slope                                 | 15         | V/ns               |
| $dv/dt^{(3)}$  | MOSFET $dv/dt$ ruggedness                                         | 50         | V/ns               |
| $T_{stg}$      | Storage temperature range                                         | -55 to 150 | $^{\circ}\text{C}$ |
| $T_J$          | Operating junction temperature range                              |            | $^{\circ}\text{C}$ |

1. Pulse width limited by safe operating area.
2.  $I_{SD} \leq 4.5\text{ A}$ ,  $di/dt \leq 400\text{ A}/\mu\text{s}$ ,  $V_{DS}(\text{peak}) < V_{(BR)DSS}$ ,  $V_{DD} = 400\text{ V}$ .
3.  $V_{DD} = 480\text{ V}$ .

**Table 2. Thermal data**

| Symbol     | Parameter                               | Value              |      | Unit                        |
|------------|-----------------------------------------|--------------------|------|-----------------------------|
|            |                                         | D <sup>2</sup> PAK | DPAK |                             |
| $R_{thJC}$ | Thermal resistance, junction-to-case    | 2.08               |      | $^{\circ}\text{C}/\text{W}$ |
| $R_{thJA}$ | Thermal resistance, junction-to-ambient | 30 <sup>(1)</sup>  | 50   | $^{\circ}\text{C}/\text{W}$ |

1. When mounted on a standard 1 inch<sup>2</sup> area of FR-4 PCB with 2-oz copper.

**Table 3. Avalanche characteristics**

| Symbol   | Parameter                                                                                                              | Value | Unit |
|----------|------------------------------------------------------------------------------------------------------------------------|-------|------|
| $I_{AR}$ | Avalanche current, repetitive or not-repetitive (pulse width limited by $T_J$ max.)                                    | 1     | A    |
| $E_{AS}$ | Single pulse avalanche energy (starting $T_J = 25\text{ }^{\circ}\text{C}$ , $I_D = I_{AR}$ , $V_{DD} = 50\text{ V}$ ) | 86    | mJ   |

## 2 Electrical characteristics

( $T_C = 25\text{ }^{\circ}\text{C}$  unless otherwise specified)

**Table 4. On/off states**

| Symbol        | Parameter                         | Test conditions                                                                             | Min. | Typ. | Max.     | Unit          |
|---------------|-----------------------------------|---------------------------------------------------------------------------------------------|------|------|----------|---------------|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage    | $I_D = 1\text{ mA}$ , $V_{GS} = 0\text{ V}$                                                 | 600  | -    | -        | V             |
| $I_{DSS}$     | Zero gate voltage drain current   | $V_{GS} = 0\text{ V}$ , $V_{DS} = 600\text{ V}$                                             | -    | -    | 1        | $\mu\text{A}$ |
|               |                                   | $V_{GS} = 0\text{ V}$ , $V_{DS} = 600\text{ V}$ , $T_C = 125\text{ }^{\circ}\text{C}^{(1)}$ | -    | -    | 100      | $\mu\text{A}$ |
| $I_{GSS}$     | Gate body leakage current         | $V_{DS} = 0\text{ V}$ , $V_{GS} = \pm 25\text{ V}$                                          | -    | -    | $\pm 10$ | $\mu\text{A}$ |
| $V_{GS(th)}$  | Gate threshold voltage            | $V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$                                          | 2    | 3    | 4        | V             |
| $R_{DS(on)}$  | Static drain-source on-resistance | $V_{GS} = 10\text{ V}$ , $I_D = 2.25\text{ A}$                                              | -    | 1.06 | 1.2      | $\Omega$      |

1. Specified by design, not tested in production.

**Table 5. Dynamic**

| Symbol                     | Parameter                           | Test conditions                                                                                                                                   | Min. | Typ. | Max. | Unit     |
|----------------------------|-------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------|------|------|------|----------|
| $C_{iss}$                  | Input capacitance                   | $V_{DS} = 100\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0\text{ V}$                                                                              | -    | 232  | -    | pF       |
| $C_{oss}$                  | Output capacitance                  |                                                                                                                                                   | -    | 14   | -    | pF       |
| $C_{rss}$                  | Reverse transfer capacitance        |                                                                                                                                                   | -    | 0.7  | -    | pF       |
| $C_{oss\text{ eq.}}^{(1)}$ | Equivalent capacitance time related | $V_{DS} = 0\text{ to }480\text{ V}$ , $V_{GS} = 0\text{ V}$                                                                                       | -    | 71   | -    | pF       |
| $Q_g$                      | Total gate charge                   | $V_{DD} = 480\text{ V}$ , $I_D = 4.5\text{ A}$ , $V_{GS} = 0\text{ to }10\text{ V}$<br>(see the Figure 15. Test circuit for gate charge behavior) | -    | 8.2  | -    | nC       |
| $Q_{gs}$                   | Gate-source charge                  |                                                                                                                                                   | -    | 1.7  | -    | nC       |
| $Q_{gd}$                   | Gate-drain charge                   |                                                                                                                                                   | -    | 4.2  | -    | nC       |
| $R_g$                      | Intrinsic gate resistance           | $f = 1\text{ MHz}$ , $I_D = 0\text{ A}$                                                                                                           | -    | 6.5  | -    | $\Omega$ |

1.  $C_{oss\text{ eq.}}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$ .

**Table 6. Switching times**

| Symbol       | Parameter           | Test conditions                                                                                                | Min. | Typ. | Max. | Unit |
|--------------|---------------------|----------------------------------------------------------------------------------------------------------------|------|------|------|------|
| $t_{d(on)}$  | Turn-on delay time  | $V_{DD} = 300\text{ V}$ , $I_D = 1.65\text{ A}$ ,<br>$R_G = 4.7\text{ }\Omega$ , $V_{GS} = 10\text{ V}$        | -    | 9.5  | -    | ns   |
| $t_r$        | Rise time           |                                                                                                                | -    | 7.4  | -    | ns   |
| $t_{d(off)}$ | Turn-off delay time | (see the Figure 14. Test circuit for resistive load switching times and<br>Figure 19. Switching time waveform) | -    | 24   | -    | ns   |
| $t_f$        | Fall time           |                                                                                                                | -    | 22.5 | -    | ns   |

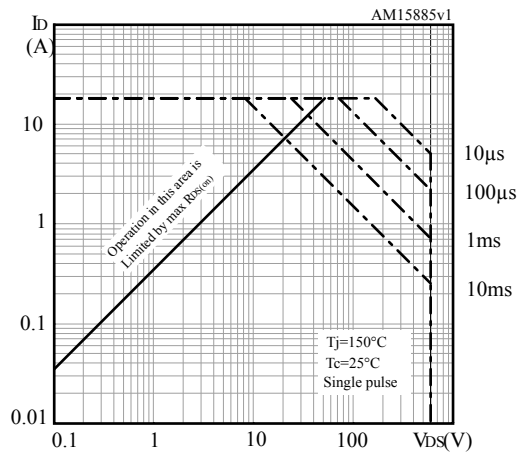
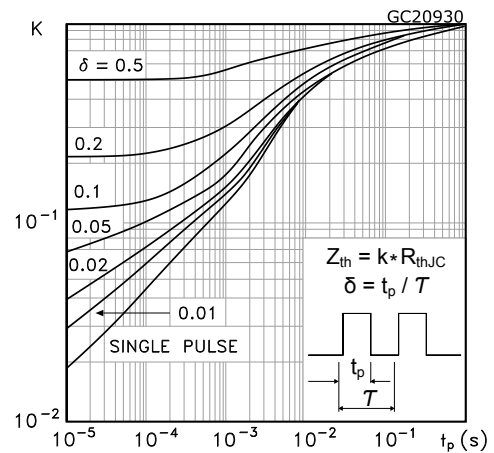
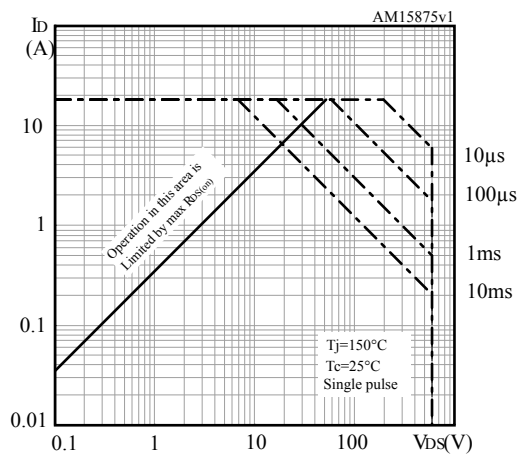
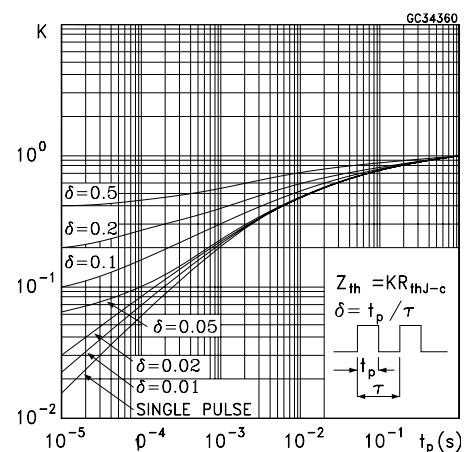
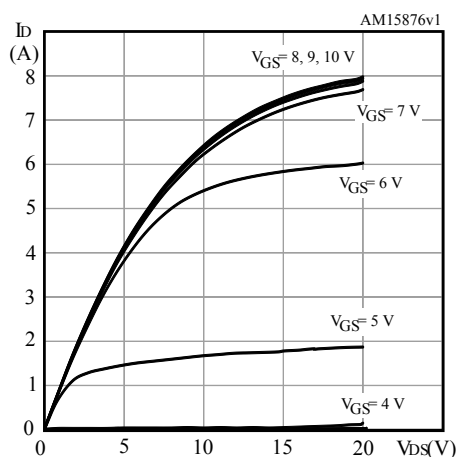
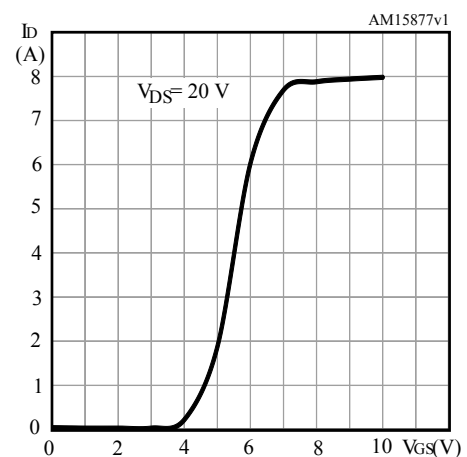
**Table 7. Source-drain diode**

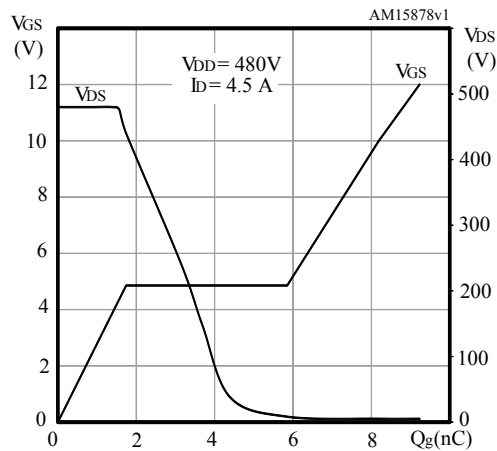
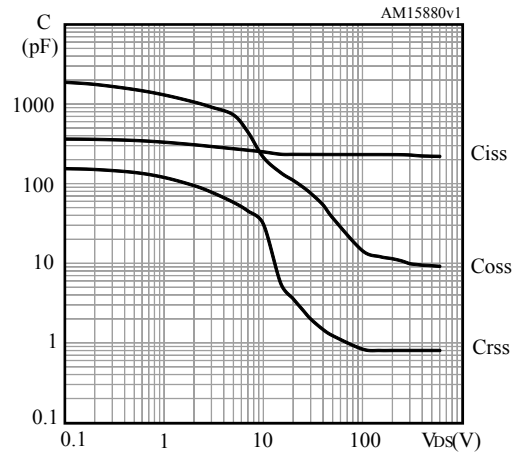
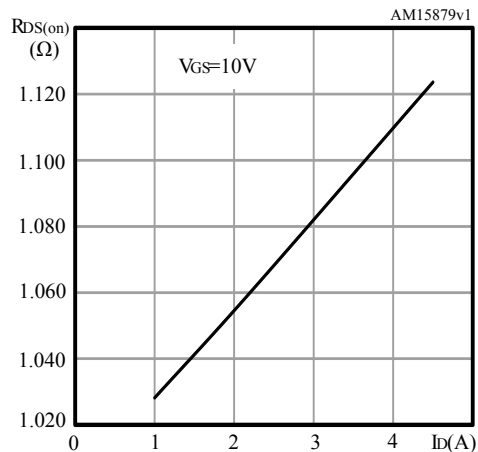
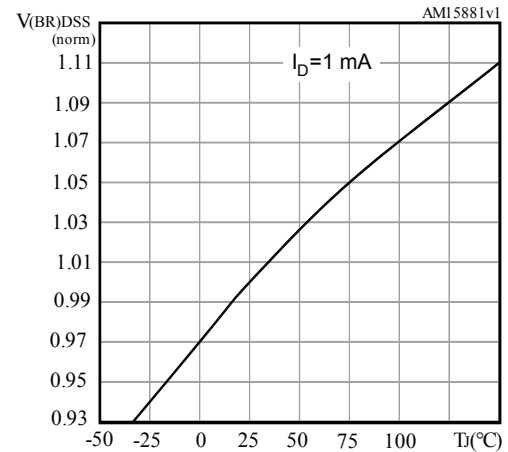
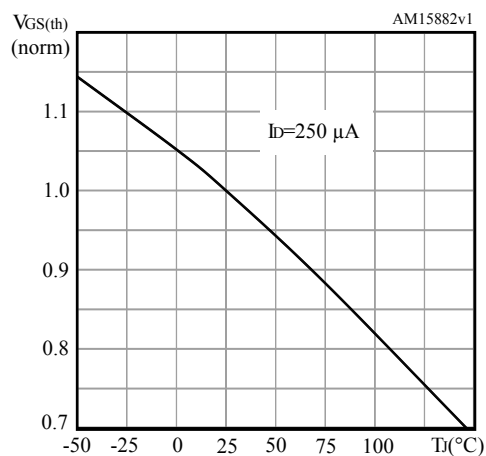
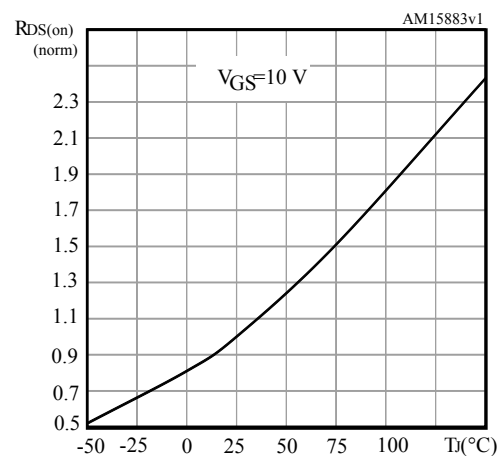
| Symbol          | Parameter                     | Test conditions                                                                                                                                                                                                             | Min. | Typ. | Max. | Unit          |
|-----------------|-------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|------|------|---------------|
| $I_{SD}$        | Source-drain current          |                                                                                                                                                                                                                             | -    | -    | 4.5  | A             |
| $I_{SDM}^{(1)}$ | Source-drain current (pulsed) |                                                                                                                                                                                                                             | -    | -    | 18   | A             |
| $V_{SD}^{(2)}$  | Forward on voltage            | $I_{SD} = 4.5 \text{ A}$ , $V_{GS} = 0 \text{ V}$                                                                                                                                                                           | -    | -    | 1.6  | V             |
| $t_{rr}$        | Reverse recovery time         | $I_{SD} = 4.5 \text{ A}$ , $di/dt = 100 \text{ A}/\mu\text{s}$ , $V_{DD} = 60 \text{ V}$<br>(see the Figure 16. Test circuit for inductive load switching and diode recovery times)                                         | -    | 274  | -    | ns            |
| $Q_{rr}$        | Reverse recovery charge       |                                                                                                                                                                                                                             | -    | 1.47 | -    | $\mu\text{C}$ |
| $I_{RRM}$       | Reverse recovery current      |                                                                                                                                                                                                                             | -    | 10.7 | -    | A             |
| $t_{rr}$        | Reverse recovery time         | $I_{SD} = 4.5 \text{ A}$ , $di/dt = 100 \text{ A}/\mu\text{s}$ ,<br>$V_{DD} = 60 \text{ V}$ , $T_J = 150 \text{ }^\circ\text{C}$<br>(see the Figure 16. Test circuit for inductive load switching and diode recovery times) | -    | 376  | -    | ns            |
| $Q_{rr}$        | Reverse recovery charge       |                                                                                                                                                                                                                             | -    | 1.96 | -    | $\mu\text{C}$ |
| $I_{RRM}$       | Reverse recovery current      |                                                                                                                                                                                                                             | -    | 10.5 | -    | A             |

1. Pulse width limited by safe operating area.

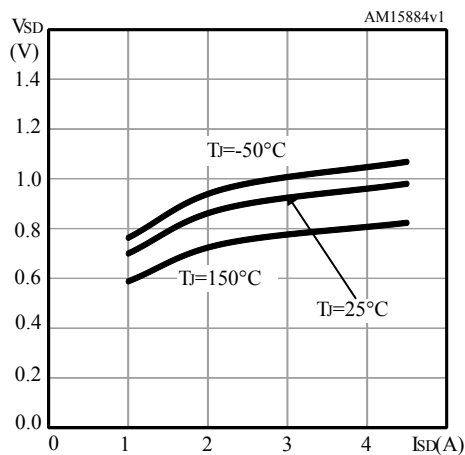
2. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%.

## 2.1 Electrical characteristics (curves)

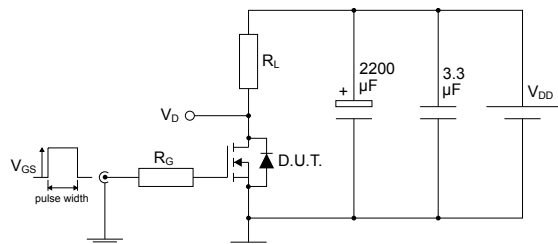
**Figure 1. Safe operating area for D<sup>2</sup>PAK**

**Figure 2. Normalized transient thermal impedance for D<sup>2</sup>PAK**

**Figure 3. Safe operating area for DPAK**

**Figure 4. Normalized transient thermal impedance for DPAK**

**Figure 5. Typical output characteristics**

**Figure 6. Typical transfer characteristics**


**Figure 7. Typical gate charge characteristics**

**Figure 8. Typical capacitance characteristics**

**Figure 9. Typical drain-source on-resistance**

**Figure 10. Normalized breakdown voltage vs temperature**

**Figure 11. Normalized gate threshold vs temperature**

**Figure 12. Normalized on-resistance vs temperature**


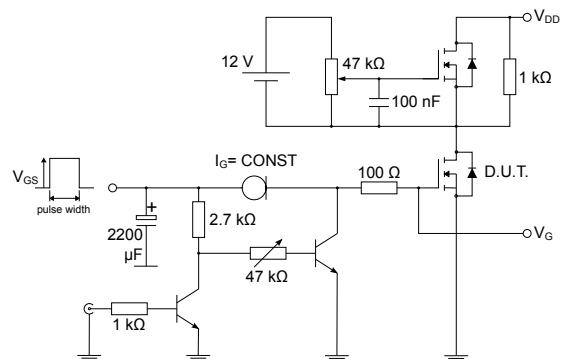
**Figure 13. Typical reverse diode forward characteristics**



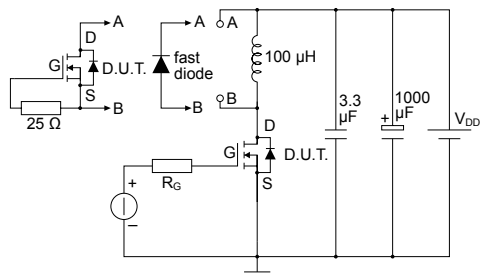
### 3 Test circuits

**Figure 14. Test circuit for resistive load switching times**


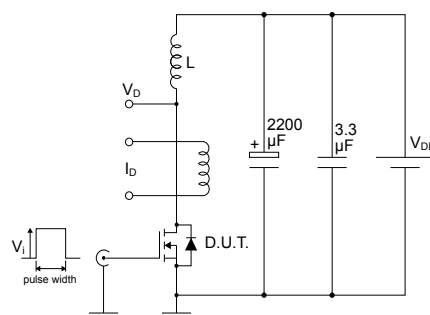
AM01468v1

**Figure 15. Test circuit for gate charge behavior**


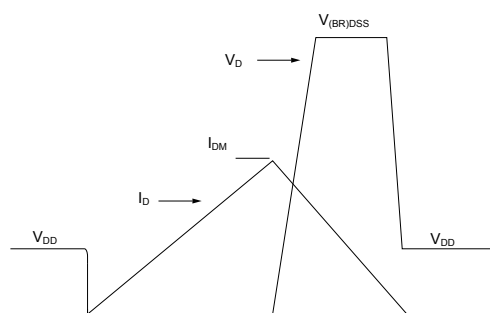
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**Figure 16. Test circuit for inductive load switching and diode recovery times**


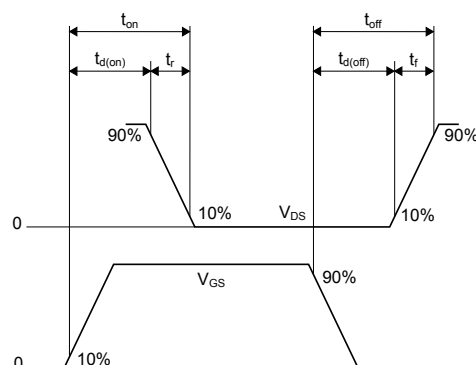
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**Figure 17. Unclamped inductive load test circuit**


AM01471v1

**Figure 18. Unclamped inductive waveform**


AM01472v1

**Figure 19. Switching time waveform**


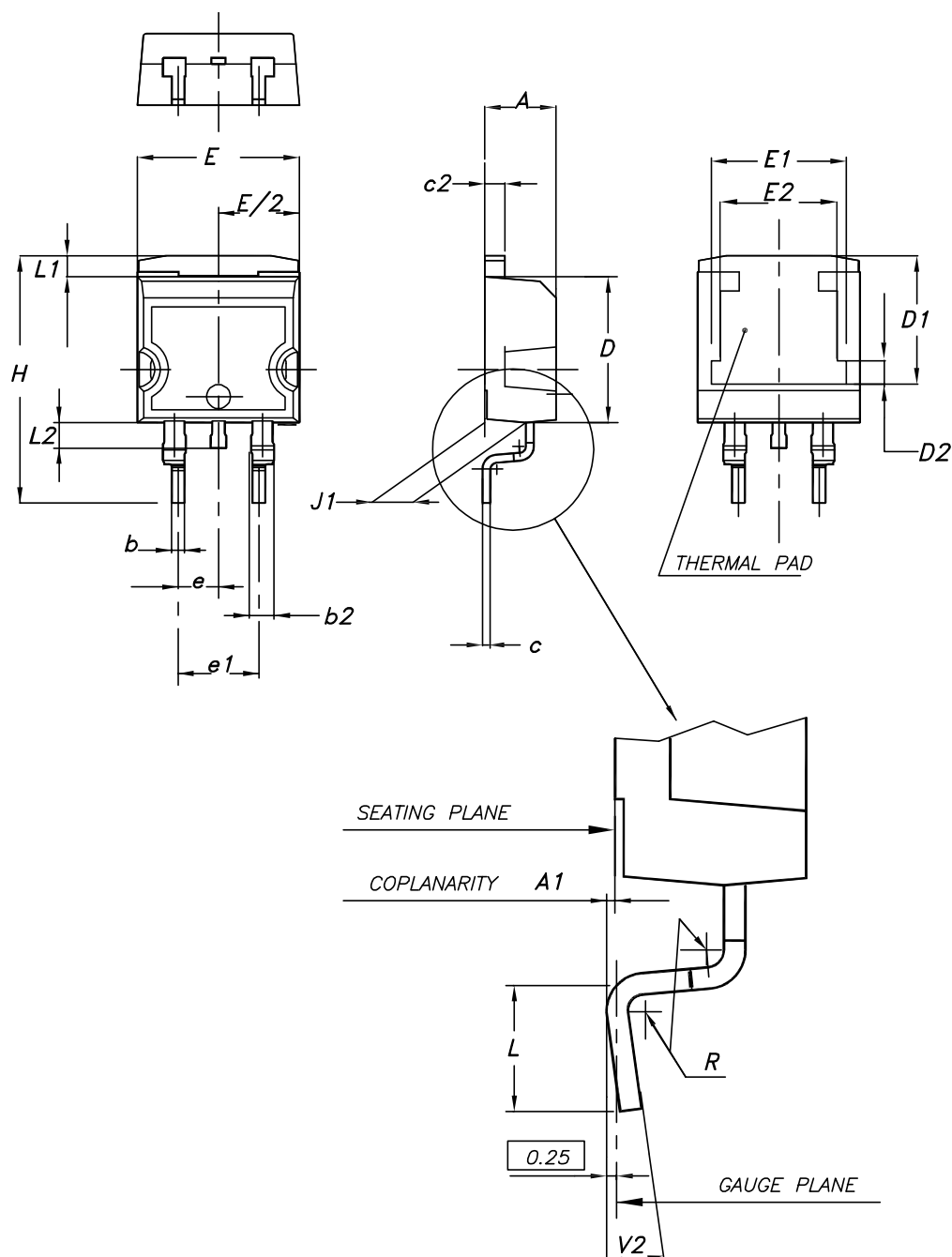
AM01473v1

## 4 Package information

To meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

### 4.1 D<sup>2</sup>PAK (TO-263) type A package information

Figure 20. D<sup>2</sup>PAK (TO-263) type A package outline

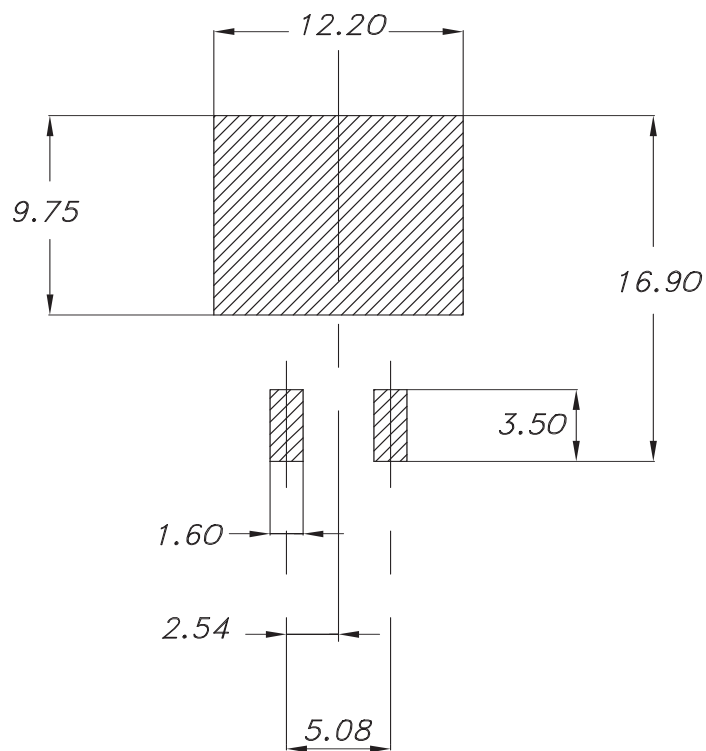


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**Table 8. D<sup>2</sup>PAK (TO-263) type A package mechanical data**

| Dim. | mm    |      |       |
|------|-------|------|-------|
|      | Min.  | Typ. | Max.  |
| A    | 4.40  |      | 4.60  |
| A1   | 0.03  |      | 0.23  |
| b    | 0.70  |      | 0.93  |
| b2   | 1.14  |      | 1.70  |
| c    | 0.45  |      | 0.60  |
| c2   | 1.23  |      | 1.36  |
| D    | 8.95  |      | 9.35  |
| D1   | 7.50  | 7.75 | 8.00  |
| D2   | 1.10  | 1.30 | 1.50  |
| E    | 10.00 |      | 10.40 |
| E1   | 8.30  | 8.50 | 8.70  |
| E2   | 6.85  | 7.05 | 7.25  |
| e    |       | 2.54 |       |
| e1   | 4.88  |      | 5.28  |
| H    | 15.00 |      | 15.85 |
| J1   | 2.49  |      | 2.69  |
| L    | 2.29  |      | 2.79  |
| L1   | 1.27  |      | 1.40  |
| L2   | 1.30  |      | 1.75  |
| R    |       | 0.40 |       |
| V2   | 0°    |      | 8°    |

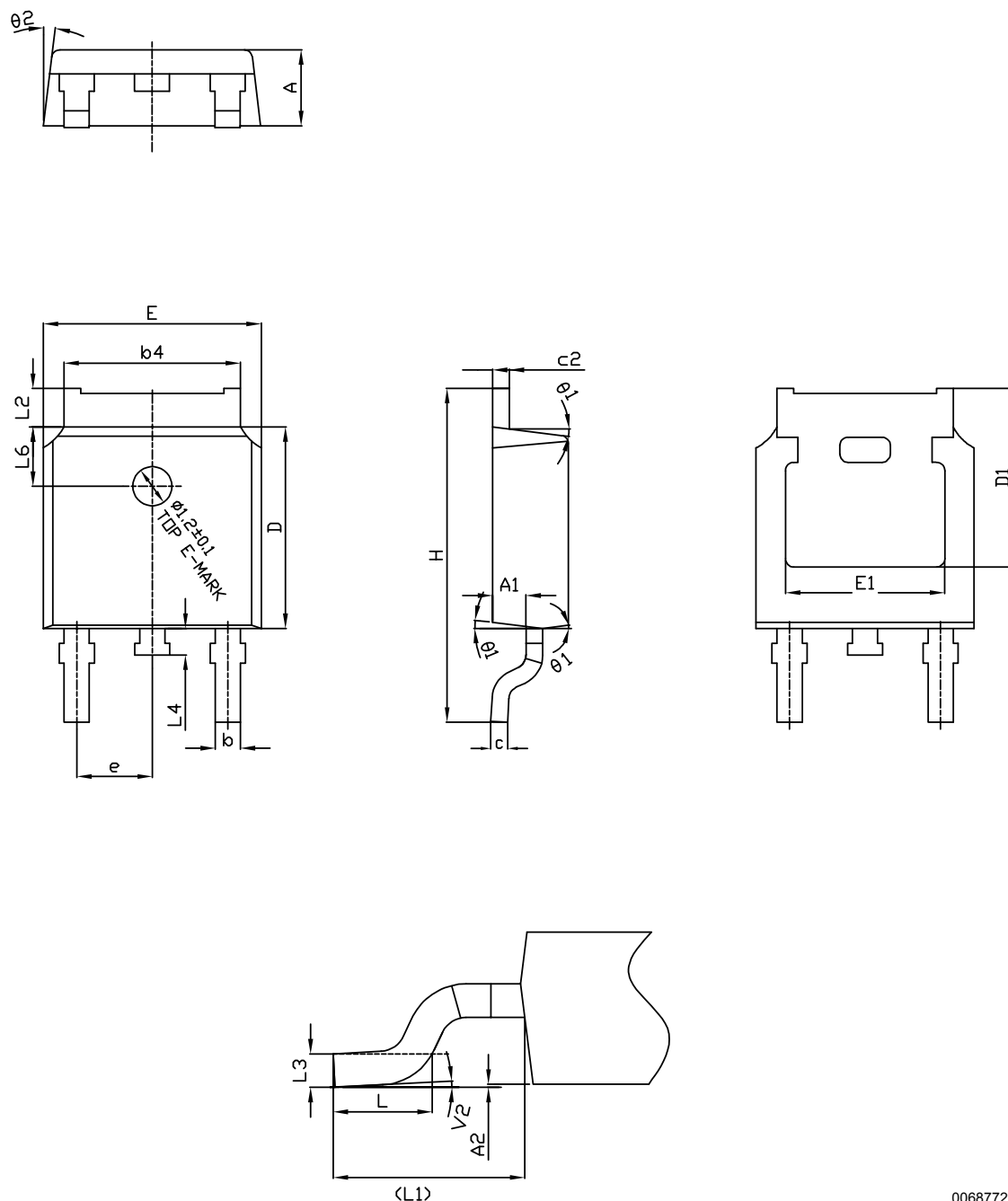
**Figure 21. D<sup>2</sup>PAK (TO-263) recommended footprint (dimensions are in mm)**



0079457\_Rev27\_footprint

## 4.2 DPAK (TO-252) type C package information

Figure 22. DPAK (TO-252) type C package outline

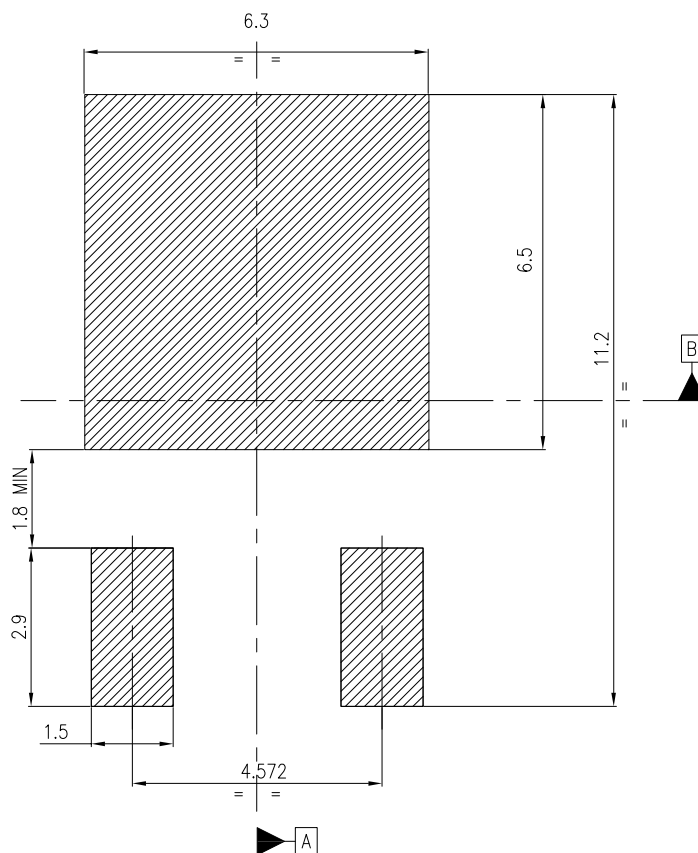


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**Table 9. DPAK (TO-252) type C mechanical data**

| Dim. | mm       |       |       |
|------|----------|-------|-------|
|      | Min.     | Typ.  | Max.  |
| A    | 2.20     | 2.30  | 2.38  |
| A1   | 0.90     | 1.01  | 1.10  |
| A2   | 0.00     |       | 0.10  |
| b    | 0.72     |       | 0.85  |
| b4   | 5.13     | 5.33  | 5.46  |
| c    | 0.47     |       | 0.60  |
| c2   | 0.47     |       | 0.60  |
| D    | 6.00     | 6.10  | 6.20  |
| D1   | 5.15     | 5.40  | 5.65  |
| E    | 6.50     | 6.60  | 6.70  |
| E1   | 4.70     | 4.85  | 5.00  |
| e    | 2.186    | 2.286 | 2.386 |
| H    | 9.80     | 10.10 | 10.40 |
| L    | 1.40     | 1.50  | 1.70  |
| L1   | 2.90 REF |       |       |
| L2   | 0.90     |       | 1.25  |
| L3   | 0.51 BSC |       |       |
| L4   | 0.60     | 0.80  | 1.00  |
| L6   | 1.80 BSC |       |       |
| θ1   | 5°       | 7°    | 9°    |
| θ2   | 5°       | 7°    | 9°    |
| V2   | 0°       |       | 8°    |

**Figure 23. DPAK (TO-252) recommended footprint (dimensions are in mm)**



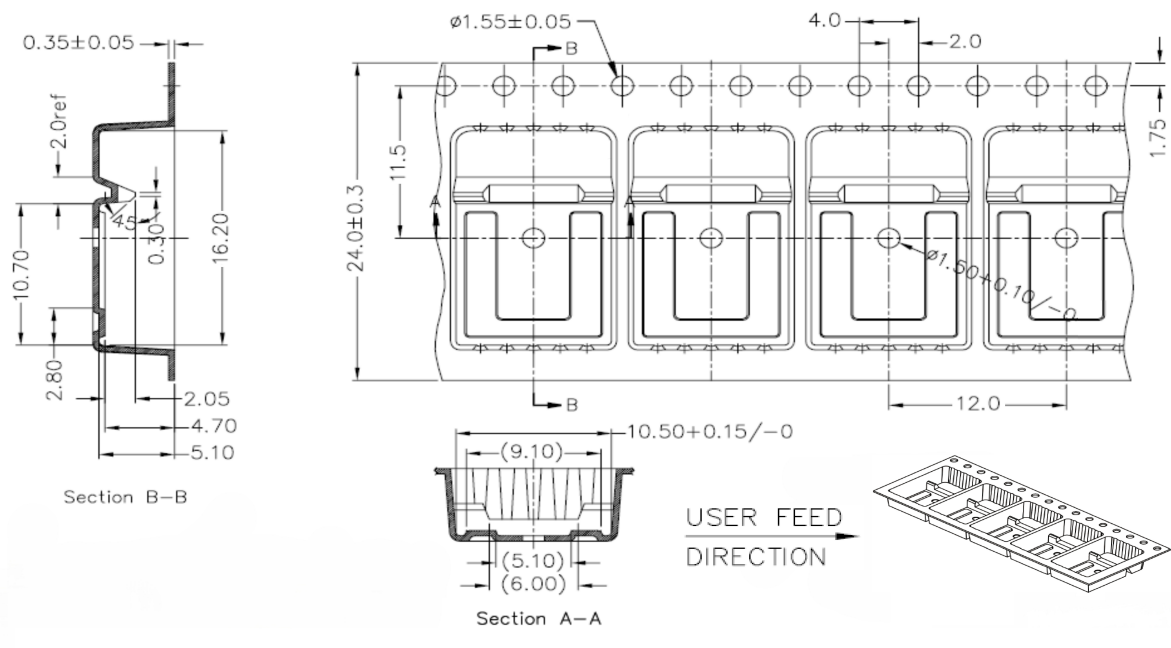
Notes:

- 1) This footprint is able to ensure insulation up to 630 Vrms (according to CEI IEC 664-1)
- 2) The device must be positioned within  $\boxed{\Phi 0.05 \text{ A B}}$

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### 4.3 D<sup>2</sup>PAK packing information

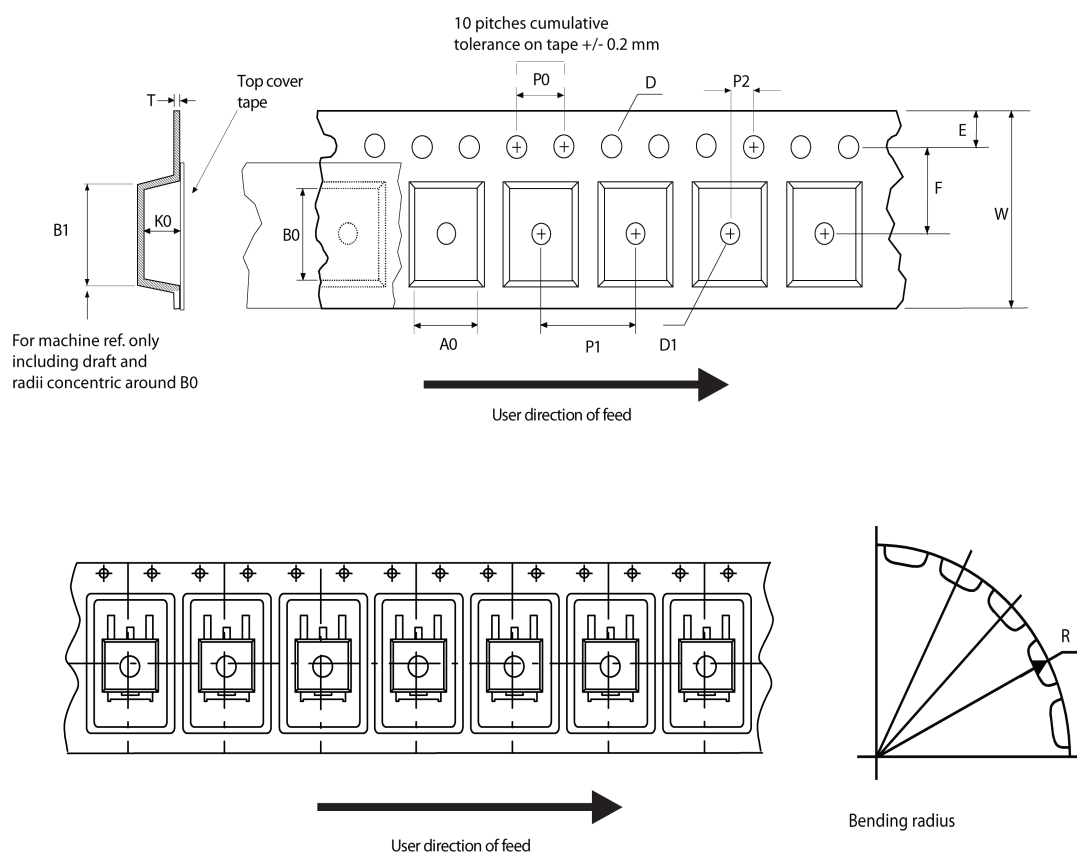
**Figure 24. D<sup>2</sup>PAK tape drawing (dimensions are in mm)**



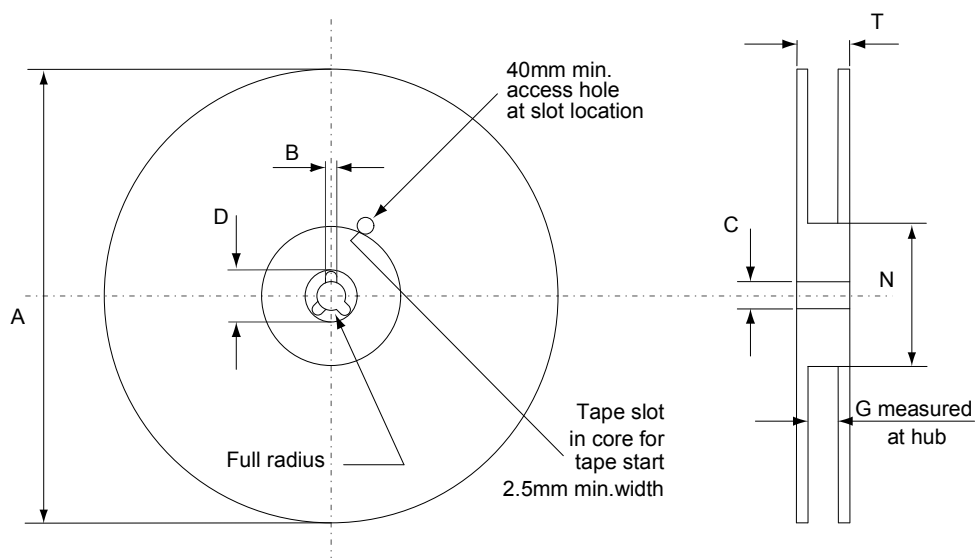
DM01095771\_2

## 4.4 DPAK packing information

Figure 25. DPAK tape outline



AM08852v1

**Figure 26. DPAK reel outline**


AM06038v1

**Table 10. DPAK tape and reel mechanical data**

| Tape |      |      | Reel      |      |      |
|------|------|------|-----------|------|------|
| Dim. | mm   |      | Dim.      | mm   |      |
|      | Min. | Max. |           | Min. | Max. |
| A0   | 6.8  | 7    | A         |      | 330  |
| B0   | 10.4 | 10.6 | B         | 1.5  |      |
| B1   |      | 12.1 | C         | 12.8 | 13.2 |
| D    | 1.5  | 1.6  | D         | 20.2 |      |
| D1   | 1.5  |      | G         | 16.4 | 18.4 |
| E    | 1.65 | 1.85 | N         | 50   |      |
| F    | 7.4  | 7.6  | T         |      | 22.4 |
| K0   | 2.55 | 2.75 |           |      |      |
| P0   | 3.9  | 4.1  | Base qty. |      | 2500 |
| P1   | 7.9  | 8.1  | Bulk qty. |      | 2500 |
| P2   | 1.9  | 2.1  |           |      |      |
| R    | 40   |      |           |      |      |
| T    | 0.25 | 0.35 |           |      |      |
| W    | 15.7 | 16.3 |           |      |      |

## Revision history

**Table 11. Document revision history**

| Date        | Revision | Changes                                                                                                                                                                                                                                  |
|-------------|----------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 11-Jun-2013 | 1        | First release.                                                                                                                                                                                                                           |
| 09-Jul-2013 | 2        | Modified: $R_{thj-case}$ value for D <sup>2</sup> PAK in <i>Table 3</i> .<br>Minor text changes.                                                                                                                                         |
| 30-May-2016 | 3        | Updated title, features and description.<br>Updated <i>Table 6: Dynamic</i> and <i>Table 8: Source drain diode</i> .<br>Updated <i>Section 4: Package information</i> and <i>Section 5: Packing information</i> .<br>Minor text changes. |
| 19-Sep-2025 | 4        | Updated <a href="#">Section 4: Package information</a> .<br>Minor text changes.                                                                                                                                                          |

## Contents

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| <b>4</b> | <b>Package information</b>                             | <b>9</b>  |
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