RTL8019AS

Realtek Full-Duplex Ethernet Controller with Plug and Play Function (RealPNP)

ADVANCE INFORMATION

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RTL8019AS

Contents:

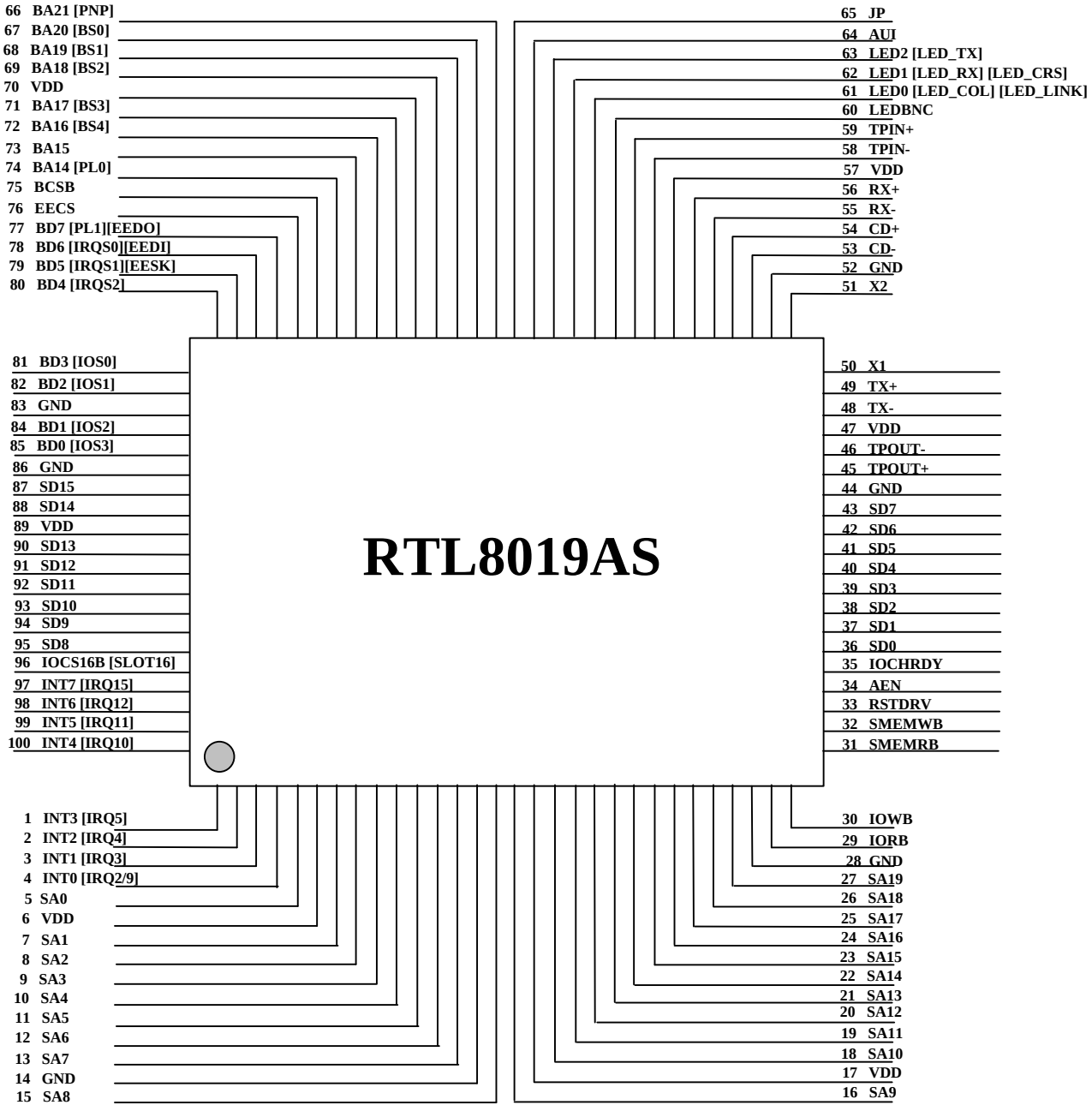
1. Features:

¡ERTL8019 software compatible
¡ESupports PnP auto detect mode
¡E16k byte SRAM built in
¡ESupports flash memory read/write
¡ESupports UTP, AUI & BNC auto-detect
¡ESupports IO address fully decode mode
¡EMakes PnP jumper option more user-friendly
¡EImproves the blinking problem of CRS LED when the cable is not connected

2. General Description

The RTL8019AS integrates the RTL8019 and 16K-byte SRAM in a single chip. It is designed not only to provide more friendly functions but also to save the effort of SRAM sourcing and inventory. Most of the design spec. inherit from RTL8019. *Thus, this document mainly describes those spec. different from RTL8019.*

3. Pin Configuration



Total Pin Count	Pin Number	Type	Symbol 1	Symbol 2	Symbol 3	Status
4	6, 17, 70, 89	P	VDD			
3	14, 28, 83, 86	P	GND			
2	57, 47	P	AVDD			
2	52, 44	P	AGND			
1	34	I	AEN			
8	97-100, 1-4	O	INT7-0	IRQ15, 12, 11, 10, 5, 4, 3, 2/9		
1	35	OD	IOCHRDY			
1	96	OD	IOCS16B	SLOT16		
1	29	I	IORB			
1	30	I	IOWB			
1	33	I	RSTDRV			
20	27-18, 16-15, 13-7, 5	I	SA19-0			SA10, 12, 13 new
16	87, 88, 90-95, 43-36	IO	SD15-0			
1	31	I	SMEMRB			
1	32	I	SMEMWB			new
1	75	O	BCSB			
1	76	O	EECS			
1	85	IO	BD0	IOS3		
1	84	IO	BD1	IOS2		
1	82	IO	BD2	IOS1		
1	81	IO	BD3	IOS0		
1	80	IO	BD4	IRQS2		
1	79	IO	BD5	IRQS1	EESK	
1	78	IO	BD6	IRQS0	EEDI	
1	77	IO	BD7	PL1	EEDO	
1	74	O	BA14	PL0		
1	73	O	BA15			
1	72	O	BA16	BS4		
1	71	O	BA17	BS3		

1	69	O	BA18	BS2		
1	68	O	BA19	BS1		
1	67	O	BA20	BS0		
1	66	O	BA21	PNP		
1	65	I	JP			
1	63	O	LED2	LED_TX		
1	62	O	LED1	LED_RX	LED_CRS	
1	61	O	LED0	LED_COL	LED_LINK	
1	60	O	LEDBNC			
1	64	I	AUI			new
2	59, 58	I	TPIN+/-			
2	45, 46	O	TPOUT+/-			
2	56, 55	I	RX+/-			
2	54, 53	I	CD+/-			
2	49, 48	O	TX+/-			
2	50, 51	I, O	X1, X2			

4. Pin Descriptions

SA10:
SA10 is added to implement the fully decode of PnP ports, address 279h and A79h. In RTL8019, SA10 is not decoded. In RTL8019AS, SA10 should be 0 for a valid access to PnP ports.

SA12:
SA12 is from ISA bus.

SA13:
SA13 is from ISA bus.

SMEMWB:
This pin is added to decode the write command of a flash memory.

BA14-21:
After RTL8019 latches all jumper status upon power on reset, these pins ***always**** reflect the value of BPAGE register directly in BROM page mode. In normal mode, BA16-21 are not used and BA14-15 act as:

BROM Size	BA14	BA15
16K	high	high
32K	SA14	high
64K	SA14	SA15

*Note: RTL8019 doesn't drive BA14-21 until the SMEMRB goes from high to low.

BCSB:
RTL8019AS drives this pin low when SA19-14 matches the selected BROM memory base address and either of the 2 conditions below meets:
(1) SMEMRB is low
(2) SMEMWB is low and RTL8019AS's flash memory write function is enabled.

AUI:
This input is used to detect the usage of an external MAU on the AUI interface. The input should be driven low for embedded BNC and high for external MAU. When the input is high, RTL8019AS sets

the AUI bit (bit5) in CONFIG0 and drives LEDBNC low to disable the BNC. If this pin is not used, it should be connected to GND such that RTL8019AS acts like RTL8019. Please refer to section 5.2. CONFIG0 for more details.

5. Function Descriptions

5.1. Register Table

No (Hex)	Page0		Page1	Page2	Page3	
	[R]	[W]	[R/W]	[R]	[R]	[W]
00	CR	CR	CR	CR	CR	CR
01	CLDA0	PSTART	PAR0	PSTART	***9346CR***	***9346CR***
02	CLDA1	PSTOP	PAR1	PSTOP	***BPAGE***	***BPAGE***
03	BNRY	BNRY	PAR2	-	***CONFIG0***	-
04	TSR	TPSR	PAR3	TPSR	***CONFIG1***	***CONFIG1***
05	NCR	TBCR0	PAR4	-	***CONFIG2***	***CONFIG2***
06	FIFO	TBCR1	PAR5	-	***CONFIG3***	***CONFIG3***
07	ISR	ISR	CURR	-	-	***TEST***
08	CRDA0	RSAR0	MAR0	-	***CSNSAV***	-
09	CRDA1	RSAR1	MAR1	-	-	***HLTCLK***
0A	***8019ID0***	RBCR0	MAR2	-		
0B	***8019ID1***	RBCR1	MAR3	-	***INTR***	-
0C	RSR	RCR	MAR4	RCR	-	***FMWP***
0D	CNTR0	TCR	MAR5	TCR	***CONFIG4***	-
0E	CNTR1	DCR	MAR6	DCR	-	-
0F	CNTR2	IMR	MAR7	IMR	-	-
10-17	Remote DMA Port					
18-1F	Reset Port					

Notes: "-" denotes reserved. Registers with names typed in ***bold italic*** format are RTL8019AS defined registers and are not supported in a standard NE2000 adapter.

Page 3(PS1=1, PS0=1)

No.	Name	Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00H	CR	R/W	PS1	PS0	RD2	RD1	RD0	TXP	STA	STP
01H	9346CR	R	EEM1	EEM0	-	-	EECS	EESK	EEDI	EEDO
		W	EEM1	EEM0	-	-	EECS	EESK	EEDI	-
02H	BPAGE	R/W	BP7	BP6	BP5	BP4	BP3	BP2	BP1	BP0
03H	CONFIG0	R	*VerID1*	*VerID0*	*AUI*	*PNPJP*	JP	BNC	0	0
04H	CONFIG1	R	IRQEN	IRQS2	IRQS1	IRQS0	IOS3	IOS2	IOS1	IOS0
		W*	IRQEN	-	-	-	-	-	-	-
05H	CONFIG2	R	PL1	PL0	BSELB	BS4	BS3	BS2	BS1	BS0
		W*	PL1	PL0	BSELB	-	-	-	-	-
06H	CONFIG3	R	PNP	FUDUP	LEDS1	LEDS0	-	SLEEP	PWRDN	ACTIVEB
		W*	-	-	-	-	-	SLEEP	PWRDN	-
07H	TEST	R/W	Reserved, Do not write							
08H	CSNSAV	R	CSN7	CSN6	CSN5	CSN4	CSN3	CSN2	CSN1	CNS0
09H	HLTCLK	W	HLT7	HLT6	HLT5	HLT4	HLT3	HLT2	HLT1	HLT0
0AH	-	-	Reserved							
0BH	INTR	R	INT7	INT6	INT5	INT4	INT3	INT2	INT1	INT0
0CH	*FMWP*	*W**	*Flash Memory Write Protect*							
0DH	CONFIG4	R	-	-	-	-	-	-	-	IOMS
0EH | 0FH	-	-	Reserved							

Note: The registers marked with type='W*' can be written only if bits EEM1=EEM0=1.

5.2. Register Descriptions

CONFIG0 (8390 Page3 offset 03h):

Bits	Name	Type	Description
7-6	VERID	R/W	Version ID: These two bits are defined as below.

Bit7	Bit6	Type	Mode
1	1	R	**RTL8019**
0	0	R	**RTL8019A**

			0	0	R/W	**RTL8019AS**, these two bits are all "0" when power on, but can be written in RTL8019AS's config write enable mode (EEM0=EEM1=1). Software uses these differences to identify the chip.
5	AUI	R	This bit is set when external MAU is used on AUI interface. Therefore it is set when in 10Base5 mode or the AUI input pin is high.			
4	PNPJP	R	This bit is set when PNP jumper pin is pulled high externally.			
3	JP	R	same as RTL8019			
2	BNC	R	same as RTL8019			
1-0	0	R	same as RTL8019			

CONFIG4 (8390 Page3 offset 0Dh):

Bits	Name	Type	Description
7-1	-	-	Reserved
0	IOMS	R	When this bit is set, RTL8019AS uses SA15-SA0 to decode I/O address of NE2000 registers. When this bit is reset, RTL8019AS only decodes SA9-SA0 like the RTL8019 does. This mode is supported for applications which might require to fully decode I/O address. This bit is read-only and comes from the CONFIG4 byte(Offset 03H) of 9346(refer to section 5.5).

The following table describes the behavior of bits and pins for cabling media.

Media Type	AUI Input	Selected Media	AUI Bit	BNC Bit	LEDBNC Output	Original BNC bit in 8019 (For reference only)
10Base5	x	AUI	1	0	L	0
10Base2	x	BNC	0	1	H	1
10BaseT Link disabled	x	UTP	0	0	L	0
Auto detect Link OK	x	UTP	0	0	L	0
Auto detect Link fail	L	BNC	0	1	H	1

Auto detect Link fail	H	AUI	1	0	L	1

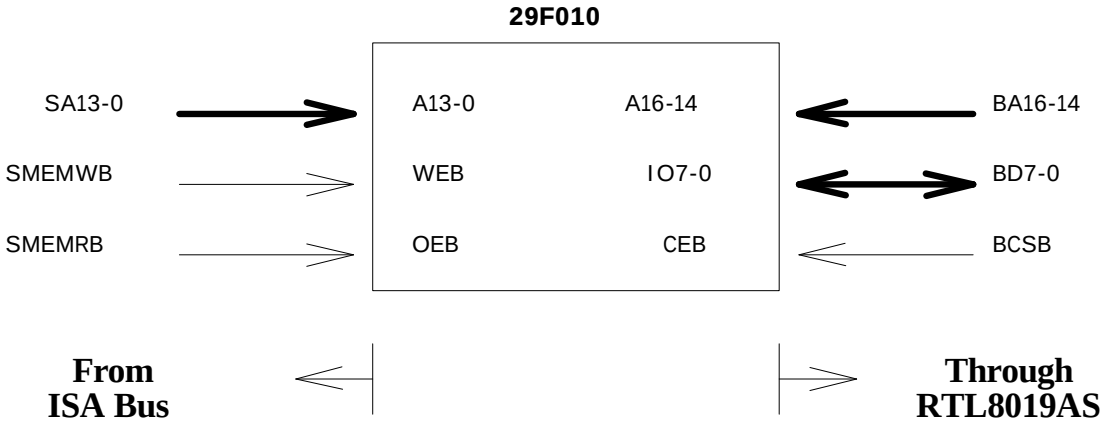
FMWP (8390 Page3 offset 0Ch): Flash Memory Write Protect Register

This register is write only. A write to this register is valid only when EEM0=EEM1=1. Sequentially writing 2 bytes of data (57H then A8H) to this register enables the flash memory write operation. Writing other data to this register will reset the write sequence and disable the flash write. All flash memory write commands from host are ignored if the write operation is not enabled.

5.3. Boot ROM

Whether a EPROM or flash memory is used as the BROM, RTL8019AS's BROM read operation is still the same as RTL8019's. The supported BROM size is the same, too.

The write operation of a flash memory is much like the read except that a SMEMWB command is issued instead of SMEMRB. The block diagram below shows the application when an 128k*8bit flash memory (e.g. 29F010) is used as the BROM.



In this case, the BROM page mode is used. Before either to read or write BROM, the appropriate ROM page must be set in the BPAGE (page3, offset 02h) register first. The RTL8019AS will always reflect the content of BPAGE onto the BA14-21 bus. When RTL8019AS decodes a valid BROM read or write command, it asserts BCSB low. Note the flash memory write must be enabled through the RTL8019AS's FMWP register before the host's flash write command.

5.4. Changed Function of RTL8019

5.4.1. Power up default ACTIVE state

In RTL8019, the ACTIVEB bit in 93C46 decides the power-up adapter status even in RT jumpless mode. In the standard application when BROM is not enabled, the adapter should be power up inactive in PnP mode and active in RT jumperless mode. However RTL8019's PnP jumper only decides the jumperless mode. The adapter's "ACTIVE" status is not changed properly at the same time when the user changes the PnP jumper state. This causes an application inconsistence when PnP jumper is to be used.

In RTL8019AS, we change RTL8019's original specification into:
The ACTIVEB bit in 9346 is ignored when RTL8019AS is in jumper or RT jumperless mode. The adapter's power-up status is always "ACTIVE" in RT jumperless mode. However, the active status still can be changed via the PnP Activate register.

New relations are shown below:

JP jumper	PnP jumper	9346 Content		Mode	CONFIG0		CONFIG3	
		PNP	ACTIVEB		JP	PNPJP	PNP	ACTIVEB
H	H L	x	x	Jumper	1	1 0	0	0
L	H	x	a (a=0or1)	PnP	0	1	1	a
L	L	1	a (a=0or1)	PnP	0	0	1	a
L	L	0	x	RT jmpless	0	0	0	0

5.4.2. PnP auto detect mode

When using RTL8019, the user needs to setup the card to PnP or jumperless mode according to the host environments. The typical operating modes of a RTL8019 card include:
(1) when used in a non-PnP PC, set the card to RT jumperless mode & power-on active
(2) when used in a PnP PC,
  (2.1) if BROM disabled, set the card to PnP mode & power-on inactive
  (2.2) if BROM enabled, set the card to PnP mode & power-on active
P.S. PCs with PnP BIOS, or Windows 95, or Intel Configuration Manager, etc. are called PnP PCs

If a card in mode(2.1) is put in a non-PnP PC, the drivers will fail to initialize the card. RTL8019AS supports a PnP auto-detect mode to solve the problem. ***The card may be set to a default state: PnP mode & power-on active with BROM disabled.*** If the card is in a non-PnP PC, it will work like a normal jumperless card. If the card is in a PnP PC which requires the card to be power-on inactive, RTL8019AS will change itself into inactive state when the first time a PnP init key is detected.

5.4.3. LED1 (LED_RX or LED_CRS)

RTL8019's LED_RX or LED_CRS LED sometimes keeps blinking when the media type of a 2-in-1 (UTP+BNC) LAN adapter is set to auto-detect and both UTP and coaxial cable are not connected. In the case, RTL8019 is actually using the BNC because the UTP link test fails. Many 8392 will falsely detect a carrier when the BNC inteface is not properly terminated (e.g. coaxial cable is not connected). That carrier sense will then make RTL8019's LED_RX or LED_CRS blink. The problem is that not all 8392s cause the LED blinking, which makes the phenomenon very ambiguous. Considering the phenomenon is normally awared upon power on, we change RTL8019's original function to solve the problem to some extent.

The new specification is:
The LED_RX or LED_CRS does not reflect the carrier sense when the CR register bit 0 is set (in stop mode). Thus, the false carrier due to cabling problem upon power on will not cause the LED1 to blink anymore.

5.5. 9346 Contents

The 9346 is a 1k-bit EEPROM. Although it is actually addressed by words, we list its contents by bytes below for convenience.

Bytes		Contents	Comments
00H - 03H	**(4 bytes)**		**Power-up initial value of Page3 and PnP logical device configuration registers**
	00H	CONFIG1	
	01H	CONFIG2	
	02H	CONFIG3	
	03H	CONFIG4	
04H - 11H	**(14 bytes)**		**NE2000 IDPROM**
	04H - 09H	Ethernet ID 0-5	Ethernet node address
	0AH - 11H	Product ID 0-7	Assigned by card makers; negligible
12H - 1AH	**(9 bytes)**		**Plug and Play Serial Identifier**
	12H - 15H	Vendor ID 0-3	
	16H - 19H	Serial Number 0-3	
	1AH	Serial ID Checksum	
1BH - 7FH	**(101 bytes)**		**Plug and Play Resource Data**

6. DC/AC Characteristics

Please refer to RTL8019.

7. Application Circuit

See Appedix