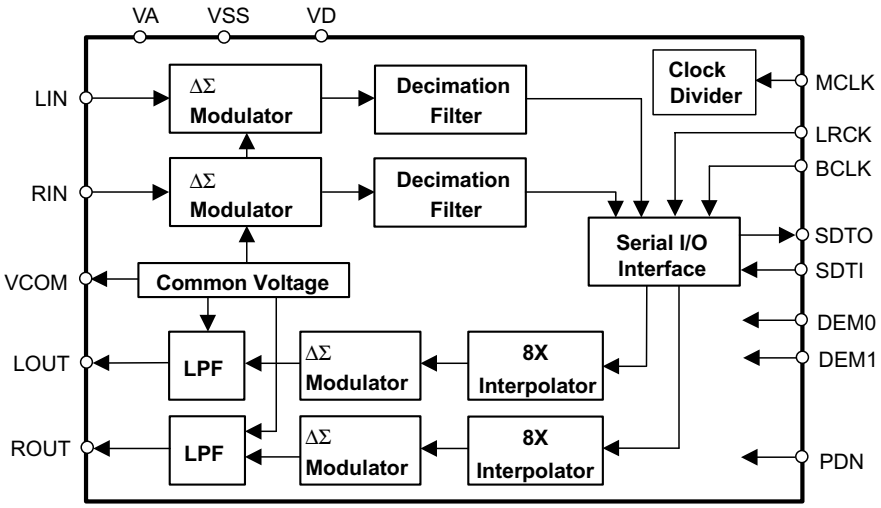
AK4552
3V 96kHz 24Bit ΔΣ CODEC

GENERAL DESCRIPTION

The AK4552 is a low voltage 24bit 96kHz A/D & D/A converter for digital audio system. In the AK4552, the loss of accuracy form clock jitter is also improved by using SCF techniques for on-chip post filter. Analog signal input/output of the AK4552 are single-ended, therefore, any external filters are not required. As the package is 16pin TSSOP, the AK4552 is a suitable for minimizing system.

FEATURES

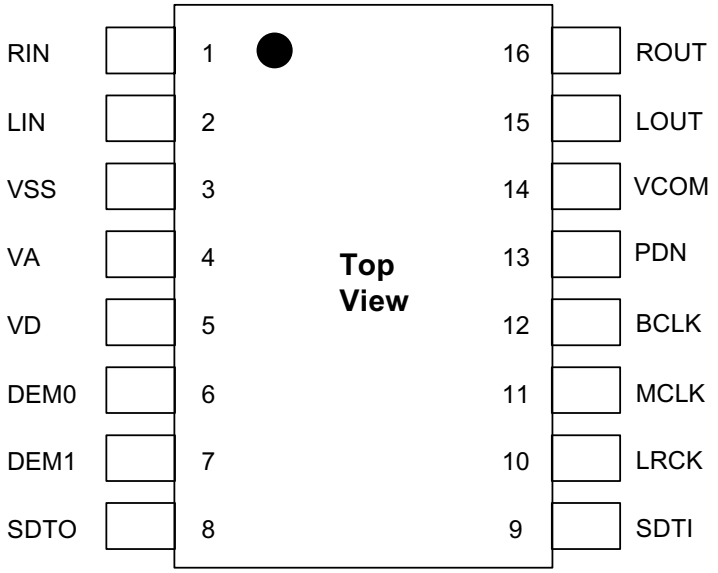
- ☐ **HPF for DC-offset cancel (fc=3.4Hz@fs=44.1kHz)**
- ☐ **Single-ended ADC**
  - **S/(N+D): 89dB@VA=3.0V**
  - **Dynamic Range, S/N: 97dB@VA=3.0V**
- ☐ **Single-ended DAC**
  - **Digital de-emphasis for 32kHz, 44.1kHz and 48kHz sampling**
  - **S/(N+D): 88dB@VA=3.0V**
  - **Dynamic Range, S/N: 100dB@VA=3.0V**
- ☐ **Audio I/F format: MSB First, 2's Compliment**
  - **ADC: 24bit MSB justified, DAC: 24bit LSB justified**
- ☐ **Input/Output Voltage: ADC = 1.85Vpp@VA=3.0V**
  DAC = 1.75Vpp@VA=3.0V
- ☐ **Sampling Rate: 8kHz to 50kHz (Normal Speed)**
  50kHz to 100kHz (Double Speed, Double Speed Monitor)
  100kHz to 200kHz (Quad Speed Monitor)
- ☐ **Master Clock: 256fs, 384fs, 512fs or 768fs@Normal Speed**
  256fs or 384fs@Double Speed
  128fs or 192fs@Double Speed Monitor
  64fs, 96fs, 128fs or 192fs@Quad Speed Monitor
- ☐ **Power Supply: 2.4 to 4.0V**
- ☐ **Power Supply Current: 14mA**
- ☐ **Ta = -40 to 85°C**
- ☐ **Very Small Package: 16pin TSSOP**



■ Ordering Guide

AK4552VT	-40 ~ +85°C	16pin TSSOP (0.65mm pitch)
AKD4552	Evaluation Board for AK4552	

■ Pin Layout



PIN/FUNCTION

No.	Pin Name	I/O	Function
1	RIN	I	Rch Analog Input Pin
2	LIN	I	Lch Analog Input Pin
3	VSS	-	Ground Pin
4	VA	-	Analog Power Supply Pin
5	VD	-	Digital Power Supply Pin
6	DEM0	I	De-emphasis Control Pin
7	DEM1	I	De-emphasis Control Pin
8	SDTO	O	Audio Serial Data Output Pin
9	SDTI	I	Audio Serial Data Input Pin
10	LRCK	I	Input/Output Channel Clock Pin
11	MCLK	I	Master Clock Input Pin
12	BCLK	I	Audio Serial Data Clock Pin
13	PDN	I	Power-Down & Reset Mode Pin "L": Power-down and Reset, "H": Normal operation
14	VCOM	O	Common Voltage Output Pin, 0.45 x VA
15	LOUT	O	Lch Analog Output Pin
16	ROUT	O	Rch Analog Output Pin

ABSOLUTE MAXIMUM RATINGS

(VSS=0V; Note 1)

Parameter		Symbol	min	max	Units
Power Supply	Analog Power Supply	VA	-0.3	4.6	V
	Digital Power Supply	VD	-0.3	4.6	V
Input Current (Any Pin Except Supplies)		IIN	-	±10	mA
Analog Input Voltage (LIN, RIN pin)		VINA	-0.3	VA+0.3	V
Digital Input Voltage		VIND	-0.3	VD+0.3	V
Ambient Temperature (power applied)		Ta	-40	85	°C
Storage Temperature		Tstg	-65	150	°C

Note: 1. All voltages with respect to ground.

WARNING: Operation at or beyond these limits may results in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(VSS=0V; Note 1)

Parameter		Symbol	min	typ	max	Units
Power Supply	Analog Power Supply	VA	2.4	3.0	4.0	V
	Digital Power Supply (Note 2)	VD	2.4 or VA-0.3	3.0	4.0	V

Note: 1. All voltages with respect to ground.
Note: 2. Min Value is high value either 2.4V or VA-0.3V.

*AKM assumes no responsibility for the usage beyond the conditions in this data sheet.

ANALOG CHARACTERISTICS

(Ta=25°C; VA, VD=3.0V; VSS=0V; fs=44.1kHz; Signal Frequency=1kHz; BCLK=64fs;
Measurement frequency=10Hz ~ 20kHz at fs=44.1kHz, 20Hz ~ 40kHz at fs=96kHz; unless otherwise specified)

Parameter			min	typ	max	Units
ADC Analog Input Characteristics: (Note 3)						
Resolution					24	Bits
S/(N+D)	(-0.5dB Input)	fs=44.1kHz	80	89		dB
		fs=96kHz	80	89		dB
D-Range	(-60dB Input)	fs=44.1kHz, A-weighted	90	97		dB
		fs=96kHz	87	94		dB
		fs=96kHz, A-weighted	-	100		dB
S/N		fs=44.1kHz, A-weighted	90	97		dB
		fs=96kHz	87	94		dB
		fs=96kHz, A-weighted	-	100		dB
Interchannel Isolation			90	110		dB
Interchannel Gain Mismatch				0.2	0.5	dB
Input Voltage		(Note 4)	1.65	1.85	2.05	Vpp
Input Resistance		fs=44.1kHz	20	34	-	kΩ
		fs=96kHz	14	24	-	kΩ
DAC Analog Output Characteristics:						
Resolution					24	Bits
S/(N+D)	(0dB Output)	fs=44.1kHz	78	88		dB
		fs=96kHz	75	85		dB
D-Range	(-60dB Output)	fs=44.1kHz, A-weighted	93	100		dB
		fs=96kHz	88	96		dB
		fs=96kHz, A-weighted	-	100		dB
S/N		fs=44.1kHz, A-weighted	93	100		dB
		fs=96kHz	88	96		dB
		fs=96kHz, A-weighted	-	100		dB
Interchannel Isolation			90	110		dB
Interchannel Gain Mismatch				0.2	0.5	dB
Output Voltage		(Note 4)	1.56	1.75	1.94	Vpp
Load Resistance			10			kΩ
Load Capacitance					30	pF
Power Supplies						
Power Supply Current (VA+VD)						
	Power up	PDN = "H" fs=44.1kHz		14	21	mA
		PDN = "H" fs=96kHz		18	27	mA
	Power down (Note 5)	PDN = "L"		10	100	μA

Note: 3. The offset of ADC is removed by internal HPF.
Note: 4. Input/Output of ADC and DAC scales with VA voltage. (ADC = 0.617 x VA, DAC = 0.583 x VA)
Note: 5. In case of power-down mode, all digital input including clocks pins (MCLK, BCLK, LRCK) are held VD or VSS. But PDN pin is held VSS.

FILTER CHARACTERISTICS

(Ta=25°C; VA, VD=2.4 ~ 4.0V; fs=44.1kHz; DEM0="1", DEM1="0")

Parameter		Symbol	min	typ	max	Units
ADC Digital Filter (Decimation LPF):						
Passband (Note 6)	±0.1dB	PB	0		17.4	kHz
	-1.0dB			20.0		kHz
	-3.0dB			21.1		kHz
Stopband (Note 6)		SB	27.0			kHz
Passband Ripple		PR			±0.1	dB
Stopband Attenuation		SA	65			dB
Group Delay (Note 7)		GD		17.0		1/fs
Group Delay Distortion		ΔGD		0		μs
ADC Digital Filter (HPF):						
Frequency Response (Note 6)	-3dB	FR		3.4		Hz
	-0.5dB			10		Hz
	-0.1dB			22		Hz
DAC Digital Filter:						
Passband (Note 6)	±0.1dB	PB	0		20.0	kHz
	-6.0dB			22.05		kHz
Stopband (Note 6)		SB	24.1			kHz
Passband Ripple		PR			±0.06	dB
Stopband Attenuation		SA	43			dB
Group Delay (Note 7)		GD		15.4		1/fs
Group Delay Distortion		ΔGD		0		μs
DAC Digital Filter + Analog Filter						
Frequency Response 0 ~ 20.0kHz		FR		±0.5		dB
~ 40.0kHz (Note 8)				±1.0		dB

Note: 6. The passband and stopband frequencies scale with fs (sampling frequency).
For examples, PB=20.0kHz(@ADC: -1.0dB, DAC: -0.1dB) are 0.454 x fs.

Note: 7. The calculating delay time which occurred by digital filtering. This time is from the input of analog signal to setting the 24bit data of both channels to the output register for ADC. For DAC, this time is from setting the 24bit data of both channels on input register to the output of analog signal.

Note: 8. fs=96kHz.

DC CHARACTERISTICS

(Ta=25°C; VA, VD=2.4 ~ 4.0V)

Parameter	Symbol	min	typ	max	Units
High-Level Input Voltage	VIH	70%VD	-	-	V
Low-Level Input Voltage	VIL	-	-	30%VD	V
High-Level Output Voltage (Iout=-20μA)	VOH	VD-0.1	-	-	V
Low-Level Output Voltage (Iout=20μA)	VOL	-	-	0.1	V
Input Leakage Current	Iin	-	-	± 10	μA

SWITCHING CHARACTERISTICS

(Ta=25°C; VA, VD=2.4 ~ 4.0V; C_L=20pF)

Parameter	Symbol	min	typ	max	Units
Master Clock Timing					
Frequency	fCLK	2.048		38.4	MHz
Pulse Width Low	tCLKL	10			ns
Pulse Width High	tCLKH	10			ns
LRCK Frequency					
Normal Speed	fsn	8		50	kHz
Double Speed	fsd	50		100	kHz
Quad Speed	fsq	100		200	kHz
Duty Cycle	Duty	45		55	%
Serial Interface Timing					
BCLK Period					
Normal Speed	tBCK	1/96fsn			ns
Double Speed	tBCK	1/64fsd			ns
Quad Speed	tBCK	1/64fsq			ns
BCLK Pulse Width Low	tBCKL	33			ns
Pulse Width High	tBCKH	33			ns
LRCK Edge to BCLK "↑" (Note 9)	tLRB	20			ns
BCLK "↑" to LRCK Edge (Note 9)	tBLR	20			ns
LRCK Edge to SDTO (MSB)	tDLR			40	ns
BCLK "↓" to SDTO	tDBS			40	ns
SDTI Hold Time	tSDH	20			ns
SDTI Setup Time	tSDS	20			ns
Reset Timing					
PDN Pulse Width	tPW	150			ns
PDN "↑" to SDTO Valid (Note 10)	tPWV		2081		1/fs

Note: 9. BCLK rising edge must not occur at the same time as LRCK edge.

Note: 10. These cycles are the number of LRCK rising from PDN rising.

■ Timing Diagram

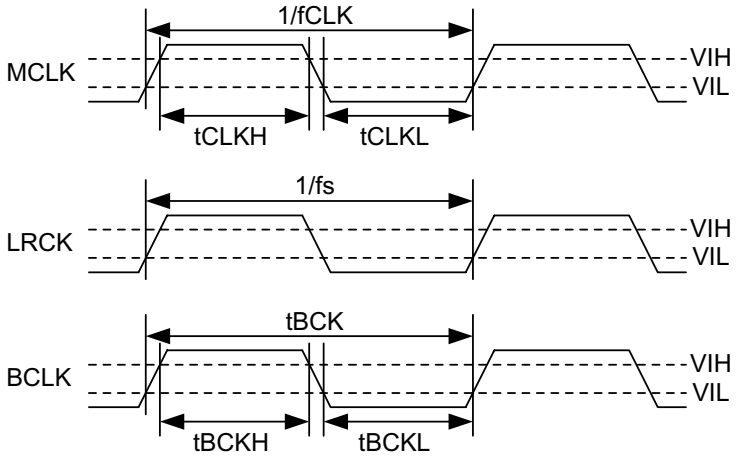


Figure 1. Clock Timing

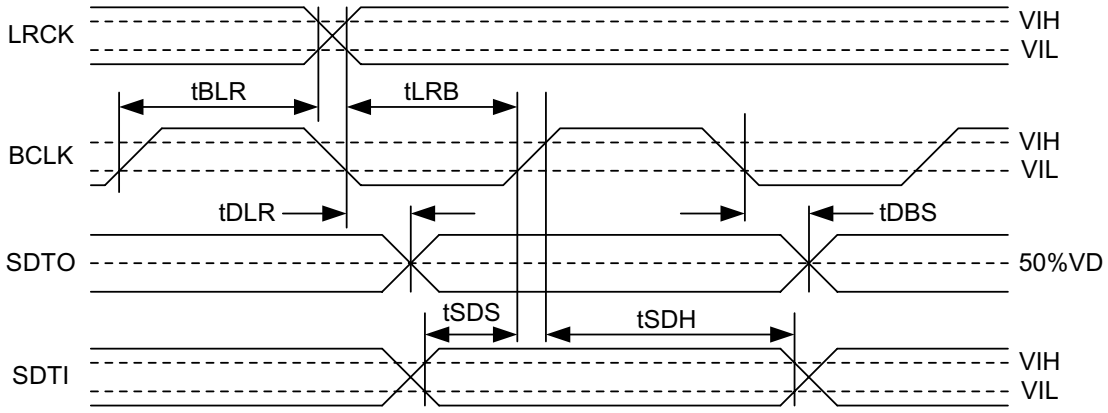


Figure 2. Audio Data Input/Output Timing

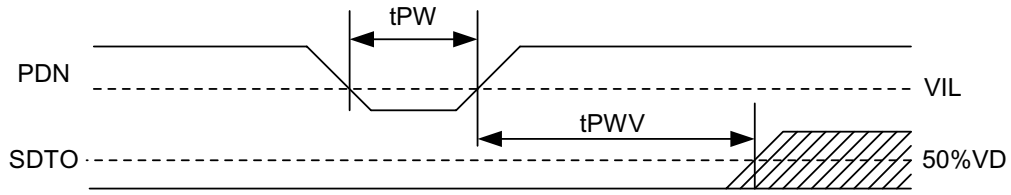


Figure 3. Reset Timing

OPERATION OVERVIEW

■ System Clock Input

The relationship between the clock applied to the MCLK input and sampling rate is defined Table 1. The AK4552 detects the changes of normal speed, double speed and quad speed automatically, ADC and DAC operation in Table 2 are decided by inputted MCLK. In case of double speed, there are normal output and 1/2 decimation output in DAC. Selected 1/2 decimation, ADC outputs "L", but not power-down. In case of 4 times speed, there are 1/2 decimation and 1/4 decimation output in DAC, but not normal output. Selected 1/2 and 1/4 decimation, ADC outputs "L" but not power-down. The LRCK clock input must be synchronized with MCLK, however the phase is not critical. *fs is sampling frequency.

Changed MCLK in operation, the AK4552 need not reset by PDN pin because the AK4552 detects the change of MCLK automatically. But ADC and DAC may occur click noise until the clock is stable. However, if the clock may be stopped when it is changed, the AK4552 is powered down.

All external clocks (MCLK, BCLK, LRCK) must be present unless PDN = "L". If these clocks are not provided, the AK4552 may draw excess current and may not possibly operate properly because the device utilizes dynamic refreshed logic internally.

MCLK	Normal Speed (fs=44.1kHz)	Double Speed (fs=88.2kHz)	Quad Speed (fs=176.4kHz)
64fs	N/A	N/A	11.2896MHz
96fs	N/A	N/A	16.9344MHz
128fs	N/A	11.2896MHz	22.5792MHz
192fs	N/A	16.9344MHz	33.8688MHz
256fs	11.2896MHz	22.5792MHz	N/A
384fs	16.9344MHz	33.8688MHz	N/A
512fs	22.5792MHz	N/A	N/A
768fs	33.8688MHz	N/A	N/A

Table 1. Master Clock Frequency Example

MCLK		Normal Speed	Double Speed	Quad Speed
64fs	ADC	N/A	N/A	"L" Output
	DAC	N/A	N/A	1/4 Decimation
96fs	ADC	N/A	N/A	"L" Output
	DAC	N/A	N/A	1/4 Decimation
128fs	ADC	N/A	"L" Output	"L" Output
	DAC	N/A	1/2 Decimation	1/2 Decimation
192fs	ADC	N/A	"L" Output	"L" Output
	DAC	N/A	1/2 Decimation	1/2 Decimation
256fs	ADC	O	O	N/A
	DAC	O	O	N/A
384fs	ADC	O	O	N/A
	DAC	O	O	N/A
512fs	ADC	O	N/A	N/A
	DAC	O	N/A	N/A
768fs	ADC	O	N/A	N/A
	DAC	O	N/A	N/A

Table 2. Master Clock Frequency & ADC/DAC Operation

* In Table 2, "O" mark is normal output, N/A is "Not Available".

- About the data operation in internal DAC at Decimation

See the Figure 4. The 1/2 decimation takes in one data per 2 periods of LRCK, and the 1/4 decimation takes in one data per 4 periods of LRCK. Therefore, 1/2 decimation outputs a signal which has bandwidth until fs/2, and 1/4 decimation outputs a signal which has bandwidth until fs/4.

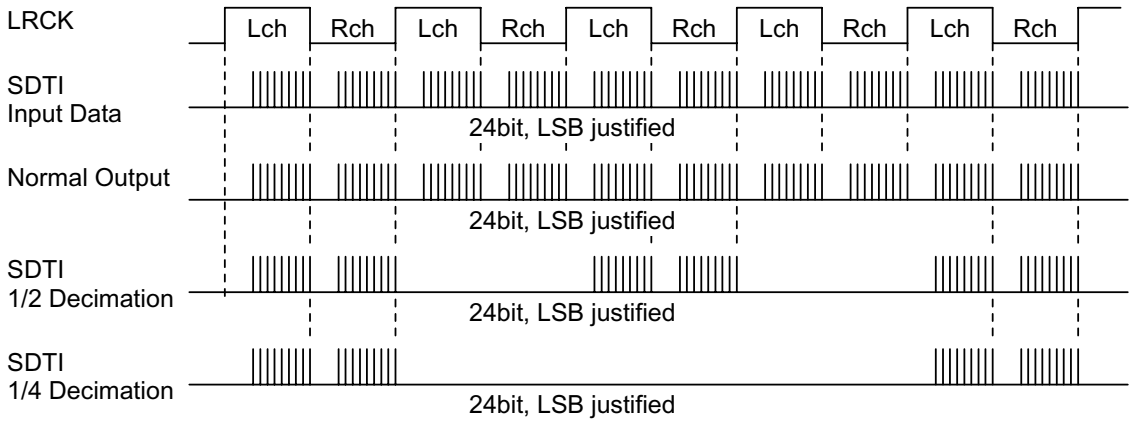


Figure 4. About the data operation in internal DAC at Decimation

■ Audio Serial Interface Format

Data is shifted in/out the SDTI/SDTO pins using BCLK and LRCK inputs. The data is MSB first, 2's compliment.

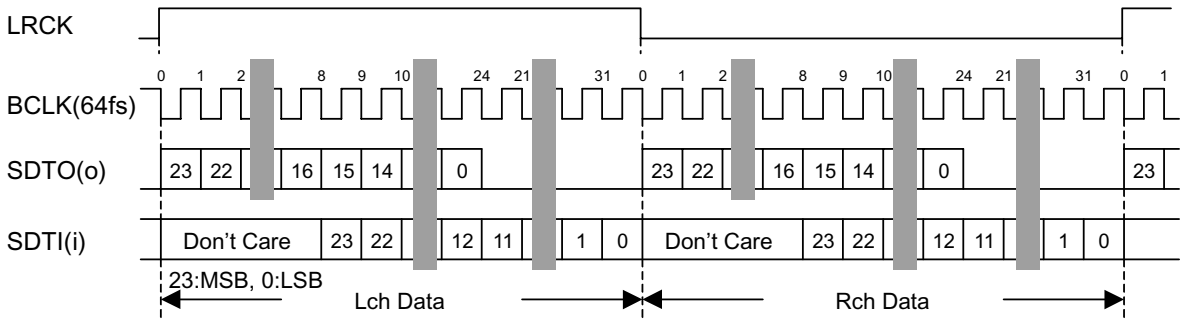


Figure 5. Audio Data I/F Timing

■ De-emphasis Filter

The DAC of AK4552 includes the digital de-emphasis filter (tc=50/15μs) by IIR filter. This filter corresponds to three frequencies (32kHz, 44.1kHz, 48kHz). The de-emphasis filter selected by DEM0 and DEM1 is enabled for input audio data. The de-emphasis is also disabled at DEM0="1" and DEM1="0".

DEM1	DEM0	Mode
0	0	44.1kHz
0	1	OFF
1	0	48kHz
1	1	32kHz

Table 3. De-emphasis filter control

■ Digital High Pass Filter

The AK4552 has a Digital High Pass Filter (HPF) for DC-offset cancel. The cut-off frequency of the HPF is 3.4Hz at fs=44.1kHz and the frequency response at 20Hz is -0.12dB. It also scales with the sampling frequency (fs).

■ Power-down & Reset

The ADC and DAC of AK4552 are placed in the power-down mode by bringing power down pin, PDN = "L" and each digital filter is also reset at the same time. These resets should always be done after power-up. In case of the ADC, an anlog initialization cycle starts after exiting the power-down mode. Therefore, the output data, SDTO becomes available after 2081 cycles of LRCK clock. This initialization cycle does not affect the DAC operation. Figure 6 shows the power-up sequence.

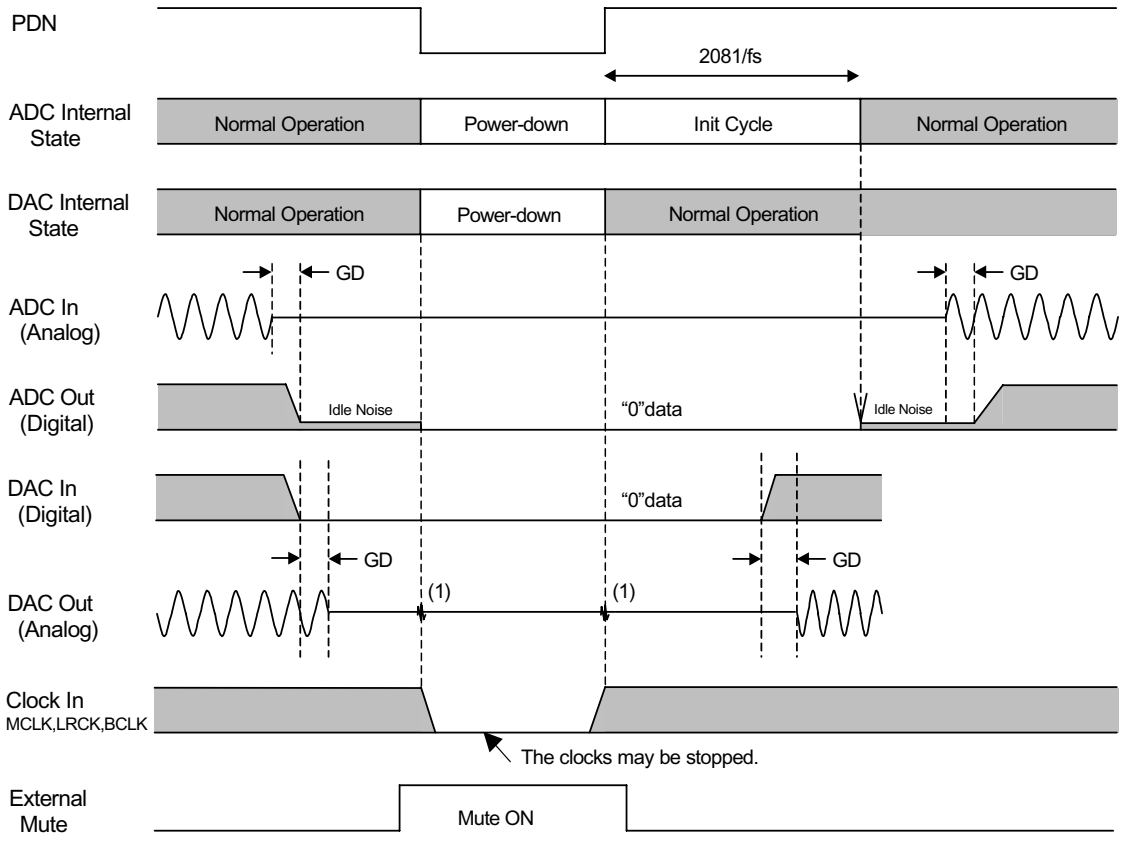


Figure 6. Power-up Sequence

(1) Click noise occurs at the "↑↓" of PDN signal. Please mute the analog output external if the click noise influences system application.

SYSTEM DESIGN

Figure 7 shows the system connection diagram. An evaluation board [AKD4552] is available which demonstrates application circuit, optimum layout, power supply arrangements and measurement results.

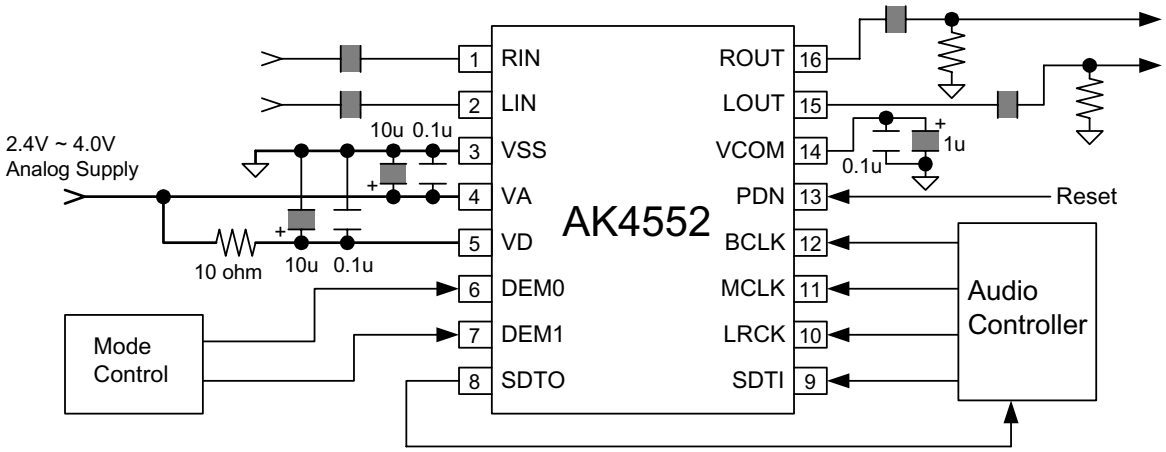


Figure 7. System Connection Diagram Example

Notes:
- When LOUT/ROUT drives some capacitive load, some resistor should be added in series between LOUT/ROUT and capacitive load.
- Electrolytic capacitor value of VCOM depends on low frequency noise of supply voltage.

1. Grounding and Power Supply Decoupling

The AK4552 requires careful attention to power supply and grounding arrangements. VA and VD are usually supplied from analog supply in system. Alternatively if VA and VD are supplied separately, the power up sequence is not critical. VSS of the AK4552 should be connected to analog ground plane. System analog ground and digital ground should be connected together near to where the supplies are brought onto the printed circuit board. Decoupling capacitors should be as near to the AK4552 as possible, with the small value ceramic capacitor being the nearest.

2. Voltage Reference

The input to VA voltage sets the analog input/output range. A 0.1μF ceramic capacitor and a 10μF electrolytic capacitor is connected to VA and VSS pins, normally. VCOM is a signal ground of this chip. An electrolytic less than 1μF (typ; max: 2.2μF) in parallel with a 0.1μF ceramic capacitor attached to these pins eliminates the effects of high frequency noise. No load current may be drawn from VCOM pin. All signals, especially clock, should be kept away from the VA, VD and VCOM pins in order to avoid unwanted coupling into the AK4552.

3. Analog Inputs

ADC inputs are single-ended and internally biased to VCOM. The input signal range scales with the supply voltage and nominally 0.617 x VA Vpp (typ). The ADC output data format 2's compliment. The output code is 7FFFFFH(@24bit) for input above a positive full scale and 800000H(@24bit) for input below a negative full scale. The ideal code is 000000H(@24bit) with no input signal.

The AK4552 samples the analog inputs at 64fs. The digital filter rejects noise above the stop band except for multiples of 64fs. A simple RC filter may be used to attenuate any noise around 64fs and most audio signals do not have significant energy at 64fs.

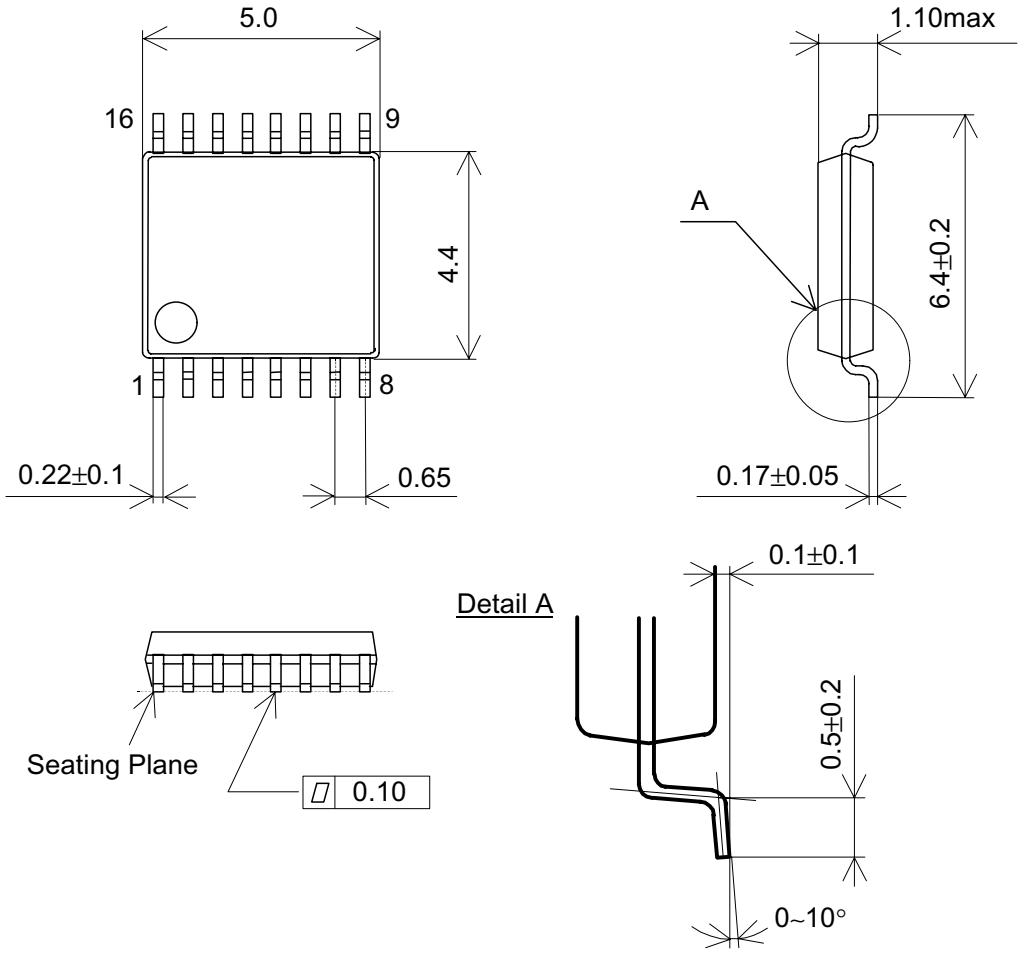
4. Analog Outputs

The analog outputs are also single-ended and centered around the VCOM voltage. The input signal range scales with the supply voltage and nominally 0.583 x VA Vpp (typ). The DAC input data format is 2's compliment. The output voltage is a positive full scale for 7FFFFFH(@24bit) and a negative full scale for 800000H(@24bit). The ideal output is VCOM voltage for 000000H(@24bit). If the noise generated by the delta-sigma modulator beyond the audio band would be the problem, the attenuation by external filter is required.

DC offsets on analog outputs are eliminated by AC coupling since DAC outputs have DC offsets of a few mV.

PACKAGE

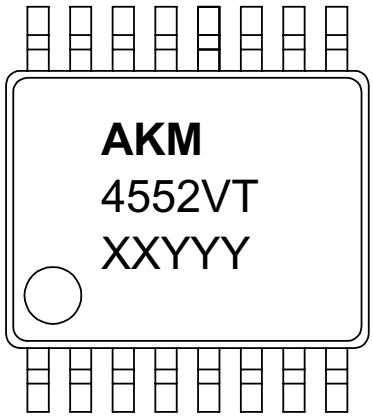
16pin TSSOP (Unit: mm)



■ **Package & Lead frame material**

Package molding compound:	Epoxy
Lead frame material:	Cu
Lead frame surface treatment:	Solder plate

MARKING



1) Pin #1 indication
2) Date Code : XXYYY (5 digits)
   XX: lot#
   YYY: Date Code
3) Marketing Code : 4552VT
4) Asahi Kasei Logo