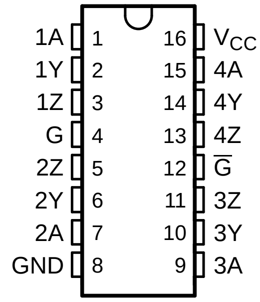
FEATURES

- **Switching Rates up to 32 MHz**
- **Operate From a Single 3.3-V Supply**
- **Propagation Delay Time . . . 8 ns Typ**
- **Pulse Skew Time . . . 500 ps Typ**
- **High Output-Drive Current . . . ±30 mA**
- **Controlled Rise and Fall Times . . . 3 ns Typ**
- **Differential Output Voltage With 100-Ω Load . . . 1.5 V Typ**
- **Ultra-Low Power Dissipation**
  - **dc, 0.3 mW Max**
  - **32 MHz All Channels (No Load), 385 mW Typ**
- **Accept 5-V Logic Inputs With 3.3-V Supply**
- **Low-Voltage Pin-to-Pin Compatible Replacement for AM26C31, AM26LS31, MB571**
- **High Output Impedance in Power-Off Condition**
- **Driver Output Short-Protection Circuit**
- **Package Options Include Plastic Small-Outline (D, NS) Packages**

D OR NS PACKAGE
(TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

The AM26LV31C and AM26LV31I are BiCMOS quadruple differential line drivers with 3-state outputs. They are designed to be similar to TIA/EIA-422-B and ITU Recommendation V.11 drivers with reduced supply-voltage range.

The devices are optimized for balanced-bus transmission at switching rates up to 32 MHz. The outputs have very high current capability for driving balanced lines such as twisted-pair transmission lines and provide a high impedance in the power-off condition. The enable function is common to all four drivers and offers the choice of active-high or active-low enable inputs. The AM26LV31C and AM26LV31I are designed using Texas Instruments proprietary LinIMPACT-C60™ technology, facilitating ultra-low power consumption without sacrificing speed. These devices offer optimum performance when used with the AM26LV32 quadruple line receivers.

The AM26LV31C is characterized for operation from 0°C to 70°C. The AM26LV31I is characterized for operation from –45°C to 85°C

ORDERING INFORMATION

T_A	PACKAGE(1)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	SOIC – D	Tape and reel	AM26LV31CD	AM26LV31C
			AM26LV31CDR	
	SOIC – NS	Tape and reel	AM26LV31CNS	26LV31
			AM26LV31CNSR	
–45°C to 85°C	SOIC – D	Tape and reel	AM26LV31ID	AM26LV31I
			AM26LV31IDR	
	SOIC – NS	Tape and reel	AM26LV31INS	26LV31I
			AM26LV31INSR	

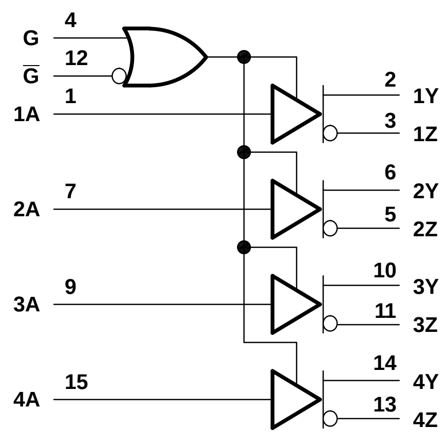
(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE(1)

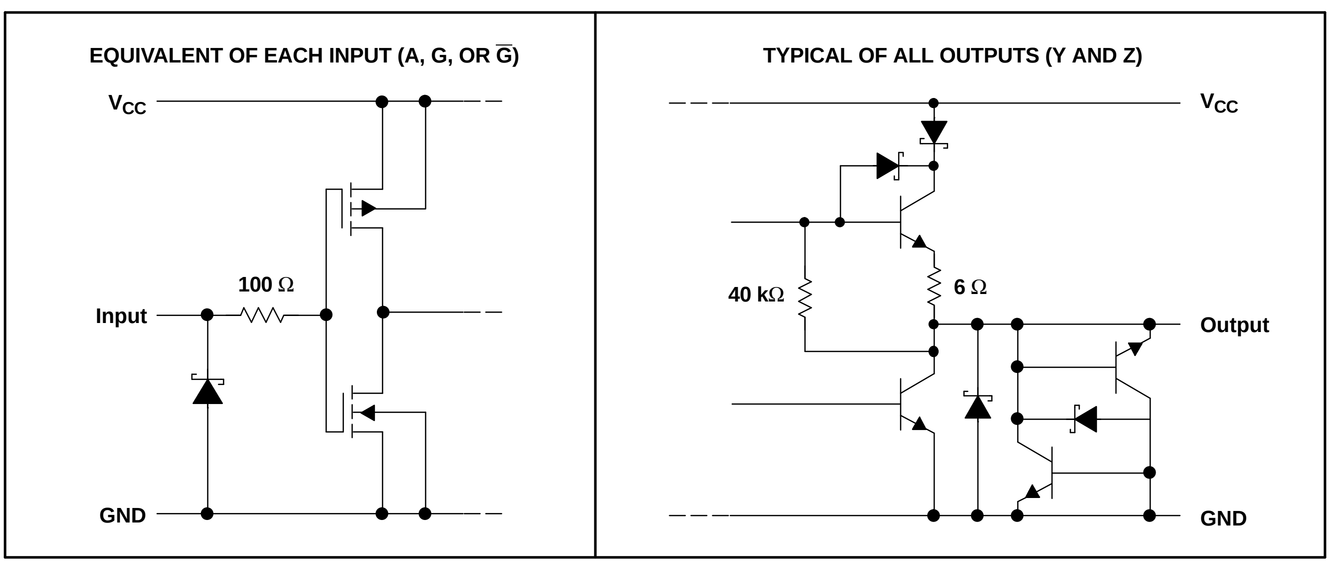
INPUT A	ENABLES		OUTPUTS	
	G	$\overline{G}$	Y	Z
H	H	X	H	L
L	H	X	L	H
H	X	L	H	L
L	X	L	L	H
X	L	H	Z	Z

(1) H = high level, L = low level, X = irrelevant,
Z = high impedance (off)

LOGIC DIAGRAM (POSITIVE LOGIC)



SCHEMATIC (EACH DRIVER)



All resistor values are nominal.

Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range(2)		–0.3	6	V
V_I	Input voltage range		–0.3	6	V
V_O	Output voltage range		–0.3	6	V
θ_{JA}	Package thermal impedance(3)	D package		73	°C/W
		NS package		64	
	Lead temperature	1,6 mm (1/16 in) from case for 10 s		260	°C
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to GND.
(3) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3	3.3	3.6	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current				–30	mA
I_{OL}	Low-level output current				30	mA
T_A	Operating free-air temperature	AM26LV31C	0		70	°C
		AM26LV31I	–45		85	

Electrical Characteristics

over recommended operating supply-voltage and free-air temperature ranges (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = 18 mA				–1.5	V
V_{OH}	High-level output voltage	V_{IH} = 2 V,	I_{OH} = –12 mA	1.85	2.3		V
V_{OL}	Low-level output voltage	V_{IL} = 0.8 V,	I_{OH} = 12 mA		0.8	1.05	V
$\|V_{OD}\|$	Differential output voltage(2)	R_L = 100 Ω		0.95	1.5		V
V_{OC}	Common-mode output voltage			1.3	1.55	1.8	V
$\Delta\|V_{OC}\|$	Change in magnitude of common-mode output voltage(2)					±0.2	V
I_O	Output current with power off	V_O = –0.25 V or 6 V,	V_{CC} = 0			±100	µA
I_{OZ}	Off-state (high-impedance state) output current	V_O = –0.25 V or 6 V,	G = 0.8 V or $\overline{G}$ = 2 V			±100	µA
I_H	High-level input current	V_{CC} = 0 or 3 V,	V_I = 5.5 V			10	µA
I_L	Low-level input current	V_{CC} = 3.6 V,	V_I = 0			–10	µA
I_{OS}	Short-circuit output current	V_{CC} = 3.6 V,	V_O = 0			–200	mA
I_{CC}	Supply current (all drivers)	$V_I = V_{CC}$ or GND,	No load			100	µA
C_{pd}	Power-dissipation capacitance (all drivers)(3)	No load			160		pF

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
(2) $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.
(3) C_{pd} determines the no-load dynamic current consumption. $I_S = C_{pd} \times V_{CC} \times f + I_{CC}$

Switching Characteristics

V_{CC} = 3.3 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP[1]	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	See Figure 2	4	8	12	ns
t_{PHL}	Propagation delay time, high- to low-level output		4	8	12	ns
t_t	Transition time (t_r or t_f)			3		ns
SR	Slew rate, single-ended output voltage	See Note [2] and Figure 2		0.3	1	V/ns
t_{PZH}	Output-enable time to high level	See Figure 3		10	20	ns
t_{PZL}	Output-enable time to low level	See Figure 4		10	20	ns
t_{PHZ}	Output-disable time from high level	See Figure 3		10	20	ns
t_{PLZ}	Output-disable time from low level	See Figure 4		10	20	ns
$t_{sk(p)}$	Pulse skew	f = 32 MHz, See Note [3]		0.5	1.5	ns
$t_{sk(o)}$	Skew limit	f = 32 MHz			1.5	ns
$t_{sk(lim)}$	Skew limit (device to device)	f = 32 MHz, See Note [4]			3	ns

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
(2) Slew rate is defined by:

$$SR = \frac{90\%\left(V_{OH} - V_{OL}\right) - 10\%\left(V_{OH} - V_{OL}\right)}{t_r},$$ the differential slew rate of V_{OD} is $2 \times SR$.

(3) Pulse skew is defined as the $|t_{PLH} - t_{PHL}|$ of each channel of the same device.
(4) Skew limit (device to device) is the maximum difference in propagation delay times between any two channels of any two devices.

PARAMETER MEASUREMENT INFORMATION

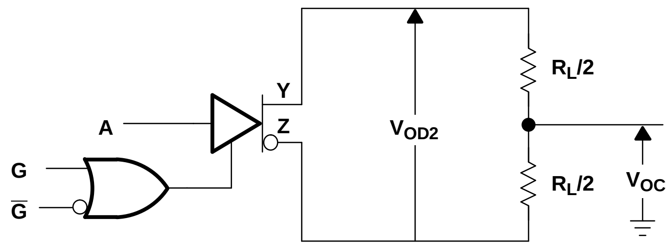
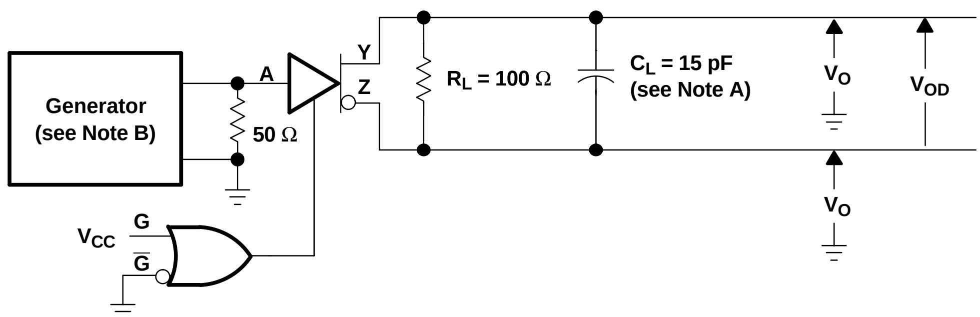
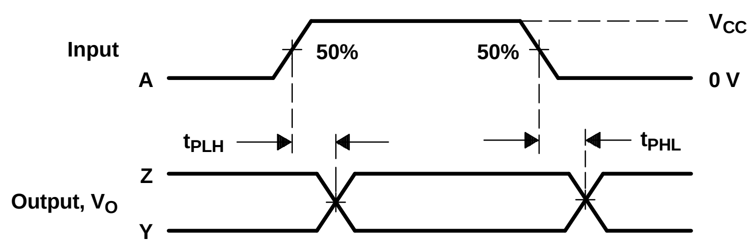


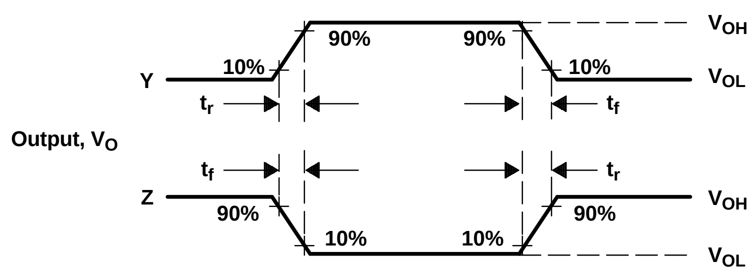
Figure 1. Differential and Common-Mode Output Voltages



TEST CIRCUIT



PROPAGATION DELAY TIMES



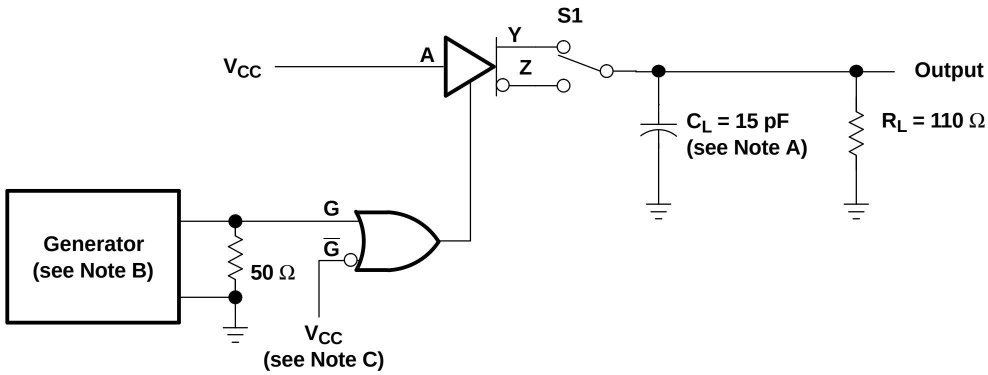
RISE AND FALL TIMES

NOTES: A. C_L includes probe and jig capacitance.

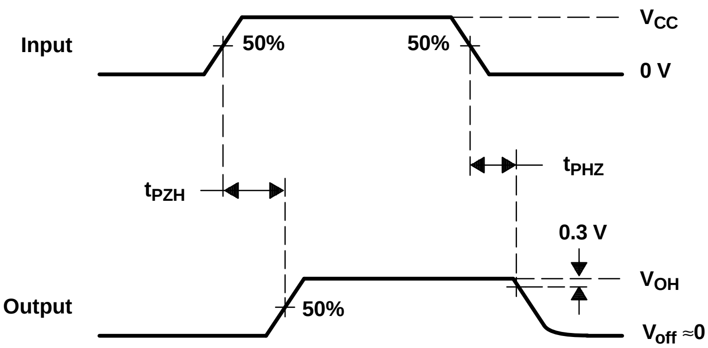
B. The input pulse is supplied by a generator having the following characteristics: PRR = 32 MHz, $Z_O \approx 50\ \Omega$, 50% duty cycle, t_r and $t_f \leq 2$ ns.

Figure 2. Test Circuit and Voltage Waveforms, t_{PHL} and t_{PLH}

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

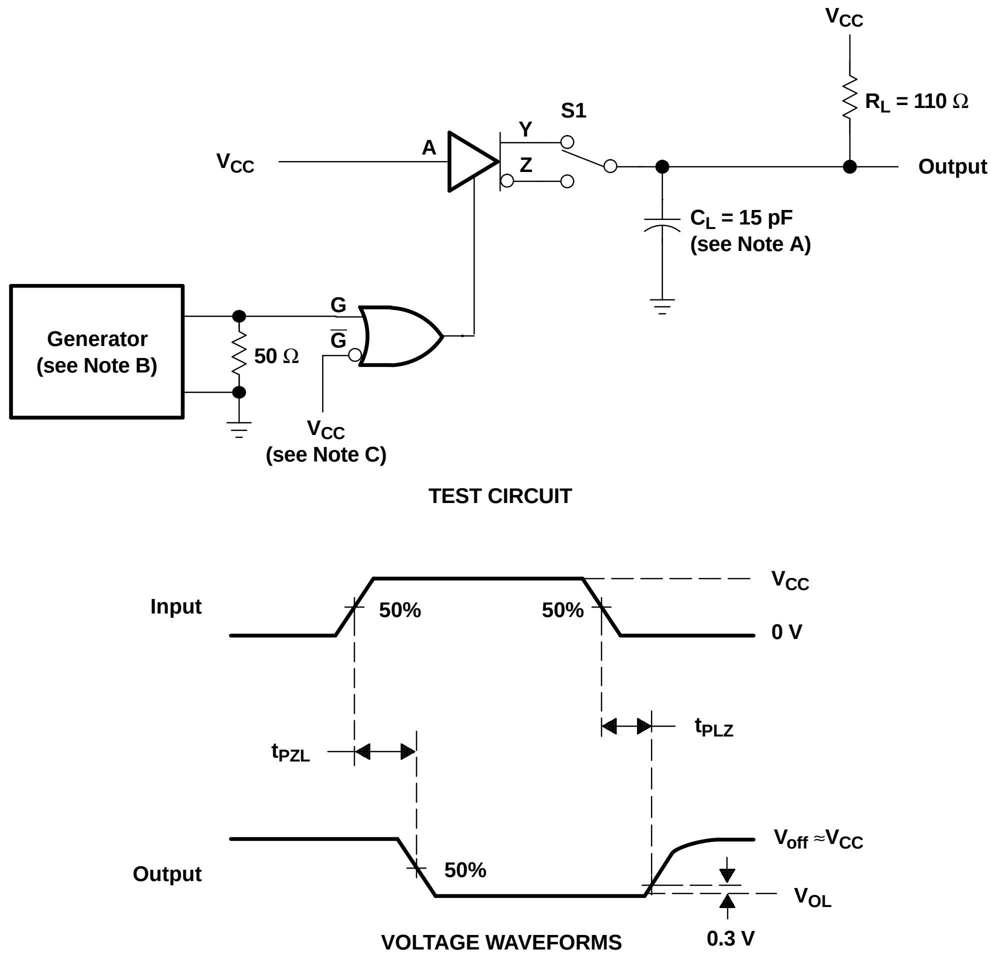


VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, Z_O = 50 Ω, 50% duty cycle, t_r and t_f (10% to 90%) ≤ 2 ns.
C. To test the active-low enable $\overline{G}$, ground G and apply an inverted waveform to $\overline{G}$.

Figure 3. Test Circuit and Voltage Waveforms, t_{PZH} and t_{PHZ}

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, Z_O = 50 Ω, 50% duty cycle, t_r and t_f (10% to 90%) ≤ 2 ns.
C. To test the active-low enable $\overline{G}$, ground G and apply an inverted waveform to $\overline{G}$.

Figure 4. Test Circuit and Voltage Waveforms, t_{PZL} and t_{PLZ}

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
AM26LV31CD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
AM26LV31CDE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
AM26LV31CDG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
AM26LV31CDR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
AM26LV31CDRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
AM26LV31CDRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
AM26LV31CNSLE	OBSOLETE	SO	NS	16		TBD	Call TI	Call TI
AM26LV31CNSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
AM26LV31CNSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
AM26LV31CNSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
AM26LV31ID	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
AM26LV31IDE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
AM26LV31IDG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
AM26LV31IDR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
AM26LV31IDRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
AM26LV31IDRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
AM26LV31INSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
AM26LV31INSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
AM26LV31INSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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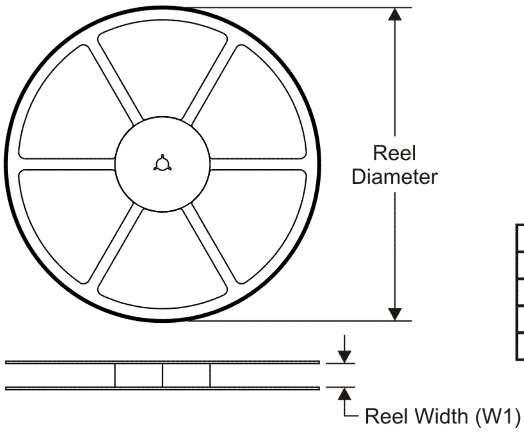
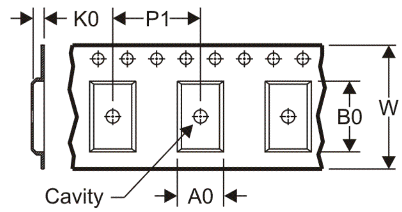
TAPE AND REEL INFORMATION

REEL DIMENSIONS

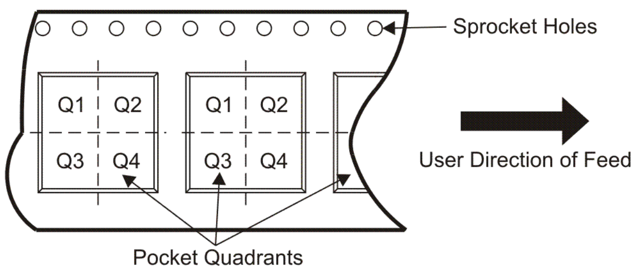


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

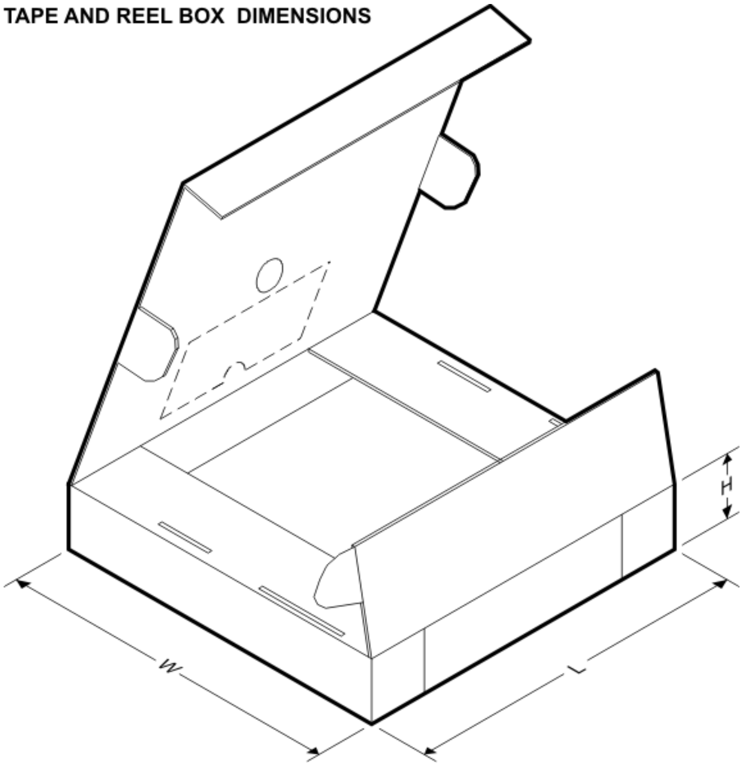
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
AM26LV31CDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
AM26LV31CNSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
AM26LV31IDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
AM26LV31INSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

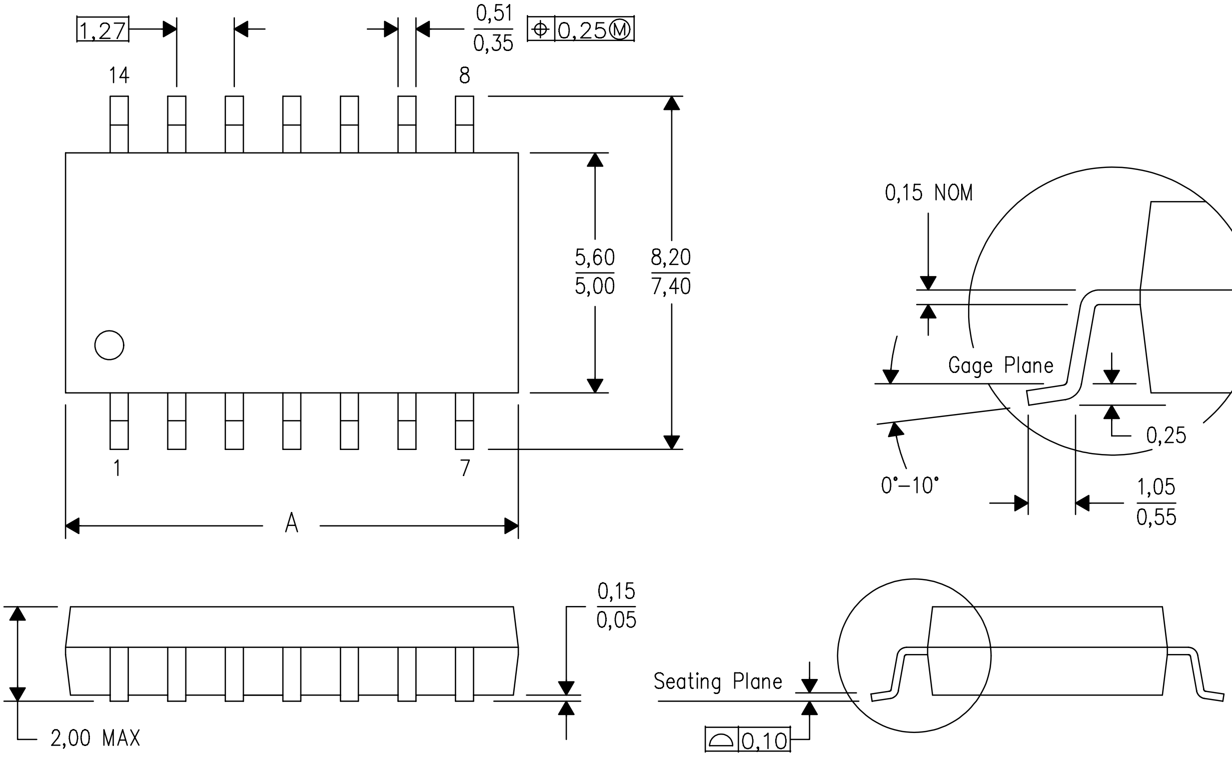


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
AM26LV31CDR	SOIC	D	16	2500	333.2	345.9	28.6
AM26LV31CNSR	SO	NS	16	2000	346.0	346.0	33.0
AM26LV31IDR	SOIC	D	16	2500	333.2	345.9	28.6
AM26LV31INSR	SO	NS	16	2000	346.0	346.0	33.0

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN

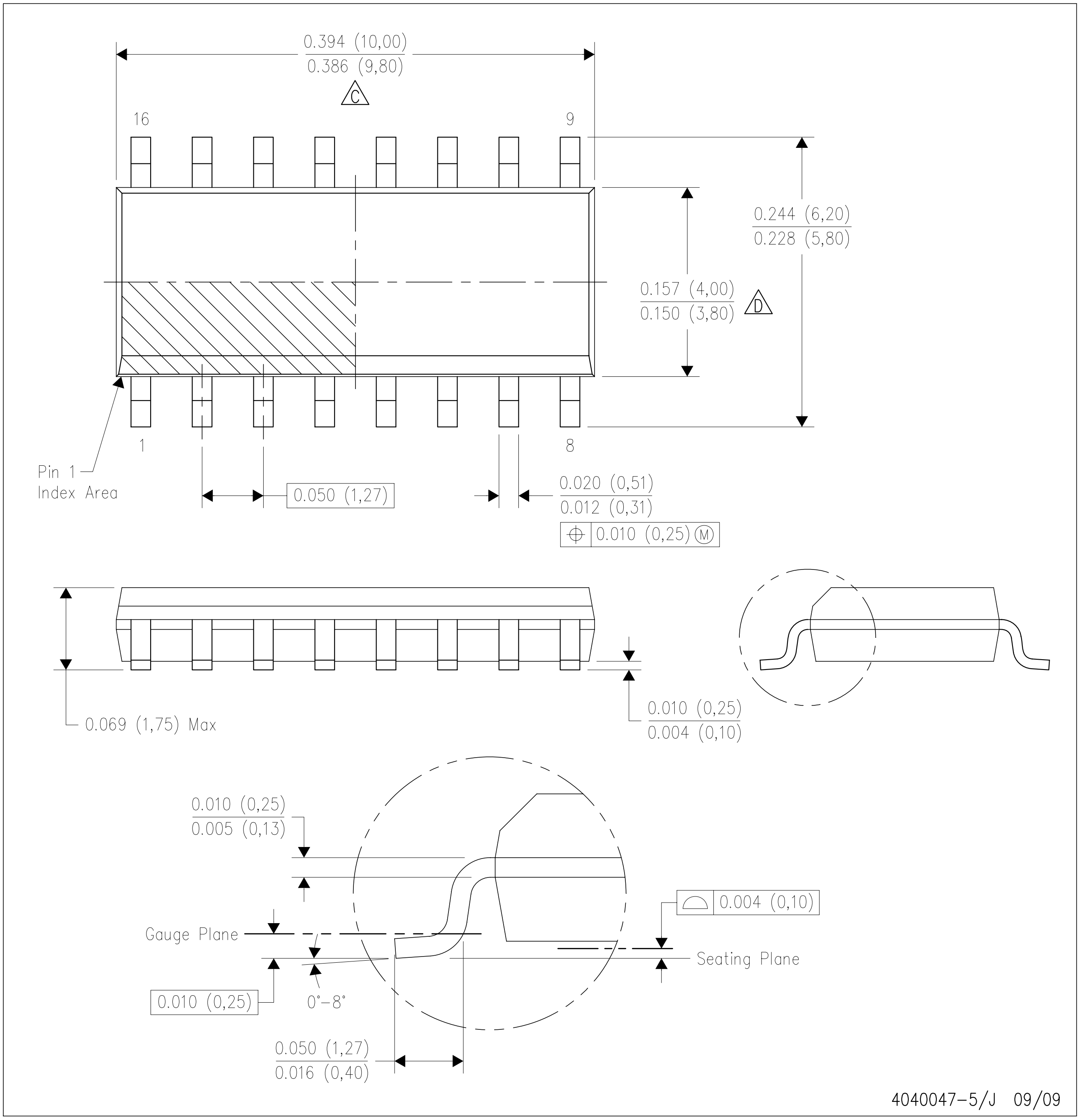


DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

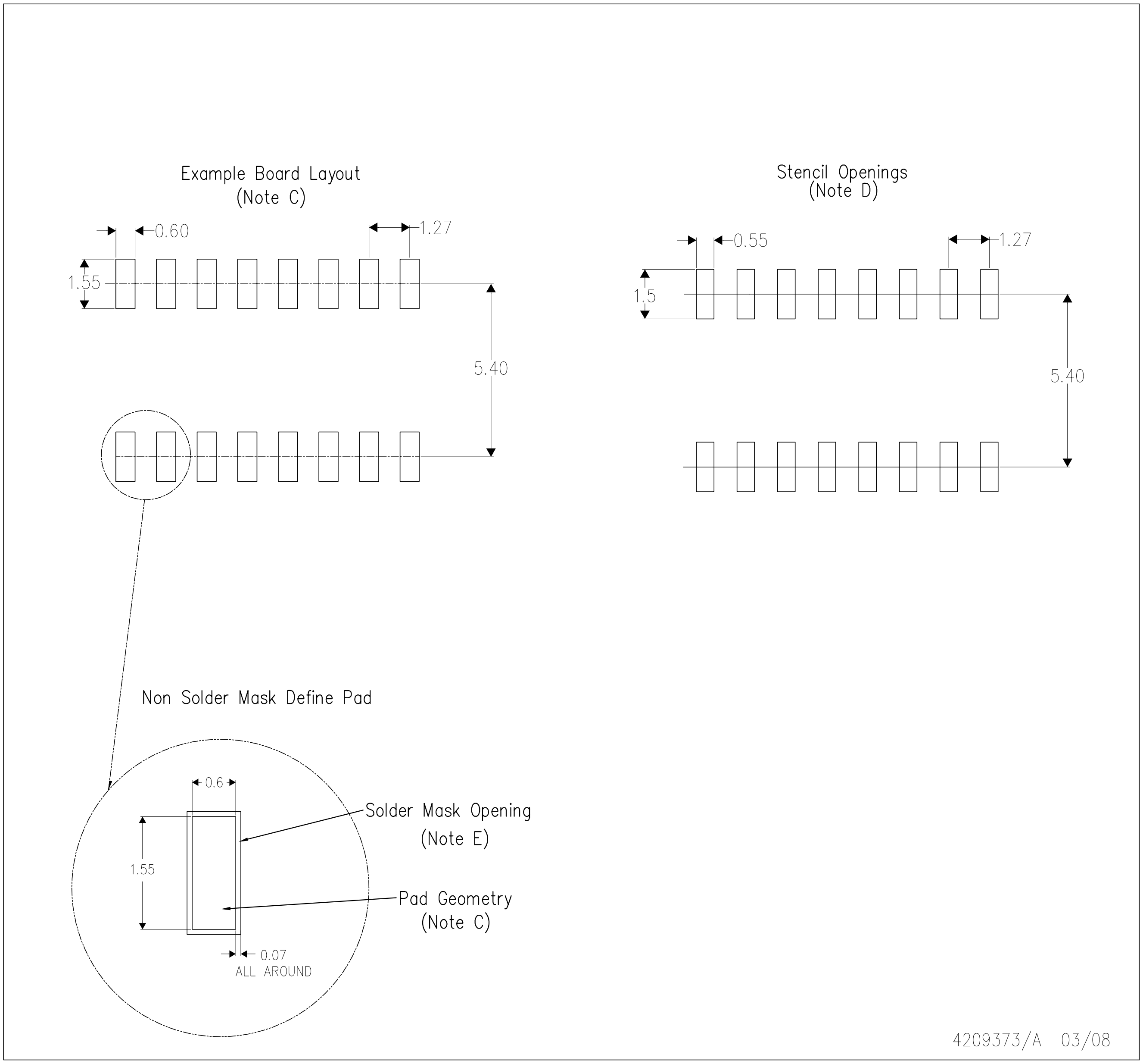
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

D (R–PDSO–G16) PLASTIC SMALL–OUTLINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
E. Reference JEDEC MS–012 variation AC.

D(R-PDSO-G16)



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Refer to IPC7351 for alternate board design.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.