LP3986 Dual Micropower 150 mA Ultra Low-Dropout CMOS Voltage Regulators in DSBGA Package

Check for Samples: LP3986

FEATURES

- **Miniature 8-I/O DSBGA Package**
- **Stable With 1µF Ceramic and High Quality Tantalum Output Capacitors**
- **Fast Turn-on**
- **Two Independent Regulators**
- **Logic Controlled Enable**
- **Over Current and Thermal Protection**

APPLICATIONS

- **CDMA Cellular Handsets**
- **GSM Cellular Handsets**
- **Portable Information Appliances**
- **Portable Battery Applications**

DESCRIPTION

The LP3986 is a 150 mA dual low dropout regulator designed for portable and wireless applications with demanding performance and board space requirements.

The LP3986 is stable with a small 1 µF ±30% ceramic output capacitor requiring smallest possible board space.

The LP3986's performance is optimized for battery powered systems to deliver ultra low noise, extremely low dropout voltage and low quiescent current independent of load current. Regulator ground current increases very slightly in dropout, further prolonging the battery life. Optional external bypass capacitor reduces the output noise further without slowing down the load transient response. Fast start-up time is achieved by utilizing a speed-up circuit that actively pre-charges the bypass capacitor. Power supply rejection is better than 60 dB at low frequencies and 55 dB at 10 kHz. High power supply rejection is maintained at low input voltage levels common to battery operated circuits.

The LP3986 is available in a DSBGA package. Performance is specified for a −40°C to +125°C temperature range. For single LDO applications, please refer to the LP3985 datasheet.

Table 1. Key Specifications

	VALUE	UNIT
Guaranteed output current per regulator	150	mA
Typical quiescent current when both regulators in shutdown mode	1	nA
Typical dropout voltage at 150 mA output current	60	mV
Typical ground current	115	µA
Typical output noise	40	µV
Fast turn-on circuit	200	µs
Junction temperature	−40 to +125	°C

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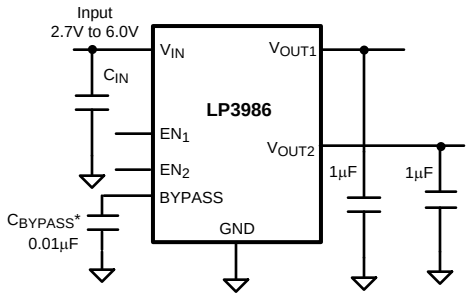
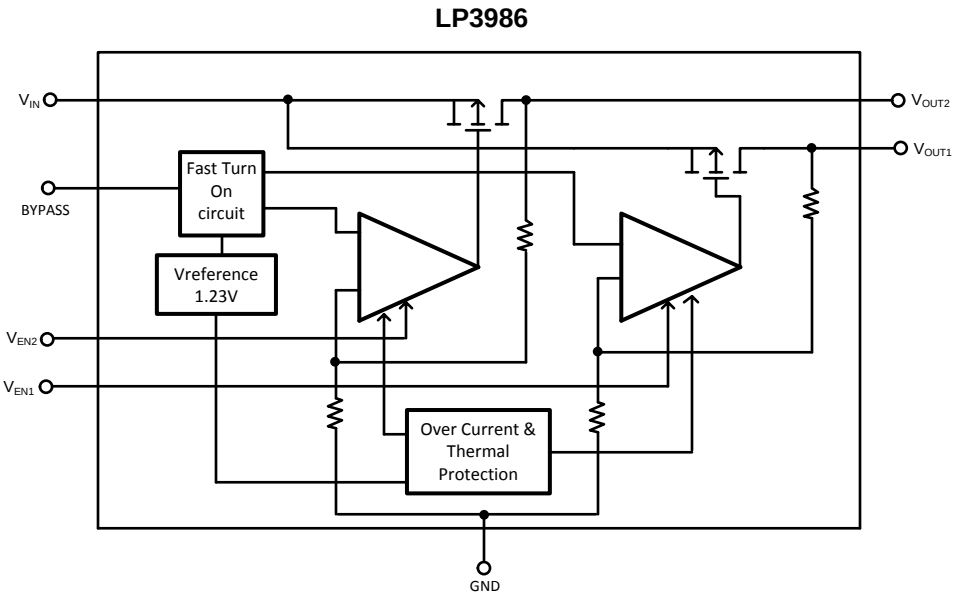
Typical Application Circuit



Block Diagram



Pin Functions

PIN DESCRIPTIONS

Name	DSBGA (1)	Function
V_{OUT2}	A1	Output Voltage of the second LDO
EN_2	B1	Enable input for the second LDO
BYPASS	C1	Bypass capacitor for the bandgap
GND	C2	Common ground
GND	C3	Common ground
EN_1	B3	Enable input for the first LDO
V_{OUT1}	A3	Output Voltage of the first LDO
V_{IN}	A2	Common input for both LDOs

(1) The pin numbering scheme for the DSBGA package was revised in April 2002 to conform to JEDEC standard. Only the pin numbers were revised. No changes to the physical location of the inputs/outputs were made. For reference purposes, the obsolete numbering scheme had V_{OUT2} as pin 1, EN_2 as pin 2, BYPASS as pin 3, GND as pins 4 and 5, EN_1 as pin 6, V_{OUT1} as pin 7, and V_{IN} as pin 8.

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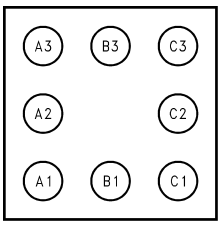
Connection Diagram



8 Bump DSBGA Package – Top View
See Package Number YZR0008

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1) (2) (3)

V_{IN}, V_{EN}	−0.3 to 6.5V
V_{OUT}	−0.3 to (V_{IN}+0.3V) ≤ 6.5V
Junction Temperature	150°C
Storage Temperature	−65°C to +150°C
Pad Temp. (4)	235°C
Maximum Power Dissipation (5)	364mW
ESD Rating (6) Human Body Model Machine Model	 2kV 200V

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is guaranteed. Operating Ratings do not imply guaranteed performance limits. For guaranteed performance limits and associated test conditions, see Electrical Characteristics.
(2) All voltages are with respect to the potential at the GND pin.
(3) **If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office / Distributors for availability and specifications.**
(4) Additional information on pad temperature can be found in TI's AN-1112 application report (SNVA009).
(5) The Absolute Maximum power dissipation depends on the ambient temperature and can be calculated using the formula: $P_D = (T_J - T_A)/\theta_{JA}$,Where T_J is the junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance. The 364mW rating appearing under Absolute Maximum Ratings results from substituting the Absolute Maximum junction temperature, 150°C, for T_J, 70°C for T_A, and 220°C/W for θ_{JA}. More power can be dissipated safely at ambient temperatures below 70°C . Less power can be dissipated safely at ambient temperatures above 70°C. The Absolute Maximum power dissipation can be increased by 4.5mW for each degree below 70°C, and it must be derated by 4.5mW for each degree above 70°C.
(6) The human body model is 100pF discharged through a 1.5kΩ resistor into each pin. The machine model is a 200pF capacitor discharged directly into each pin.

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Operating Ratings (1) (2)

V_{IN}	2.7 to 6V
V_{EN}	0 to (V_{IN}+ 0.3V) ≤ 6V
Junction Temperature	−40°C to +125°C
Thermal Resistance	
θ_{JA}	220°C/W
Maximum Power Dissipation (3)	250mW

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is guaranteed. Operating Ratings do not imply guaranteed performance limits. For guaranteed performance limits and associated test conditions, see Electrical Characteristics.
(2) All voltages are with respect to the potential at the GND pin.
(3) Like the Absolute Maximum power dissipation, the maximum power dissipation for operation depends on the ambient temperature. The 250mW rating appearing under Operating Ratings results from substituting the maximum junction temperature for operation, 125°C, for T_J, 70°C for T_A, and 220°C/W for θ_{JA} into (1) above. More power can be dissipated at ambient temperatures below 70°C . Less power can be dissipated at ambient temperatures above 70°C. The maximum power dissipation for operation can be increased by 4.5mW for each degree below 70°C, and it must be derated by 4.5mW for each degree above 70°C.

Electrical Characteristics

Unless otherwise specified: $V_{IN} = V_{OUT(nom)} + 0.5V$, C_{IN} = 1 µF, I_{OUT} = 1mA, C_{OUT} = 1 µF, C_{BYPASS} = 0.01µF. Typical values and limits appearing in standard typeface are for T_J = 25°C. Limits appearing in **boldface type** apply over the entire junction temperature range for operation, −40°C to +125°C. (1) (2)

Symbol	Parameter	Conditions	Typ	Limit		Units
				Min	Max	
ΔV_{OUT}	Output Voltage Tolerance	I_{OUT} = 1mA		−2.5 **−3.0**	2.5 **3.0**	% of $V_{OUT(nom)}$
	Line Regulation Error(3)	V_{IN} = ($V_{OUT(nom)}$ + 0.5V) to 6.0V, I_{OUT} = 1 mA	0.006		0.092 **0.128**	%/V
	Load Regulation Error(4)	I_{OUT} = 1mA to 150 mA	0.003		0.006 **0.01**	%/mA
	Output AC Line Regulation	V_{IN} = $V_{OUT(nom)}$ + 1V, I_{OUT} = 150 mA (Figure 1)	1.5			mV_{P-P}
PSRR	Power Supply Rejection Ratio	V_{IN} = 3.1V, f = 1 kHz, I_{OUT} = 50 mA (Figure 2)	60			dB
		V_{IN} = 3.1V, f = 10 kHz, I_{OUT} = 50 mA (Figure 2)	50			
I_Q	Quiescent Current	Both Regulators ON V_{EN} = 1.4V, I_{OUT} = 0 mA	115		**200**	µA
		Both Regulators ON V_{EN} = 1.4V, I_{OUT} = 0 to 150 mA	220		**320**	
		One Regulator ON V_{EN} = 1.4V I_{OUT} = 0 mA	75		**130**	
		One Regulator ON V_{EN} = 1.4V I_{OUT} = 0 to 150 mA	130		**200**	
		V_{EN} = 0.4V, Both Regulators OFF (shutdown)	0.001		2 **4**	
	Dropout Voltage(5)	I_{OUT} = 1 mA I_{OUT} = 150 mA	0.4 60		**2** **100**	mV
I_{SC}	Short Circuit Current Limit	Output Grounded	600			mA

(1) All limits are guaranteed. All electrical characteristics having room temperature limits are tested during production with T_J = 25°C or correlated using Statistical Quality Control (SQC) methods. All hot and cold limits are guaranteed by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(2) The target output voltage, which is labeled $V_{OUT(nom)}$, is the desired voltage option.
(3) The output voltage changes slightly with line voltage. An increase in the line voltage results in a slight increase in the output voltage and vice versa.
(4) The output voltage changes slightly with load current. An increase in the load current results in a slight decrease in the output voltage and vice versa. Tested limit applies to Vout 's of 2.5V and greater.
(5) Dropout voltage is the input-to-output voltage difference at which the output voltage is 100mV below its nominal value.

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Electrical Characteristics (continued)

Unless otherwise specified: $V_{IN} = V_{OUT(nom)} + 0.5V$, $C_{IN} = 1\ \mu F$, $I_{OUT} = 1mA$, $C_{OUT} = 1\ \mu F$, $C_{BYPASS} = 0.01\mu F$. Typical values and limits appearing in standard typeface are for $T_J = 25°C$. Limits appearing in **boldface type** apply over the entire junction temperature range for operation, −40°C to +125°C. (1) (2)

Symbol	Parameter	Conditions	Typ	Limit		Units
				Min	Max	
$I_{OUT(PK)}$	Peak Output Current (6)	$V_{OUT} \geq V_{OUT(nom)}$ - 5%	500	**300**		mA
T_{ON}	Turn-On Time (7)	C_{BYPASS} = 0.01 µF	200			µs
e_n	Output Noise Voltage	BW = 10 Hz to 100 kHz, C_{OUT} = 1µF	40			µVrms
ρn(1/f)	Output Noise Density	f = 120 Hz, C_{OUT} = 1µF	1			µV/√Hz
I_{EN}	Maximum Input Current at EN	V_{EN} = 0.4 and V_{IN} = 6V	±10			nA
V_{IL}	Maximum Low Level Input Voltage at EN	V_{IN} = 2.7 to 6V			**0.4**	V
V_{IH}	Minimum High Level Input Voltage at EN	V_{IN} = 2.7 to 6V		**1.4**		V
Xtalk	Crosstalk Rejection	ΔI_{Load1} = 150 mA at 1KHz rate ΔI_{Load2} = 1 mA $\Delta V_{OUT2}/\Delta V_{OUT1}$	−60			dB
		ΔI_{Load2} = 150 mA at 1KHz rate ΔI_{Load1} = 1 mA $\Delta V_{OUT2}/\Delta V_{OUT1}$	−60			
C_{IN}	Input capacitance (8)	All V_{OUT} > = 2.5V,		**1**		µF
		If V_{OUT} = 1.8V, V_{IN_MIN}>= 2.9V		**4.7**		µF
C_{OUT}	Capacitance (8)	All V_{OUT} > = 2.5V,		**1**	**22**	µF
		If V_{OUT} = 1.8V, V_{IN_MIN}>= 2.9V		**2.2**	**22**	µF
	ESR	See (9)		**5**	**500**	mΩ

(6) I_{PEAK} guaranteed for Vout 's of 2.5V and greater.
(7) Turn-on time is that between the enable input just exceeding V_{IH} and the output voltage just reaching 95% of its nominal value.
(8) Range of capacitor values for which the device will remain stable. This electrical specification is guaranteed by design.
(9) Range of capacitor ESR values for which the device will remain stable. This electrical specification is guaranteed by design.

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TEST SIGNALS

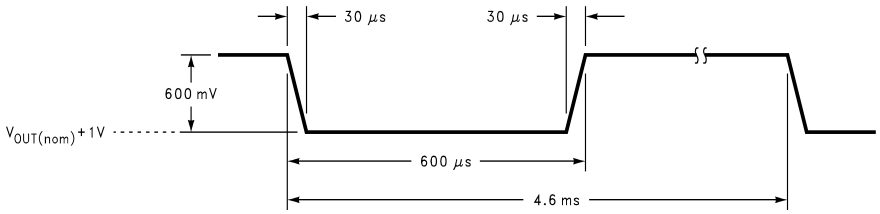

Figure 1. Line Regulation Input Test Signal

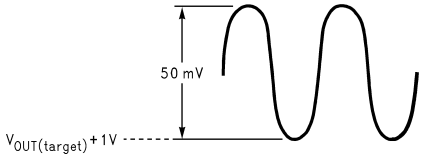

Figure 2. PSRR Input Test Signal

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TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise specified, C_{IN}= C_{OUT} 1µF Ceramic, C_{BP}= 0.01µ F, V_{IN} = V_{OUT} + 0.5, T_A= 25°C, both enable pins are tied to V_{IN}

Power Supply Rejection Ratio (C_{BP} = 0.001µF)

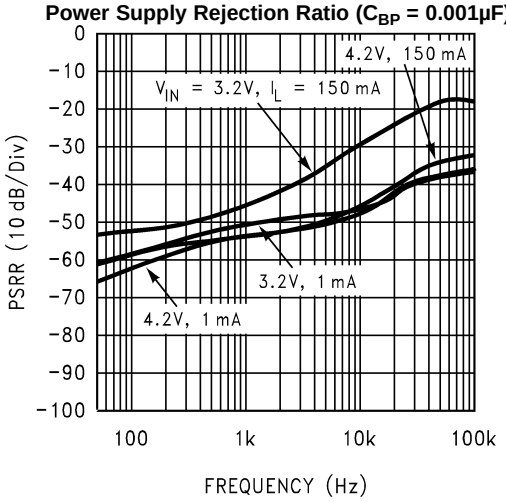

Figure 3.

Power Supply Rejection Ratio (C_{BP} = 0.01µF)

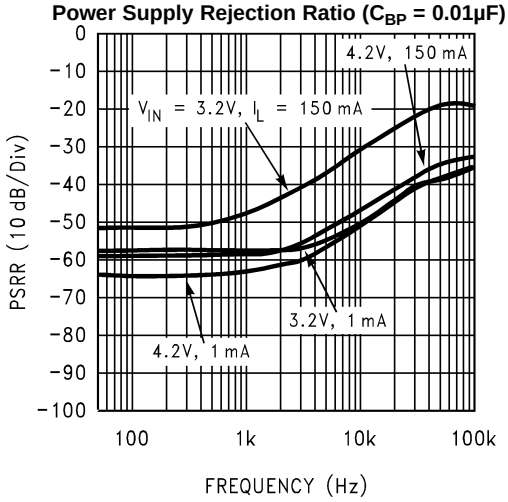

Figure 4.

Power Supply Rejection Ratio (C_{BP} = 0.1µF)

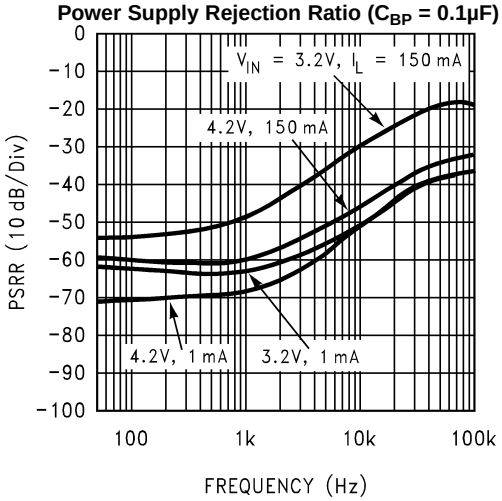

Figure 5.

Output Noise Spectral Density

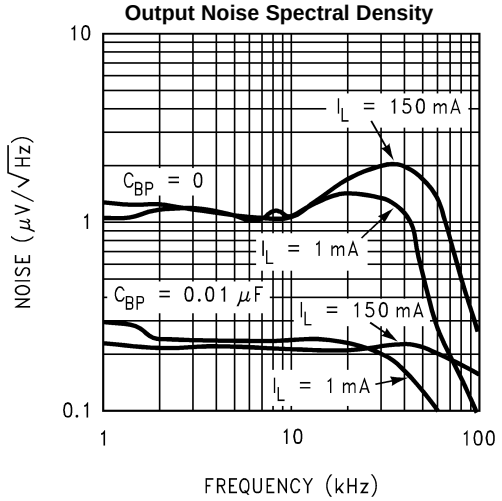

Figure 6.

Line Transient Response (C_{BP} = 0.001µF)

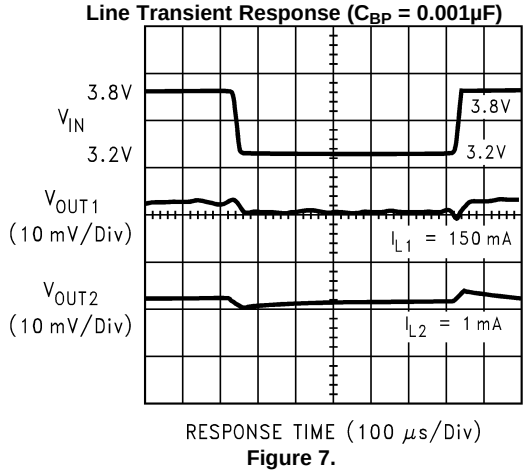

Figure 7.

Line Transient Response (C_{BP} = 0.01µF)

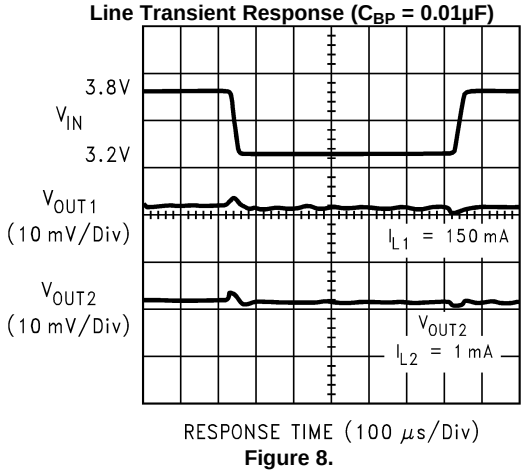

Figure 8.

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TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified, C_{IN}= C_{OUT} 1µF Ceramic, C_{BP}= 0.01µ F, V_{IN} = V_{OUT} + 0.5, T_A= 25°C, both enable pins are tied to V_{IN}

Load Transient & Cross Talk (V_{IN} = V_{OUT} + 0.2V)

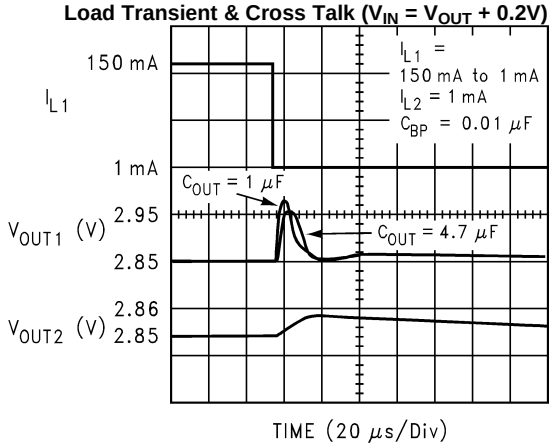

Figure 9.

Load Transient & Cross Talk (V_{IN} = V_{OUT} + 0.2V)

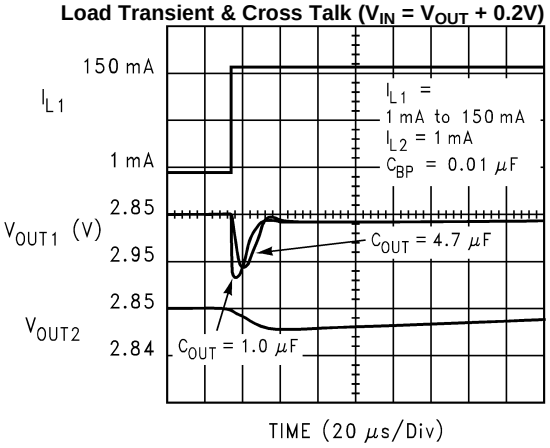

Figure 10.

Start-Up Time (C_{BP} = 0.001, 0.01, 0.1µF)

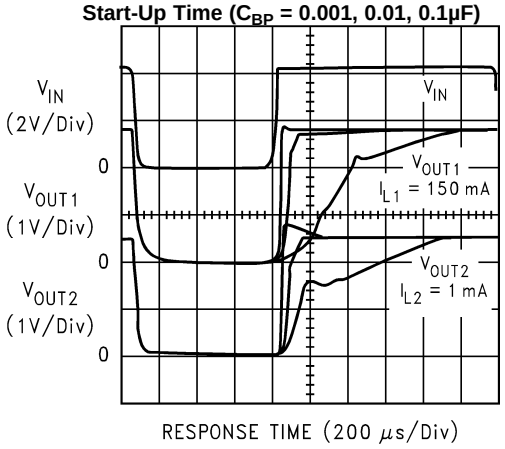

Figure 11.

Enable Response (V_{IN} = 4.2V)

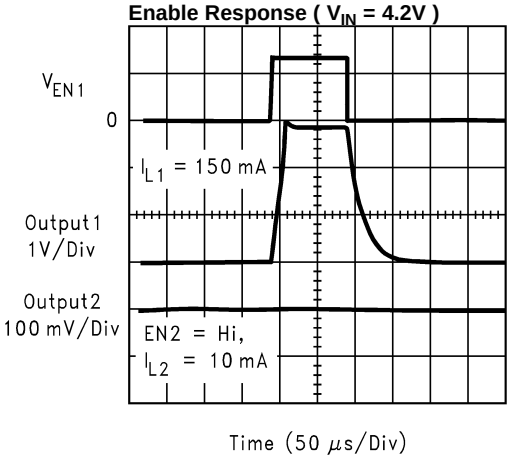

Figure 12.

Enable Response (V_{IN} = V_{OUT}+ 0.2V)

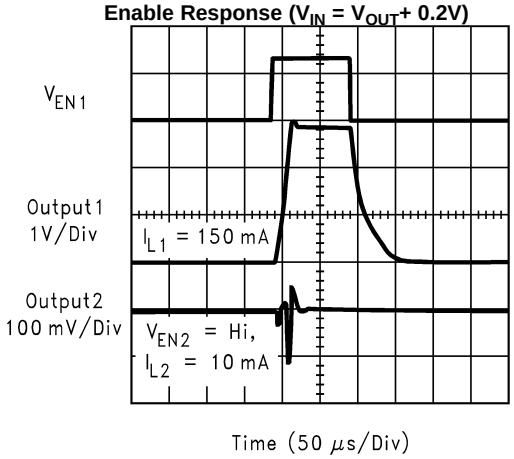

Figure 13.

Enable Response

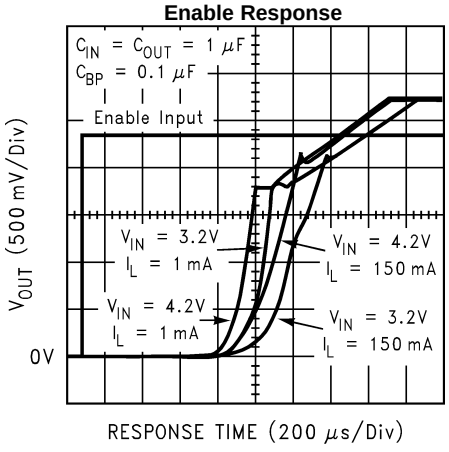

Figure 14.

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TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified, C_{IN}= C_{OUT} 1µF Ceramic, C_{BP}= 0.01µ F, V_{IN} = V_{OUT} + 0.5, T_A= 25°C, both enable pins are tied to V_{IN}

Output Short Circuit Current at V_{IN} = 6V

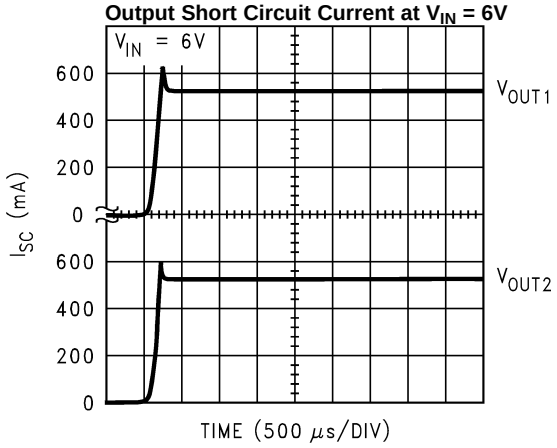

Figure 15.

Output Short Circuit Current at V_{IN} = 3.3V

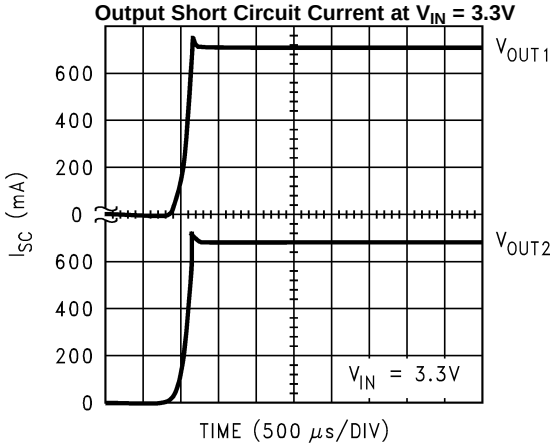

Figure 16.

APPLICATION HINTS

EXTERNAL CAPACITORS

Like any low-dropout regulator, the LP3986 requires external capacitors for regulator stability. The LP3986 is specifically designed for portable applications requiring minimum board space and smallest components. These capacitors must be correctly selected for good performance.

INPUT CAPACITOR

An input capacitance of ≅ 1µF is required between the LP3986 input pin and ground (the amount of the capacitance may be increased without limit).

This capacitor must be located a distance of not more than 1cm from the input pin and returned to a clean analog ground. Any good quality ceramic, tantalum, or film capacitor may be used at the input.

Important: Tantalum capacitors can suffer catastrophic failures due to surge current when connected to a low-impedance source of power (like a battery or a very large capacitor). If a tantalum capacitor is used at the input, it must be guaranteed by the manufacturer to have a surge current rating sufficient for the application.

There are no requirements for the ESR on the input capacitor, but tolerance and temperature coefficient must be considered when selecting the capacitor to ensure the capacitance will be ≅ 1µF over the entire operating temperature range.

OUTPUT CAPACITOR

The LP3986 is designed specifically to work with very small ceramic output capacitors, any ceramic capacitor (temperature characteristics X7R, X5R, Z5U or Y5V) in 1 to 22 µF range with 5mΩ to 500mΩ ESR range is suitable in the LP3986 application circuit.

It may also be possible to use tantalum or film capacitors at the output, but these are not as attractive for reasons of size and cost (see next section Capacitor Characteristics).

The output capacitor must meet the requirement for minimum amount of capacitance and also have an ESR (Equivalent Series Resistance) value which is within a stable range.

NO-LOAD STABILITY

The LP3986 will remain stable and in regulation with no-load (other than the internal voltage divider). This is specially important in CMOS RAM keep-alive applications.

CAPACITOR CHARACTERISTICS

The LP3986 is designed to work with ceramic capacitors on the output to take advantage of the benefits they offer: for capacitance values in the range of 1µF to 4.7µF range, ceramic capacitors are the smallest, least expensive and have the lowest ESR values (which makes them best for eliminating high frequency noise). The ESR of a typical 1µF ceramic capacitor is in the range of 20 mΩ to 40 mΩ, which easily meets the ESR requirement for stability by the LP3986.

The ceramic capacitor's capacitance can vary with temperature. The capacitor type X7R, which operates over a temperature range of -55°C to +125°C, will only vary the capacitance to within ±15%. Most large value ceramic capacitors (≅ 2.2µF) are manufactured with Z5U or Y5V temperature characteristics. Their capacitance can drop by more than 50% as the temperature goes from 25°C to 85°C. Therefore, X7R is recommended over Z5U and Y5 in applications where the ambient temperature will change significantly above or below 25°C.

Tantalum capacitors are less desirable than ceramic for use as output capacitors because they are more expensive when comparing equivalent capacitance and voltage ratings in the 1µF to 4.7µF range.

Another important consideration is that tantalum capacitors have higher ESR values than equivalent size ceramics. This means that while it may be possible to find a tantalum capacitor with an ESR value within the stable range, it would have to be larger in capacitance (which means bigger and more costly) than a ceramic capacitor with the same ESR value. It should also be noted that the ESR of a typical tantalum will increase about 2:1 as the temperature goes from 25°C down to −40°C, so some guard band must be allowed.

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NOISE BYPASS CAPACITOR

Connecting a 0.01µF capacitor between the C_{BYPASS} pin and ground significantly reduces noise on the regulator output. This cap is connected directly to a high impedance node in the band gap reference circuit. Any significant loading on this node will cause a change on the regulated output voltage. For this reason, DC leakage current through this pin must be kept as low as possible for best output voltage accuracy. The use of this 0.01µF bypass capacitor is strongly recommended to prevent overshoot on the output during start up.

The types of capacitors best suited for the noise bypass capacitor are ceramic and film. High-quality ceramic capacitors with either NPO or COG dielectric typically have very low leakage. Polypropolene and polycarbonate film capacitors are available in small surface-mount packages and typically have extremely low leakage current.

Unlike many other LDOs, addition of a noise reduction capacitor does not effect the transient response of the device.

ON/OFF INPUT OPERATION

The LP3986 is turned off by pulling the V_{EN} pin low, and turned on by pulling it high. If this feature is not used, the V_{EN} pin should be tied to V_{IN} to keep the regulator output on at all times. To assure proper operation, the signal source used to drive the V_{EN} input must be able to swing above and below the specified turn-on/off voltage thresholds listed in the Electrical Characteristics section under V_{IL} and V_{IH}.

FAST ON-TIME

The LP3986 outputs are turned on after V_{ref} voltage reaches its final value (1.23V nominal). To speed up this process, the noise reduction capacitor at the bypass pin is charged with an internal 70µA current source. The current source is turned off when the bandgap voltage reaches approximately 95% of its final value. The turn on time is determined by the time constant of the bypass capccitor. The smaller the capacitor value, the shorter the turn on time, but less noise gets reduced. As a result, turn on time and noise reduction need to be taken into design consideration when choosing the value of the bypass capacitor.

DSBGA MOUNTING

The DSBGA package requires specific mounting techniques which are detailed in TI's AN-1112 application report (SNVA009), in particular the section *Surface Mount Assembly Considerations*.

For best results during assembly, alignment ordinals on the PC board may be used to facilitate placement of the DSBGA device.

DSBGA LIGHT SENSITIVITY

Exposing the DSBGA device to direct sunlight will cause misoperation of the device. Light sources such as halogen lamps can effect electrical performance if brought near to the device.

The wavelengths which have most detrimental effect are reds and infra-reds, which means that the fluorescent lighting used inside most buildings has very little effect on performance. A DSBGA test board was brought to within 1cm of a fluorescent desk lamp and the effect on the regulated output voltage was negligible, showing a deviation of less than 0.1% from nominal.

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REVISION HISTORY

Changes from Revision T (February 2013) to Revision U	Page
• Changed layout of National Data Sheet to TI format	11

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LP3986TL-2518/NOPB	Active	Production	DSBGA (YZR) | 8	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-	D 30
LP3986TL-2518/NOPB.A	Active	Production	DSBGA (YZR) | 8	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	D 30
LP3986TL-2525/NOPB	Active	Production	DSBGA (YZR) | 8	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-	D 27
LP3986TL-2525/NOPB.A	Active	Production	DSBGA (YZR) | 8	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	D 27
LP3986TL-2828/NOPB	Active	Production	DSBGA (YZR) | 8	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	D 10
LP3986TL-2828/NOPB.A	Active	Production	DSBGA (YZR) | 8	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	D 10
LP3986TL-3030/NOPB	Active	Production	DSBGA (YZR) | 8	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	D 12
LP3986TL-3030/NOPB.A	Active	Production	DSBGA (YZR) | 8	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	D 12
LP3986TLX285285/NO.A	Active	Production	DSBGA (YZR) | 8	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	D 11
LP3986TLX285285/NOPB	Active	Production	DSBGA (YZR) | 8	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-	D 11

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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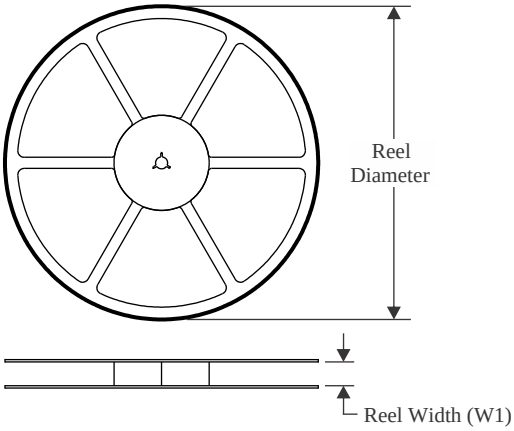
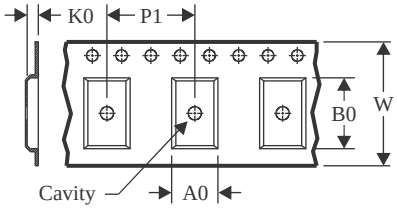
TAPE AND REEL INFORMATION

REEL DIMENSIONS

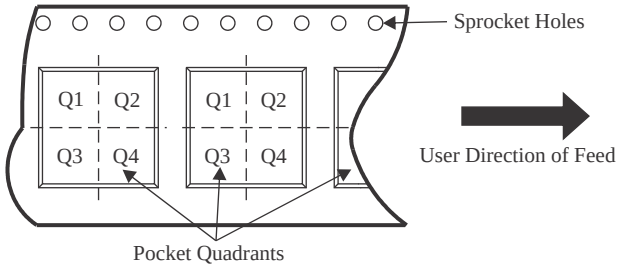


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

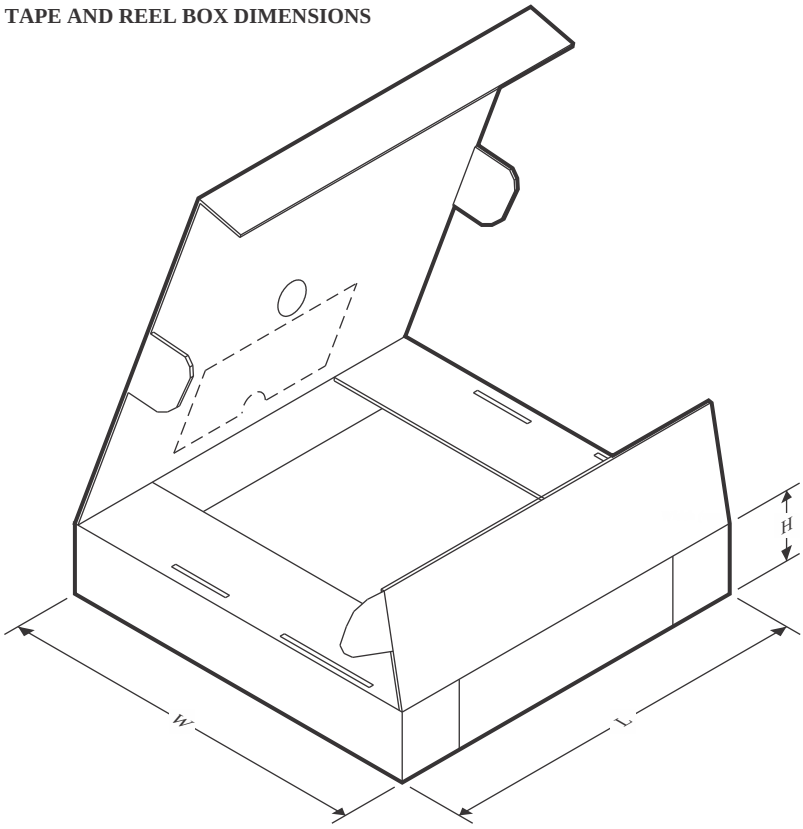
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP3986TL-2518/NOPB	DSBGA	YZR	8	250	178.0	8.4	1.7	1.7	0.76	4.0	8.0	Q1
LP3986TL-2525/NOPB	DSBGA	YZR	8	250	178.0	8.4	1.7	1.7	0.76	4.0	8.0	Q1
LP3986TL-2828/NOPB	DSBGA	YZR	8	250	178.0	8.4	1.7	1.7	0.76	4.0	8.0	Q1
LP3986TL-3030/NOPB	DSBGA	YZR	8	250	178.0	8.4	1.7	1.7	0.76	4.0	8.0	Q1
LP3986TLX285285/NOPB	DSBGA	YZR	8	3000	178.0	8.4	1.7	1.7	0.76	4.0	8.0	Q1

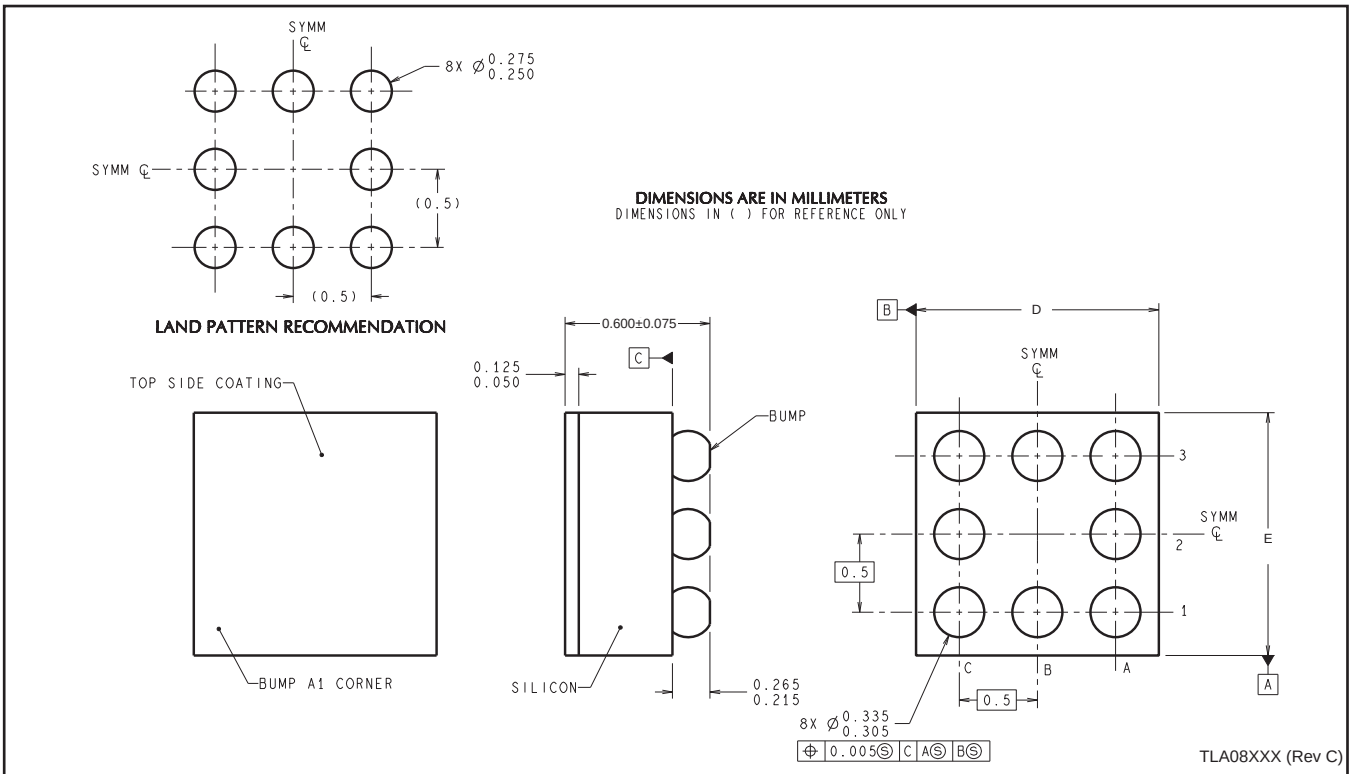
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP3986TL-2518/NOPB	DSBGA	YZR	8	250	208.0	191.0	35.0
LP3986TL-2525/NOPB	DSBGA	YZR	8	250	208.0	191.0	35.0
LP3986TL-2828/NOPB	DSBGA	YZR	8	250	208.0	191.0	35.0
LP3986TL-3030/NOPB	DSBGA	YZR	8	250	208.0	191.0	35.0
LP3986TLX285285/NOPB	DSBGA	YZR	8	3000	208.0	191.0	35.0

YZR0008



D: Max = 1.591 mm, Min = 1.53 mm

E: Max = 1.591 mm, Min = 1.53 mm

4215045/A 12/12

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

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