

OPA241
OPA2241
OPA4241

OPA251
OPA2251
OPA4251

Single-Supply, *MicroPOWER* OPERATIONAL AMPLIFIERS

OPA241 Family optimized for +5V supply.

OPA251 Family optimized for $\pm 15V$ supply.

FEATURES

- **MicroPOWER:** $I_Q = 25\mu A$
- **SINGLE-SUPPLY OPERATION**
- **RAIL-TO-RAIL OUTPUT (within 50mV)**
- **WIDE SUPPLY RANGE**
 - Single Supply: +2.7V to +36V
 - Dual Supply: $\pm 1.35V$ to $\pm 18V$
- **LOW OFFSET VOLTAGE: $\pm 250\mu V$ max**
- **HIGH COMMON-MODE REJECTION: 124dB**
- **HIGH OPEN-LOOP GAIN: 128dB**
- **SINGLE, DUAL, AND QUAD**

APPLICATIONS

- **BATTERY OPERATED INSTRUMENTS**
- **PORTABLE DEVICES**
- **MEDICAL INSTRUMENTS**
- **TEST EQUIPMENT**

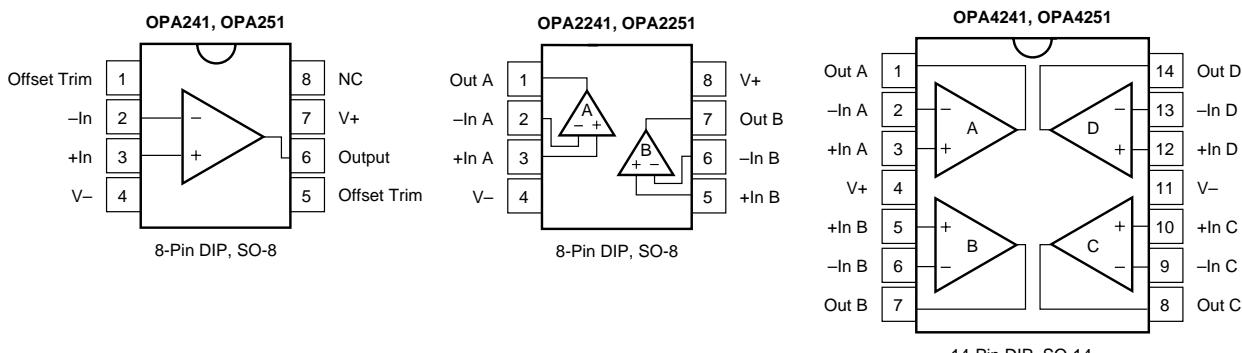
DESCRIPTION

The OPA241 series and OPA251 series are specifically designed for battery powered, portable applications. In addition to very low power consumption ($25\mu A$), these amplifiers feature low offset voltage, rail-to-rail output swing, high common-mode rejection, and high open-loop gain.

The OPA241 series is optimized for operation at low power supply voltage while the OPA251 series is optimized for high power supplies. Both can operate from either single (+2.7V to +36V) or dual supplies ($\pm 1.35V$ to $\pm 18V$). The input common-mode voltage range extends 200mV below the negative supply—ideal for single-supply applications.

They are unity-gain stable and can drive large capacitive loads. Special design considerations assure that these products are easy to use. High performance is maintained as the amplifiers swing to their specified limits. Because the initial offset voltage ($\pm 250\mu V$ max) is so low, user adjustment is usually not required. However, external trim pins are provided for special applications (single versions only).

The OPA241 and OPA251 (single versions) are available in standard 8-pin DIP and SO-8 surface-mount packages. The OPA2241 and OPA2251 (dual versions) come in 8-pin DIP and SO-8 surface-mount packages. The OPA4241 and OPA4251 (quad versions) are available in 14-pin DIP and SO-14 surface-mount packages. All are fully specified from $-40^\circ C$ to $+85^\circ C$ and operate from $-55^\circ C$ to $+125^\circ C$.



SPECIFICATIONS: $V_S = 2.7V$ to $5V$

At $T_A = +25^\circ C$, $R_L = 100k\Omega$ connected to $V_S/2$, unless otherwise noted.
Boldface limits apply over the specified temperature range, $T_A = -40^\circ C$ to $+85^\circ C$.

PARAMETER	CONDITION	OPA241UA, PA OPA2241UA, PA OPA4241UA, PA			OPA251UA, PA OPA2251UA, PA OPA4251UA, PA			UNITS
		MIN	TYP ⁽¹⁾	MAX	MIN	TYP ⁽¹⁾	MAX	
OFFSET VOLTAGE Input Offset Voltage $T_A = -40^\circ C$ to $+85^\circ C$	V_{OS}		± 50 ± 100 ± 0.4	± 250 ± 400 3		± 100 ± 130 ± 0.6		μV μV $\mu V/^\circ C$
vs Temperature vs Power Supply $T_A = -40^\circ C$ to $+85^\circ C$	dV_{OS}/dT PSRR			30 30 0.3		*	*	$\mu V/V$ $\mu V/V$ $\mu V/V$
Channel Separation (dual, quad)						*	*	
INPUT BIAS CURRENT Input Bias Current ⁽²⁾ $T_A = -40^\circ C$ to $+85^\circ C$	I_B			-4	-20 -25	*		nA nA
Input Offset Current $T_A = -40^\circ C$ to $+85^\circ C$	I_{OS}			± 0.1	± 2 ± 2	*		nA nA nA nA
NOISE Input Voltage Noise, $f = 0.1Hz$ to $10Hz$	e_n			1		*		μV_{p-p}
Input Voltage Noise Density, $f = 1kHz$				45		*		nV/\sqrt{Hz}
Current Noise Density, $f = 1kHz$	i_n			40		*		fA/\sqrt{Hz}
INPUT VOLTAGE RANGE Common-Mode Voltage Range Common-Mode Rejection Ratio $T_A = -40^\circ C$ to $+85^\circ C$	V_{CM} CMRR	$V_{CM} = -0.2V$ to $(V+) - 0.8V$ $V_{CM} = 0V$ to $(V+) - 0.8V$	-0.2 80 80	106	(V+) - 0.8	*		V dB dB
INPUT IMPEDANCE Differential Common-Mode					$10^7 \parallel 2$ $10^9 \parallel 4$	*		$\Omega \parallel pF$ $\Omega \parallel pF$
OPEN-LOOP GAIN Open-Loop Voltage Gain $T_A = -40^\circ C$ to $+85^\circ C$	A_{OL}	$R_L = 100k\Omega, V_O = (V-) + 100mV$ to $(V+) - 100mV$ $R_L = 100k\Omega, V_O = (V-) + 100mV$ to $(V+) - 100mV$ $R_L = 10k\Omega, V_O = (V-) + 200mV$ to $(V+) - 200mV$ $R_L = 10k\Omega, V_O = (V-) + 200mV$ to $(V+) - 200mV$	100 100 100 100	120		*		dB dB dB dB
FREQUENCY RESPONSE Gain-Bandwidth Product Slew Rate Overload Recovery Time	GBW SR	$V_S = 5V, G = 1$ $V_{IN} \cdot G = V_S$		35 0.01 60		*		kHz $V/\mu s$ μs
OUTPUT Voltage Output Swing from Rail ⁽³⁾ $T_A = -40^\circ C$ to $+85^\circ C$	V_O	$R_L = 100k\Omega$ to $V_S/2, A_{OL} \geq 70dB$ $R_L = 100k\Omega$ to $V_S/2, A_{OL} \geq 100dB$ $R_L = 100k\Omega$ to $V_S/2, A_{OL} \geq 100dB$ $R_L = 10k\Omega$ to $V_S/2, A_{OL} \geq 100dB$ $R_L = 10k\Omega$ to $V_S/2, A_{OL} \geq 100dB$		50 75 100 100 200	100	*		mV mV mV mV mV
$T_A = -40^\circ C$ to $+85^\circ C$ Short-Circuit Current Single Versions Dual, Quad Versions Capacitive Load Drive	I_{SC}			-24/+4 -30/+4		*		mA mA
	C_{LOAD}			See Typical Curve		*		
POWER SUPPLY Specified Voltage Range Operating Voltage Range Quiescent Current (per amplifier) $T_A = -40^\circ C$ to $+85^\circ C$	V_S I_Q	$T_A = -40^\circ C$ to $+85^\circ C$ $I_Q = 0$ $I_Q = 0$	+2.7 ± 25	+2.7 to +5 ± 30 +36 ± 36	*	*	*	V V μA μA
TEMPERATURE RANGE Specified Range Operating Range Storage Range Thermal Resistance 8-Pin DIP SO-8 Surface Mount 14-Pin DIP SO-14 Surface Mount			-40 -55 -55	+85 +125 +125	*		*	$^\circ C$ $^\circ C$ $^\circ C$ $^\circ C/W$ $^\circ C/W$ $^\circ C/W$ $^\circ C/W$

* Specifications the same as OPA241UA, PA.

NOTES: (1) $V_S = +5V$. (2) The negative sign indicates input bias current flows out of the input terminals. (3) Output voltage swings are measured between the output and power supply rails.

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SPECIFICATIONS: $V_S = \pm 15V$

At $T_A = +25^\circ C$, $R_L = 100k\Omega$ connected to ground, unless otherwise noted.
Boldface limits apply over the specified temperature range, $T_A = -40^\circ C$ to $+85^\circ C$.

PARAMETER	CONDITION	OPA241UA, PA			OPA251UA, PA			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
OFFSET VOLTAGE Input Offset Voltage $T_A = -40^\circ C$ to $+85^\circ C$	V_{OS}		± 100			± 50	± 250	μV
vs Temperature	dV_{OS}/dT		± 150			± 100	± 300	μV
vs Power Supply	$PSRR$		± 0.6			± 0.5	± 30	$\mu V/C$
$T_A = -40^\circ C$ to $+85^\circ C$			*	*		3	30	$\mu V/V$
Channel Separation (dual, quad)			*	*		0.3	30	$\mu V/V$
INPUT BIAS CURRENT Input Bias Current ⁽¹⁾ $T_A = -40^\circ C$ to $+85^\circ C$	I_B		*			-4	-20	nA
Input Offset Current $T_A = -40^\circ C$ to $+85^\circ C$	I_{OS}		*			± 0.1	± 2	nA
NOISE Input Voltage Noise, $f = 0.1Hz$ to $10Hz$	e_n		*			1		$\mu Vp-p$
Input Voltage Noise Density, $f = 1kHz$	i_n		*			45		nV/\sqrt{Hz}
Current Noise Density, $f = 1kHz$			*			40		fA/\sqrt{Hz}
INPUT VOLTAGE RANGE Common-Mode Voltage Range	V_{CM}				$(V-) - 0.2$			V
Common-Mode Rejection Ratio	$CMRR$				100	124	$(V+) - 0.8$	dB
$T_A = -40^\circ C$ to $+85^\circ C$					100			dB
INPUT IMPEDANCE Differential			*				$10^7 \parallel 2$	$\Omega \parallel pF$
Common-Mode			*				$10^9 \parallel 4$	$\Omega \parallel pF$
OPEN-LOOP GAIN Open-Loop Voltage Gain	A_{OL}				100	128		dB
$T_A = -40^\circ C$ to $+85^\circ C$					100			dB
$T_A = -40^\circ C$ to $+85^\circ C$					100	128		dB
FREQUENCY RESPONSE Gain-Bandwidth Product	GBW				100			dB
Slew Rate	SR				100			dB
Overload Recovery Time					100			dB
OUTPUT Voltage Output Swing from Rail ⁽²⁾	V_O				100	128		mV
$T_A = -40^\circ C$ to $+85^\circ C$					100			mV
$T_A = -40^\circ C$ to $+85^\circ C$					100	128		mV
Short-Circuit Current	I_{SC}				100	128		mV
Single Versions					100	128		mV
Dual Versions					100	128		mV
Capacitive Load Drive	C_{LOAD}				100	128		mV
POWER SUPPLY Specified Voltage Range	V_S				100	128		mV
Operating Voltage Range					100	128		mV
Quiescent Current (per amplifier)	I_Q				100	128		μA
$T_A = -40^\circ C$ to $+85^\circ C$					100	128		μA
TEMPERATURE RANGE Specified Range	θ_{JA}				100	128		$^\circ C$
Operating Range					100	128		$^\circ C$
Storage Range					100	128		$^\circ C$
Thermal Resistance					100	128		$^\circ C/W$
8-Pin DIP					100	128		$^\circ C/W$
SO-8 Surface Mount					100	128		$^\circ C/W$
14-Pin DIP					100	128		$^\circ C/W$
SO-14 Surface Mount					100	128		$^\circ C/W$

* Specifications the same as OPA251UA, PA.

NOTES: (1) The negative sign indicates input bias current flows out of the input terminals. (2) Output voltage swings are measured between the output and power supply rails.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Supply Voltage, V+ to V-	36V
Input Voltage ⁽²⁾	(V-) -0.5V to (V+) +0.5V
Output Short Circuit to Ground ⁽³⁾	Continuous
Operating Temperature	-55°C to +125°C
Storage Temperature	-55°C to +125°C
Junction Temperature	150°C
Lead Temperature (soldering, 10s)	300°C

NOTES: (1) Stresses above these ratings may cause permanent damage.

(2) Input terminals are diode-clamped to the power supply rails. Input signals that can swing more than 0.5V beyond the supply rails should be current-limited to 5mA or less. (3) One amplifier per package.



ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

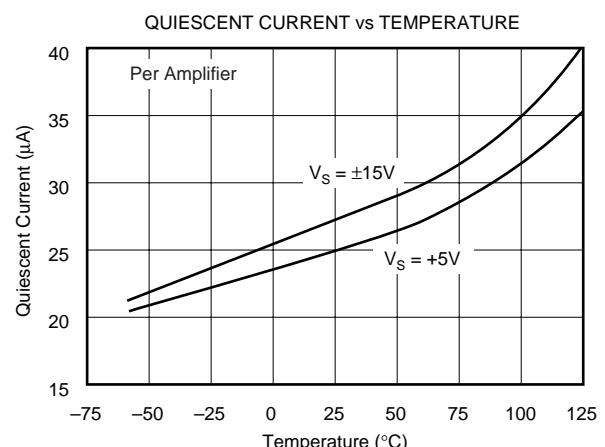
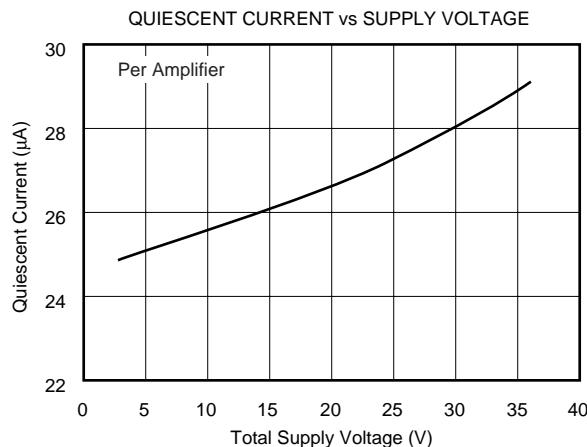
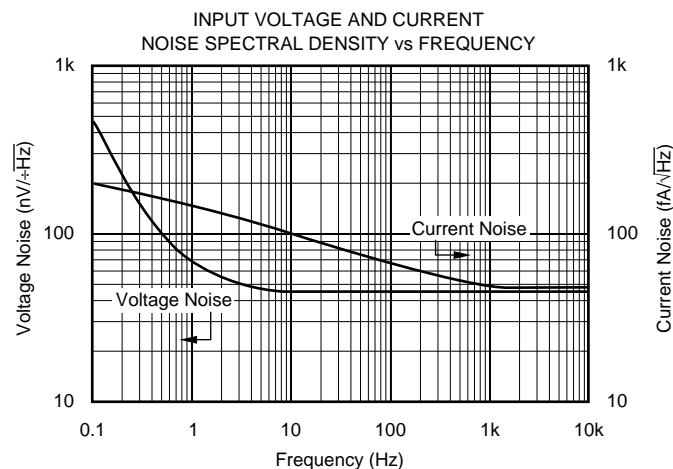
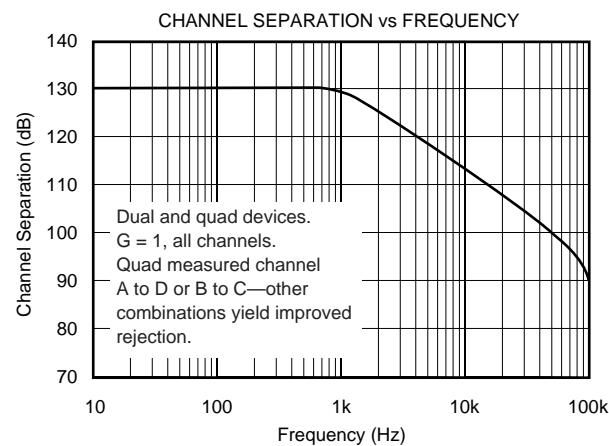
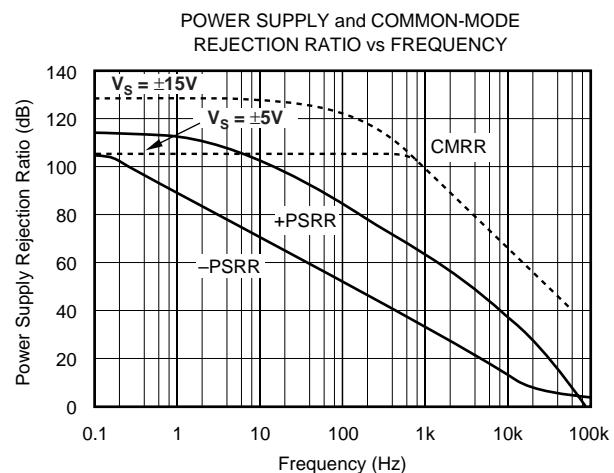
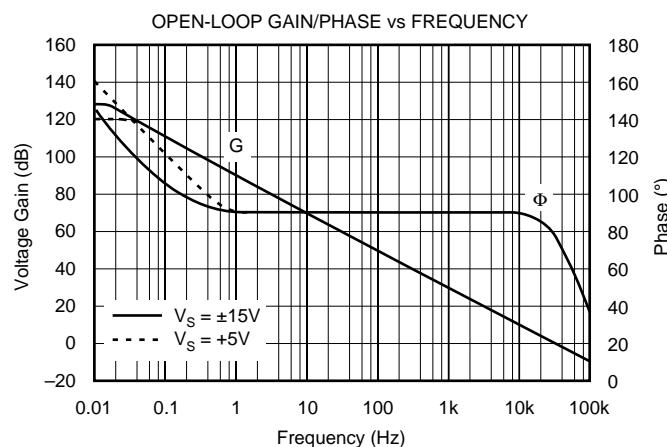
PRODUCT	SPECIFIED VOLTAGE	OPERATING VOLTAGE RANGE	PACKAGE	PACKAGE DRAWING NUMBER ⁽¹⁾	SPECIFICATION TEMPERATURE RANGE
OPA241 SERIES					
Single OPA241PA OPA241UA	2.7V to 5V 2.7V to 5V	2.7V to 36V 2.7V to 36V	8-Pin DIP SO-8 Surface Mount	006 182	-40°C to +85°C -40°C to +85°C
Dual OPA2241PA OPA2241UA	2.7V to 5V 2.7V to 5V	2.7V to 36V 2.7V to 36V	8-Pin DIP SO-8 Surface Mount	006 182	-40°C to +85°C -40°C to +85°C
Quad OPA4241PA OPA4241UA	2.7V to 5V 2.7V to 5V	2.7V to 36V 2.7V to 36V	14-Pin DIP SO-14 Surface Mount	010 235	-40°C to +85°C -40°C to +85°C
OPA251 SERIES					
Single OPA251PA OPA251UA	±15V ±15V	2.7V to 36V 2.7V to 36V	8-Pin DIP SO-8 Surface Mount	006 182	-40°C to +85°C -40°C to +85°C
Dual OPA2251PA OPA2251UA	±15V ±15V	2.7V to 36V 2.7V to 36V	8-Pin DIP SO-8 Surface Mount	006 182	-40°C to +85°C -40°C to +85°C
Quad OPA4251PA OPA4251UA	±15V ±15V	2.7V to 36V 2.7V to 36V	14-Pin DIP SO-14 Surface Mount	010 235	-40°C to +85°C -40°C to +85°C

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

TYPICAL PERFORMANCE CURVES

At $T_A = +25^\circ\text{C}$, and $R_L = 100\text{k}\Omega$ connected to $V_S/2$ (ground for $V_S = \pm 15\text{V}$), unless otherwise noted.

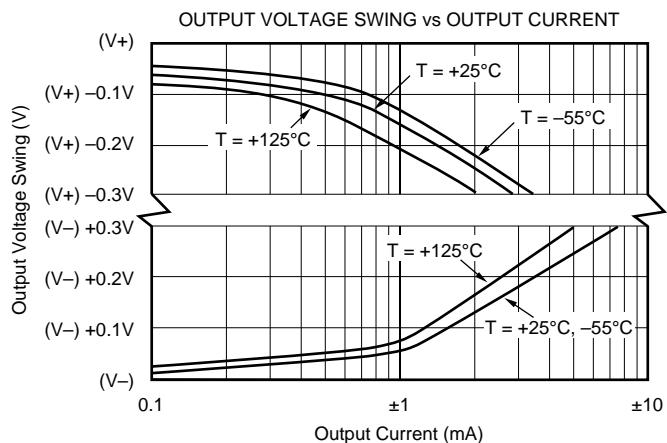
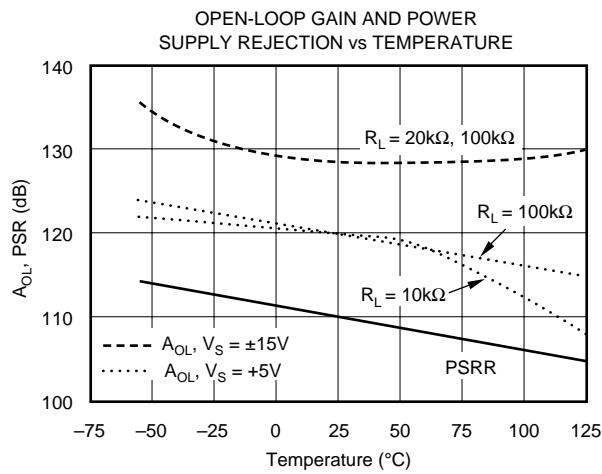
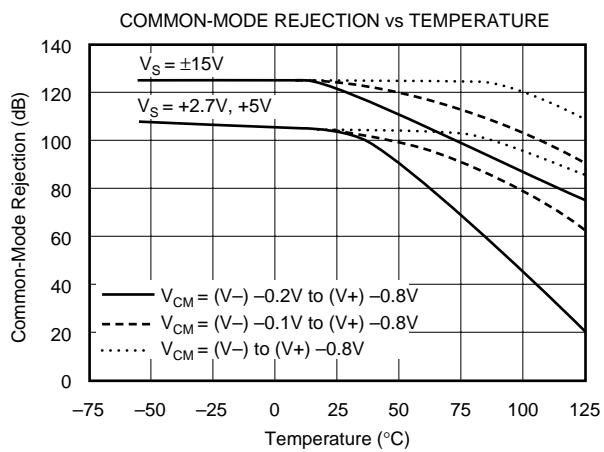
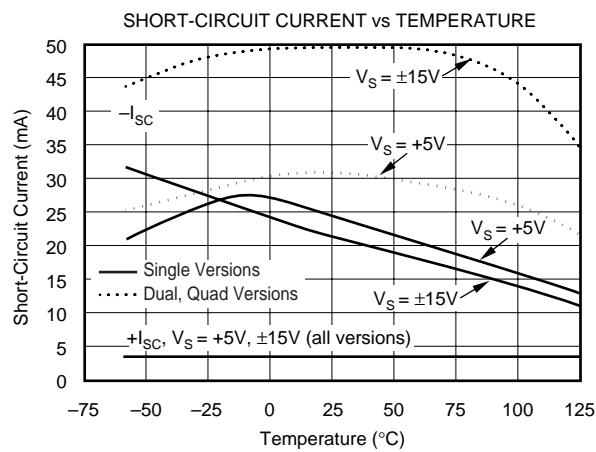
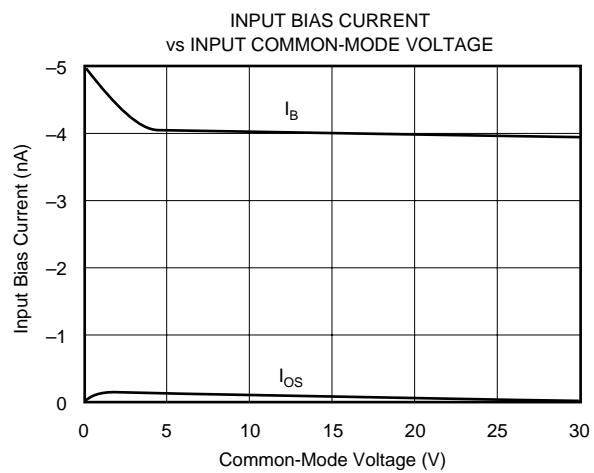
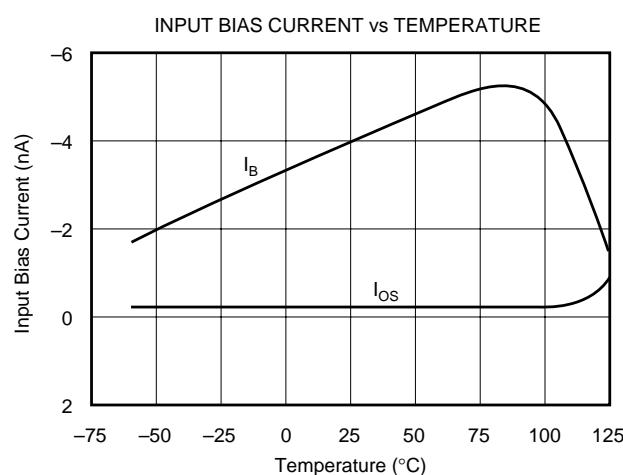
Curves apply to OPA241 and OPA251 unless specified.



TYPICAL PERFORMANCE CURVES (CONT)

At $T_A = +25^\circ\text{C}$, and $R_L = 100\text{k}\Omega$ connected to $V_S/2$ (ground for $V_S = \pm 15\text{V}$), unless otherwise noted.

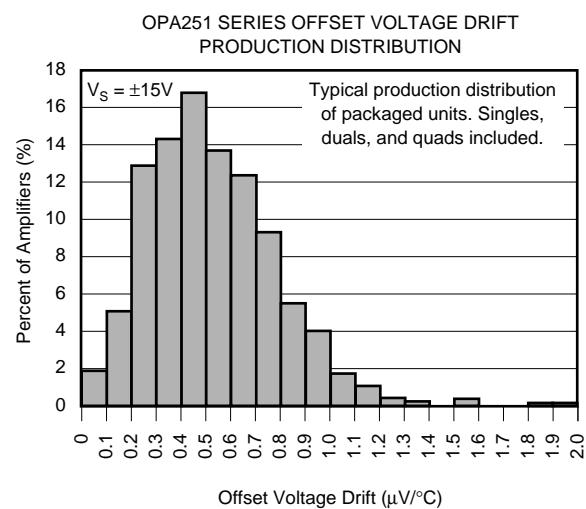
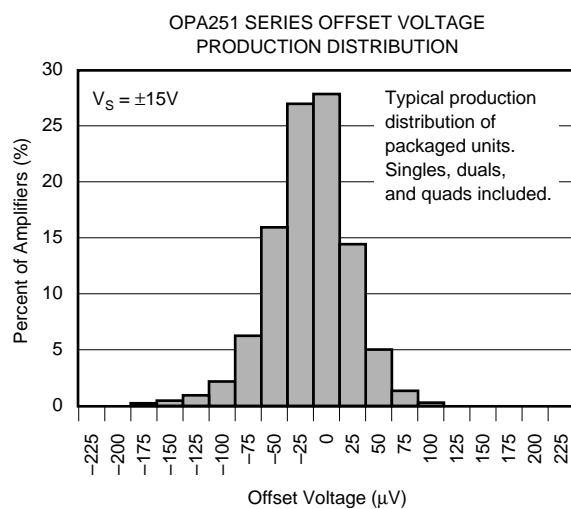
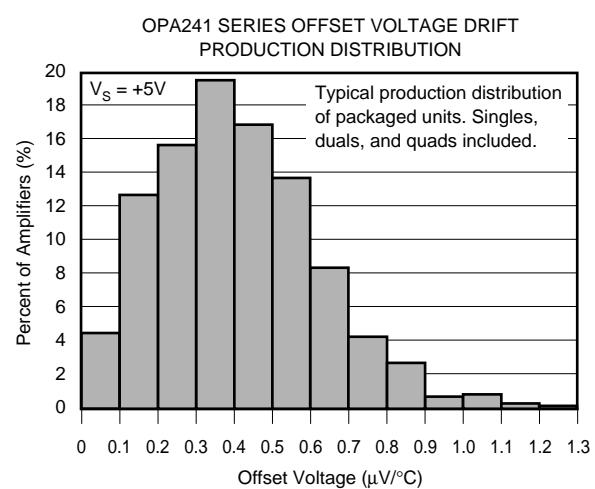
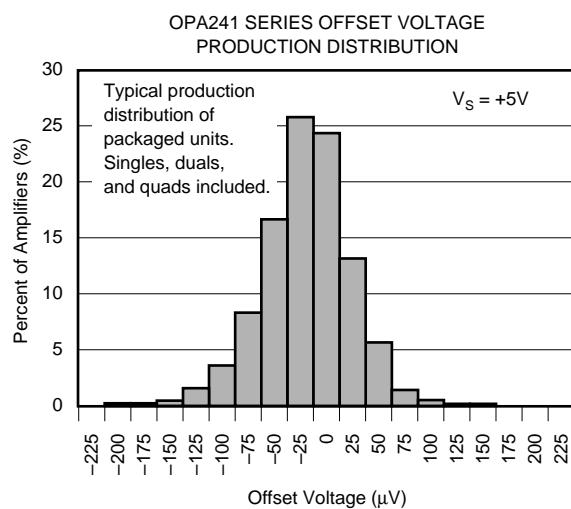
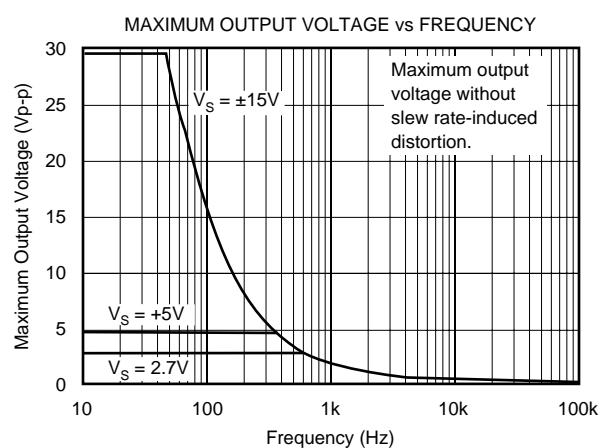
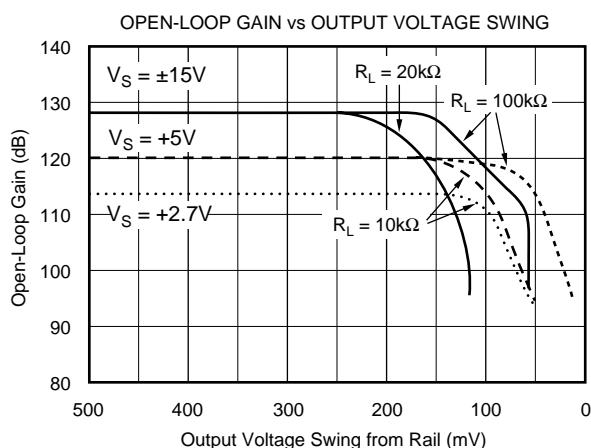
Curves apply to OPA241 and OPA251 unless specified.



TYPICAL PERFORMANCE CURVES (CONT)

At $T_A = +25^\circ\text{C}$, and $R_L = 100\text{k}\Omega$ connected to $V_S/2$ (ground for $V_S = \pm 15\text{V}$), unless otherwise noted.

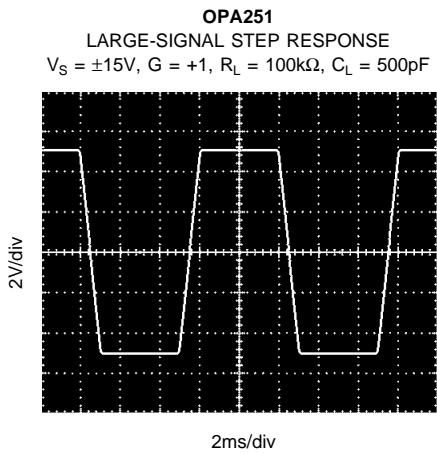
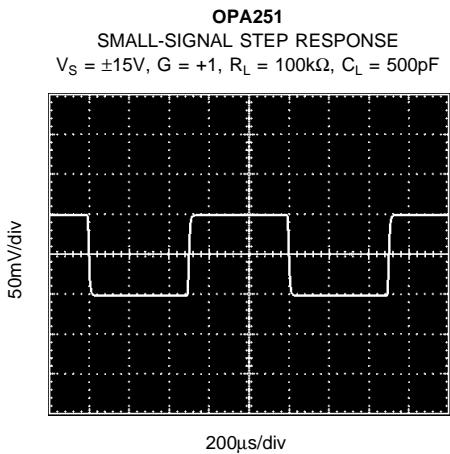
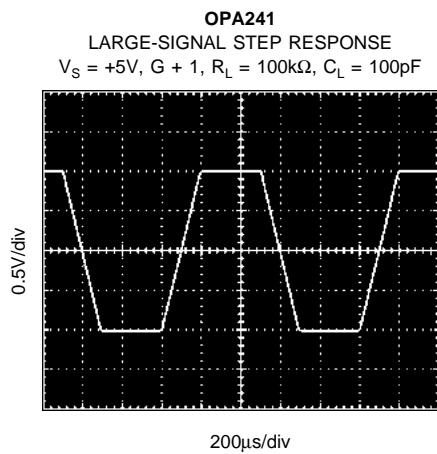
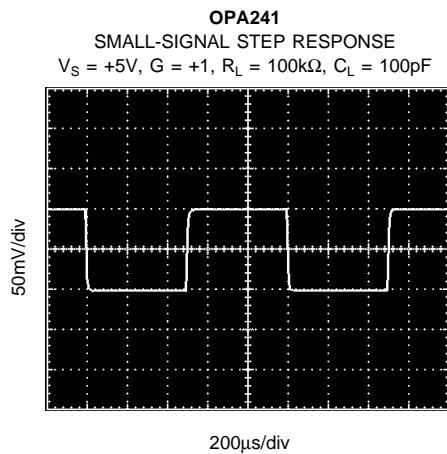
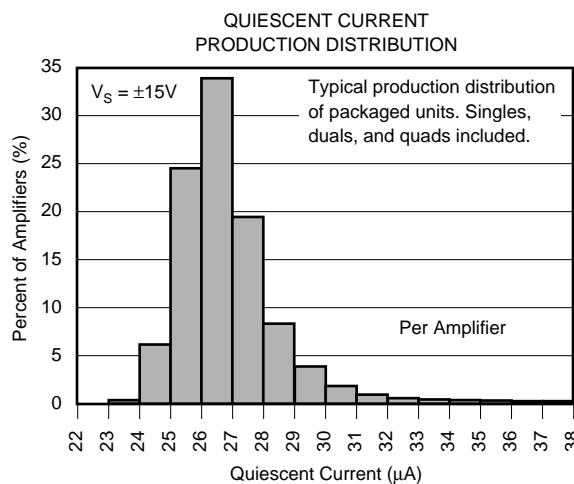
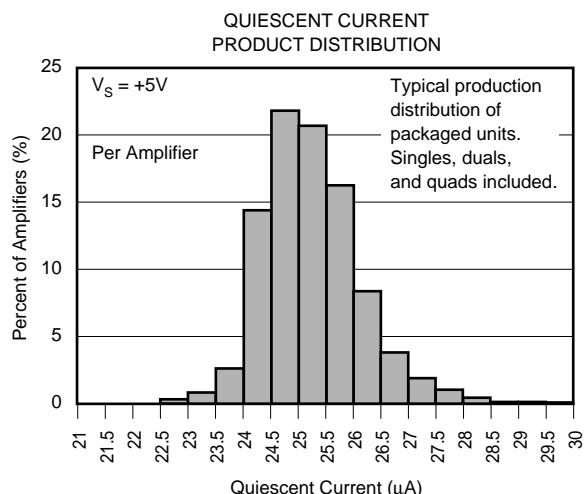
Curves apply to OPA241 and OPA251 unless specified.



TYPICAL PERFORMANCE CURVES (CONT)

At $T_A = +25^\circ\text{C}$, and $R_L = 100\text{k}\Omega$ connected to $V_S/2$ (ground for $V_S \pm 15\text{V}$), unless otherwise noted.

Curves apply to OPA241 and OPA251 unless specified.



APPLICATIONS INFORMATION

The OPA241 and OPA251 series are unity-gain stable and suitable for a wide range of general purpose applications. Power supply pins should be bypassed with $0.01\mu\text{F}$ ceramic capacitors.

OPERATING VOLTAGE

The OPA241 series is laser-trimmed for low offset voltage and drift at low supply voltage ($V_S = +5\text{V}$). The OPA251 series is trimmed for $\pm 15\text{V}$ operation. Both products operate over the full voltage range ($+2.7\text{V}$ to $+36\text{V}$ or $\pm 1.35\text{V}$ to $\pm 18\text{V}$) with some compromises in offset voltage and drift performance. However, all other parameters have similar performance. Key parameters are guaranteed over the specified temperature range, -40°C to $+85^\circ\text{C}$. Most behavior remains unchanged throughout the full operating voltage range. Parameters which vary significantly with operating voltage or temperature are shown in typical performance curves.

OFFSET VOLTAGE TRIM

As mentioned previously, offset voltage of the OPA241 series is laser-trimmed at $+5\text{V}$. The OPA251 series is trimmed at $\pm 15\text{V}$. Because the initial offset is so low, user adjustment is usually not required. However, the OPA241 and OPA251 (single op amp versions) provide offset voltage trim connections on pins 1 and 5. Offset voltage can be adjusted by connecting a potentiometer as shown in Figure 1. This adjustment should be used only to null the offset of the op amp, not to adjust system offset or offset produced by the signal source. Nulling offset could degrade the offset drift behavior of the op amp. While it is not possible to predict the exact change in drift, the effect is usually small.

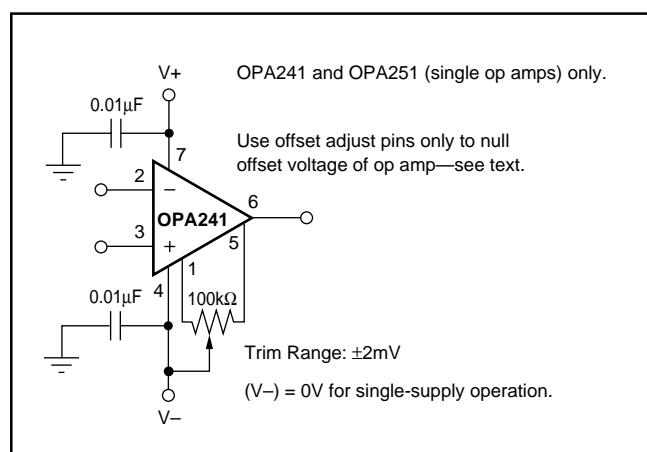


FIGURE 1. OPA241 and OPA251 Offset Voltage Trim Circuit.

CAPACITIVE LOAD AND STABILITY

The OPA241 series and OPA251 series can drive a wide range of capacitive loads. However, all op amps under certain conditions may be unstable. Op amp configuration, gain, and load value are just a few of the factors to consider when determining stability.

Figures 2 and 3 show the regions where the OPA241 series and OPA251 series have the potential for instability. As shown, the unity gain configuration with low supplies is the most susceptible to the effects of capacitive load. With $V_S = +5\text{V}$, $G = +1$, and $I_{\text{OUT}} = 0$, operation remains stable with load capacitance up to approximately 200pF . Increasing supply voltage, output current, and/or gain significantly improves capacitive load drive. For example, increasing the supplies to $\pm 15\text{V}$ and gain to 10 allows approximately 2700pF to be driven.

One method of improving capacitive load drive in the unity gain configuration is to insert a resistor inside the feedback loop as shown in Figure 4. This reduces ringing with large capacitive loads while maintaining dc accuracy. For example, with $V_S = \pm 1.35\text{V}$ and $R_S = 5\text{k}\Omega$, the OPA241 series and OPA251 series perform well with capacitive loads in excess of 1000pF . Without the series resistor, capacitive load drive is typically 200pF for these conditions. However, this method will result in a slight reduction of output voltage swing.

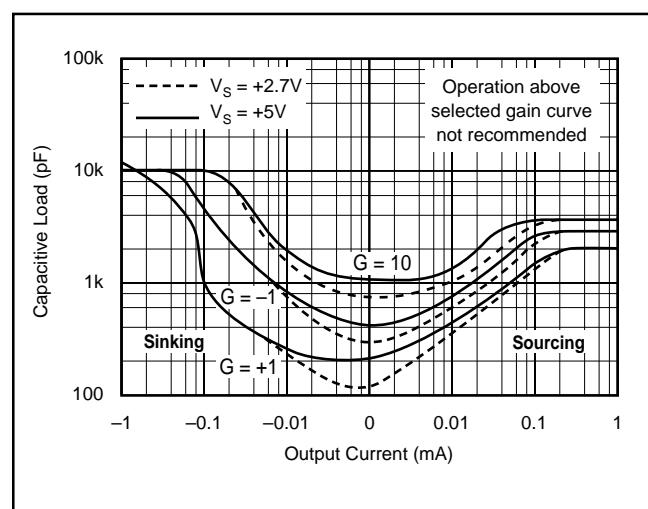


FIGURE 2. Stability—Capacitive Load versus Output Current for Low Supply Voltage.

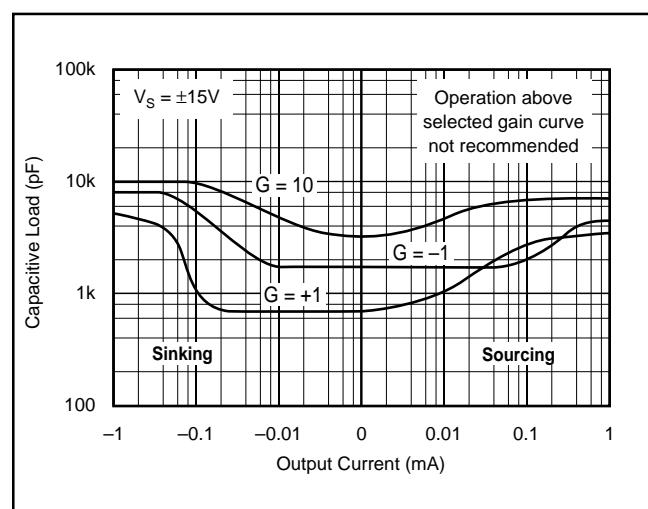


FIGURE 3. Stability—Capacitive Load versus Output Current for $\pm 15\text{V}$ Supplies.

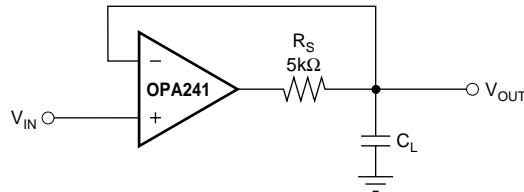
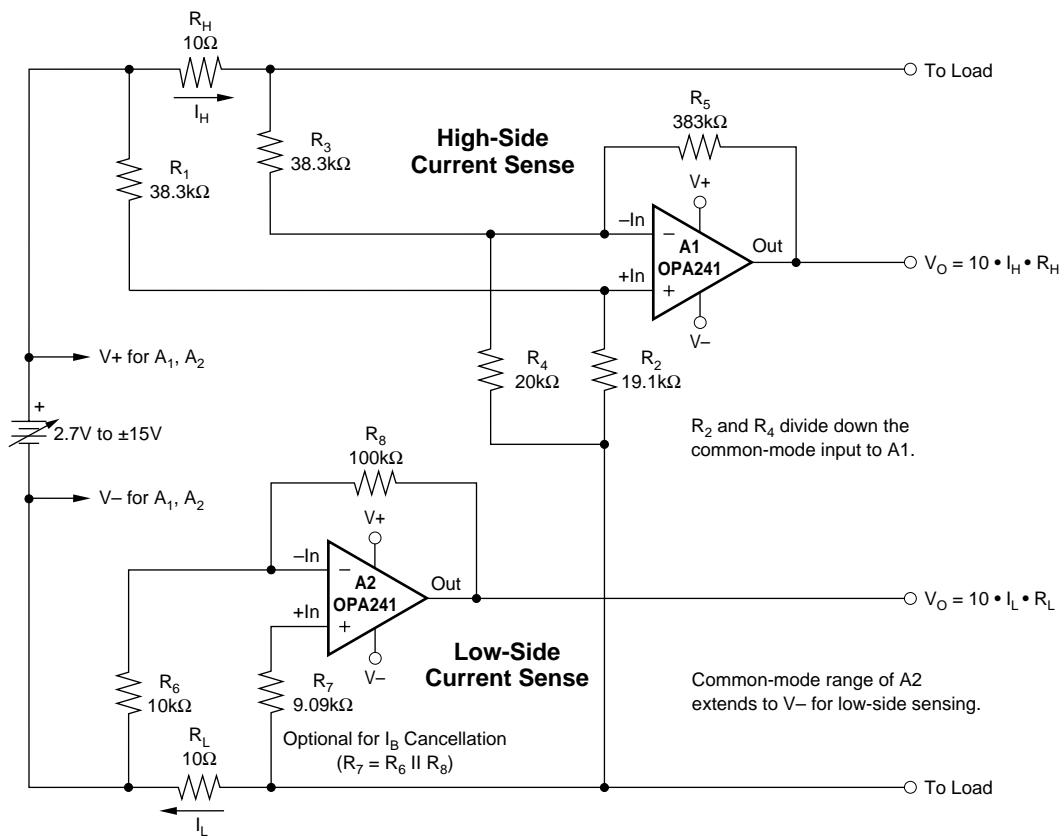


FIGURE 4. Series Resistor in Unity Gain Configuration Improves Capacitive Load Drive.



NOTE: Low and high-side sensing circuits can be used independently.

FIGURE 5. Low and High-Side Battery Current Sensing.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA2241PA	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		OPA2241PA	Samples
OPA2241PAG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		OPA2241PA	Samples
OPA2241UA	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		OPA2241UA	Samples
OPA2241UA/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		OPA2241UA	Samples
OPA2241UA/2K5G4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		OPA2241UA	Samples
OPA2241UAG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		OPA2241UA	Samples
OPA2251PA	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		OPA2251PA	Samples
OPA2251PAG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		OPA2251PA	Samples
OPA2251UA	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		OPA2251UA	Samples
OPA2251UA/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		OPA2251UA	Samples
OPA2251UA/2K5G4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		OPA2251UA	Samples
OPA2251UAG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		OPA2251UA	Samples
OPA241PA	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		OPA241PA	Samples
OPA241PAG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		OPA241PA	Samples
OPA241UA	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA241UA	Samples
OPA241UA/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA241UA	Samples
OPA241UA/2K5E4	PREVIEW	SOIC	D	8		TBD	Call TI	Call TI	-40 to 85		

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA241UA/2K5G4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA241UA	Samples
OPA241UAE4	PREVIEW	SOIC	D	8		TBD	Call TI	Call TI	-40 to 85		
OPA241UAG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA241UA	Samples
OPA251PA	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		OPA251PA	Samples
OPA251PAG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		OPA251PA	Samples
OPA251UA	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		OPA251UA	Samples
OPA251UA/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		OPA251UA	Samples
OPA251UA/2K5G4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		OPA251UA	Samples
OPA251UAG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		OPA251UA	Samples
OPA4241PA	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		OPA4241PA	Samples
OPA4241PAG4	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		OPA4241PA	Samples
OPA4241UA	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		OPA4241UA	Samples
OPA4241UA/2K5	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		OPA4241UA	Samples
OPA4241UAG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		OPA4241UA	Samples
OPA4251PA	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		OPA4251PA	Samples
OPA4251PAG4	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		OPA4251PA	Samples
OPA4251UA	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		OPA4251UA	Samples
OPA4251UA/2K5	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		OPA4251UA	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA4251UA/2K5G4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		OPA4251UA	Samples
OPA4251UAG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		OPA4251UA	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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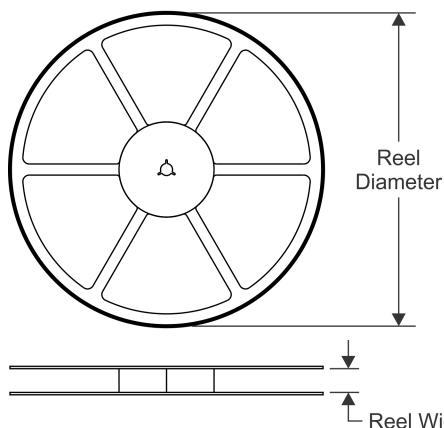
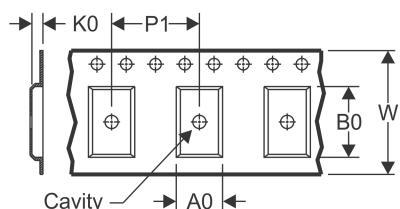
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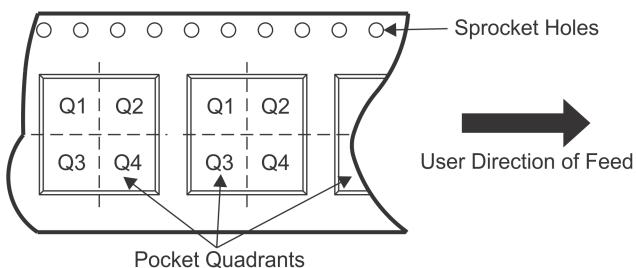
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PACKAGE OPTION ADDENDUM

10-Jun-2014

TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2241UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2251UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA241UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA251UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA4241UA/2K5	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
OPA4251UA/2K5	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

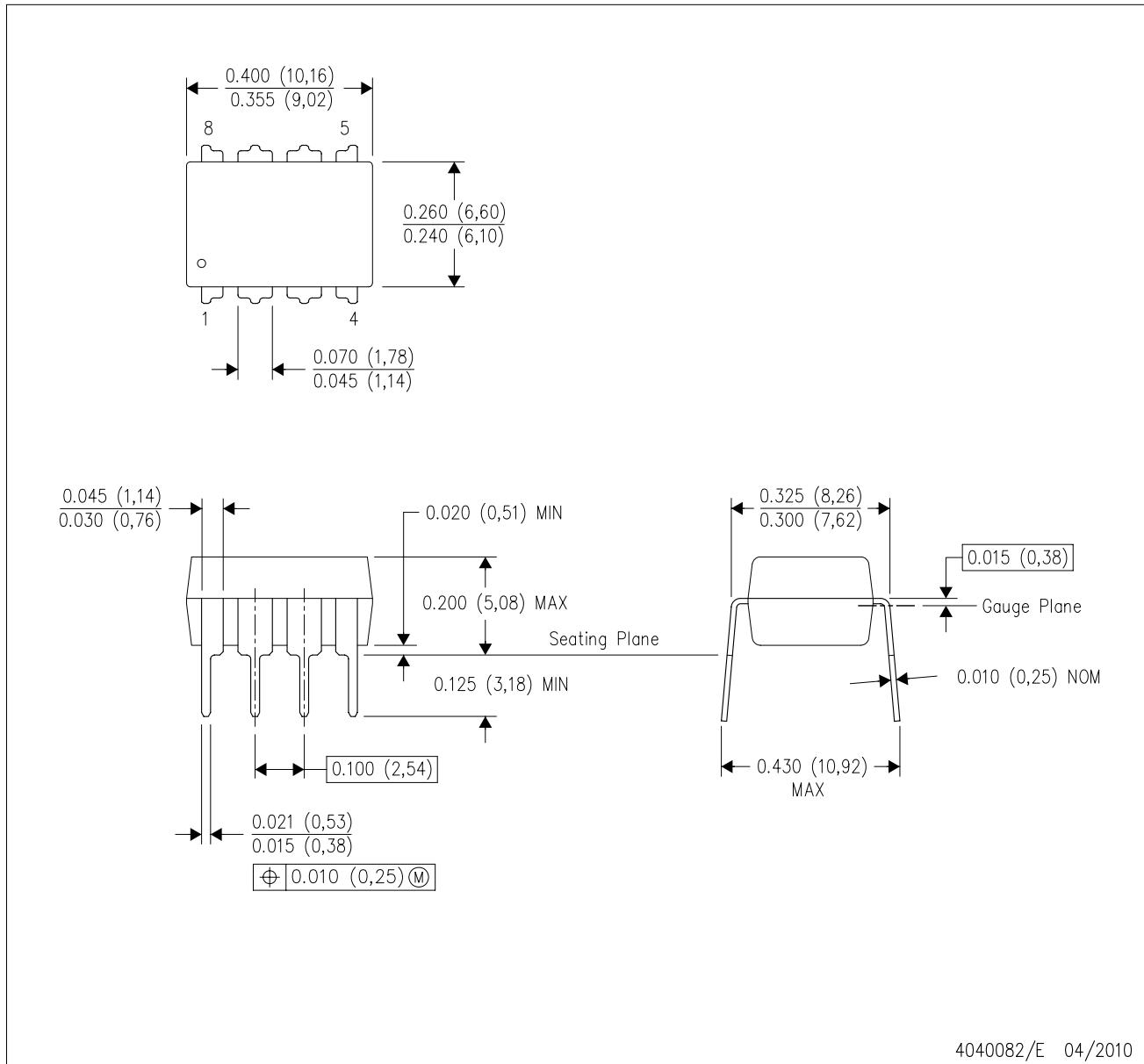
TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2241UA/2K5	SOIC	D	8	2500	367.0	367.0	35.0
OPA2251UA/2K5	SOIC	D	8	2500	367.0	367.0	35.0
OPA241UA/2K5	SOIC	D	8	2500	367.0	367.0	35.0
OPA251UA/2K5	SOIC	D	8	2500	367.0	367.0	35.0
OPA4241UA/2K5	SOIC	D	14	2500	367.0	367.0	38.0
OPA4251UA/2K5	SOIC	D	14	2500	367.0	367.0	38.0

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE

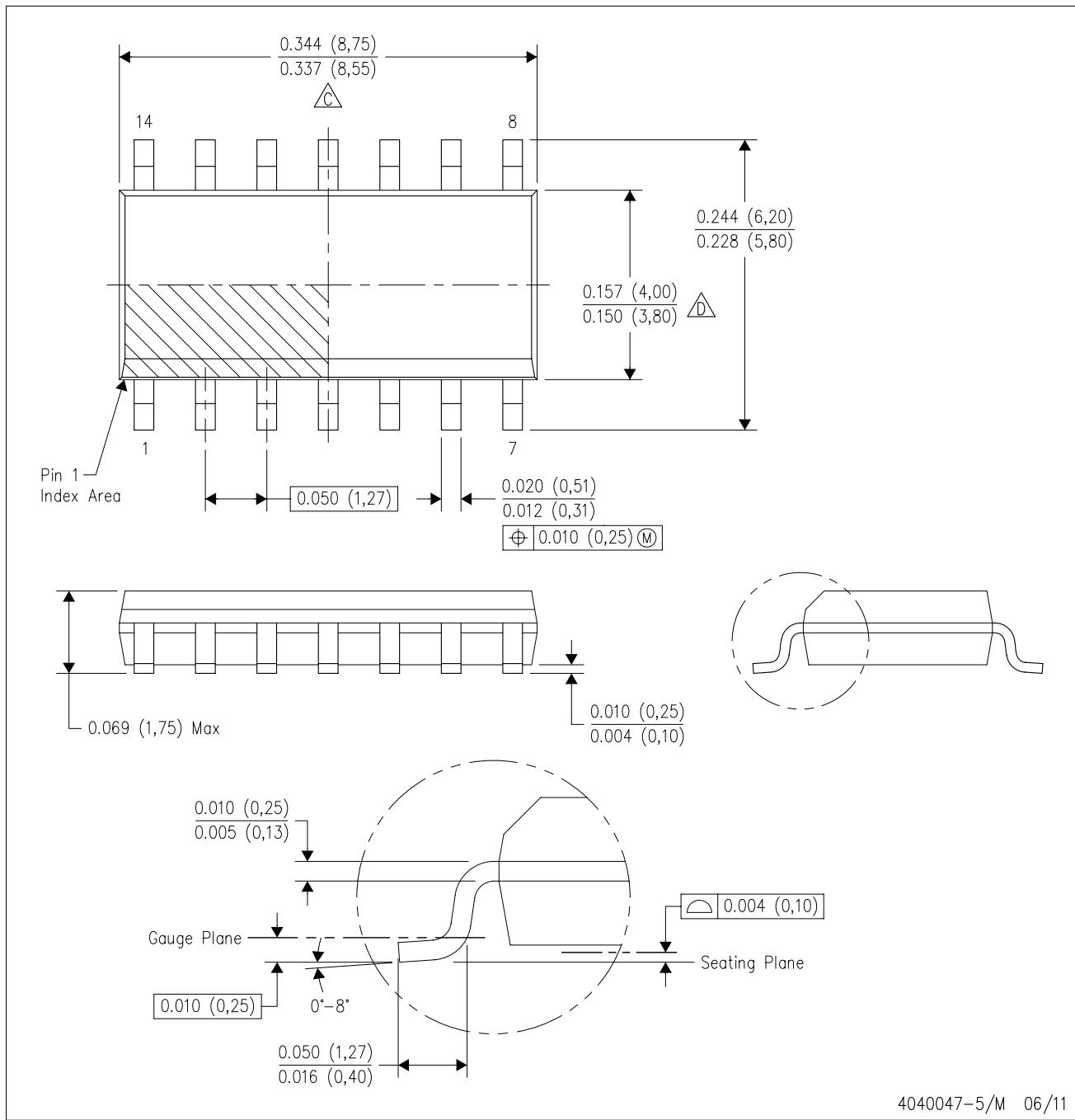


NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MS-001 variation BA.

4040082/E 04/2010

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

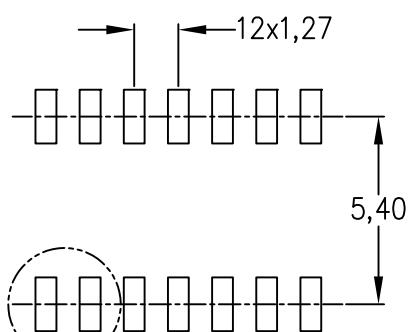
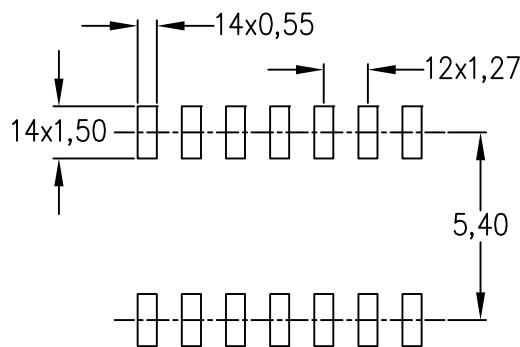
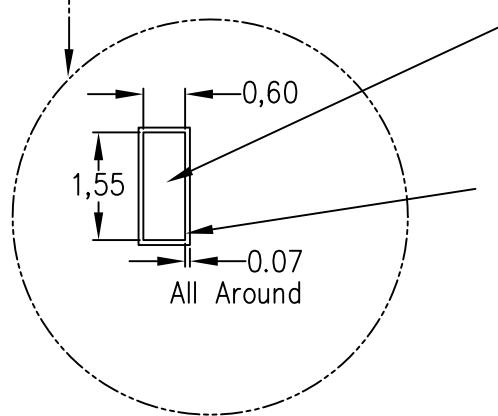
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.

D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.

E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)Stencil Openings
(Note D)Example
Non Soldermask Defined PadExample
Pad Geometry
(See Note C)Example
Solder Mask Opening
(See Note E)

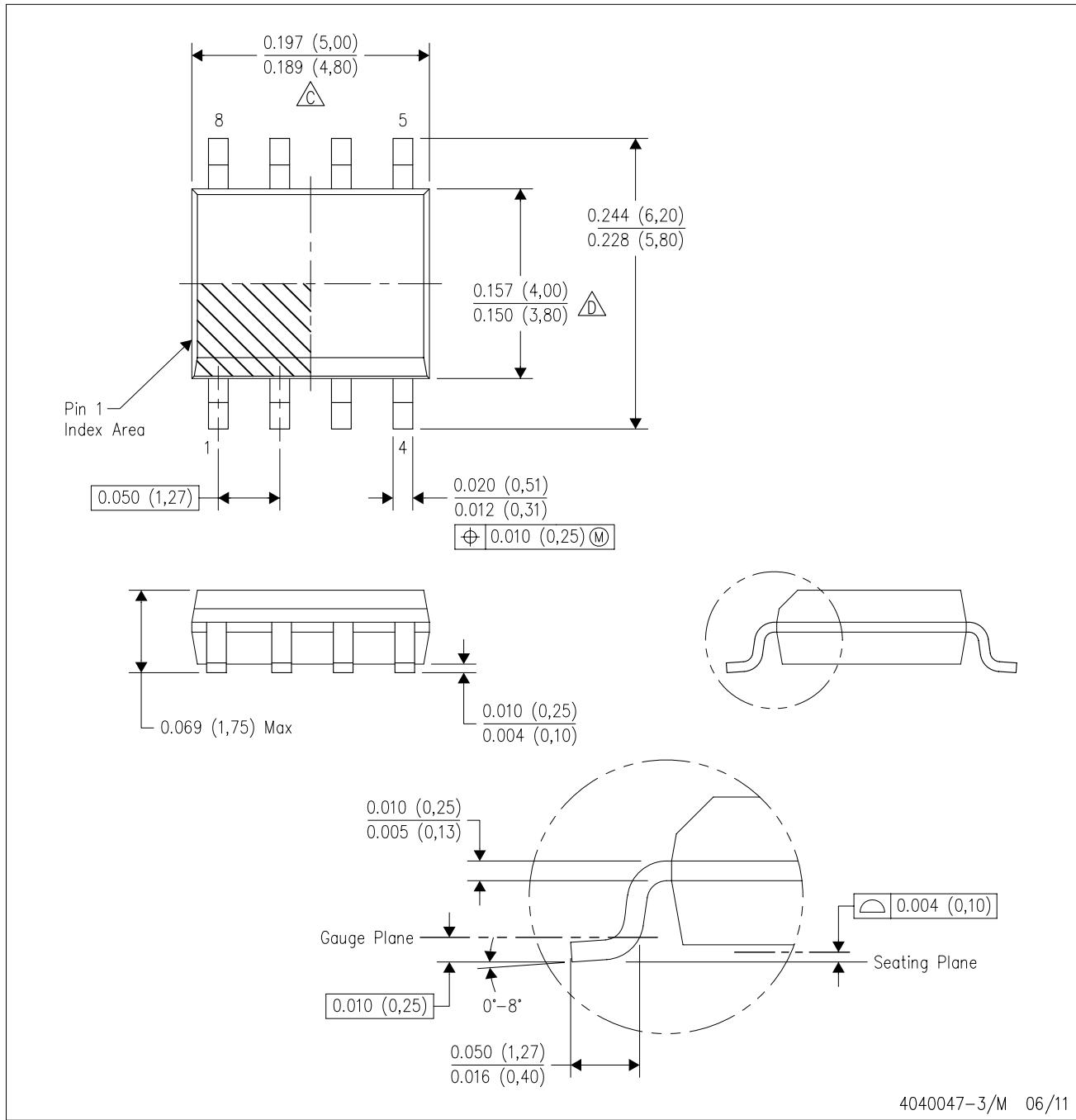
4211283-3/E 08/12

NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Publication IPC-7351 is recommended for alternate designs.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

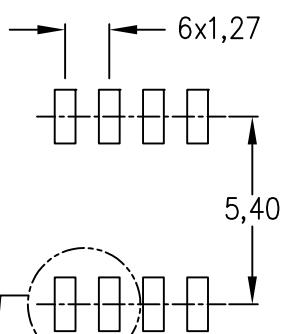
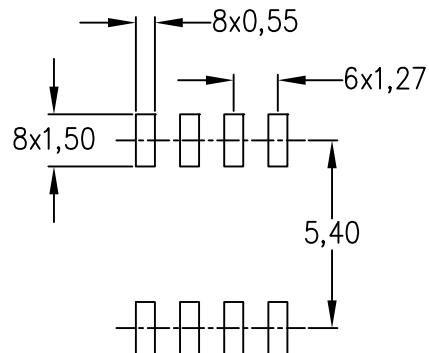
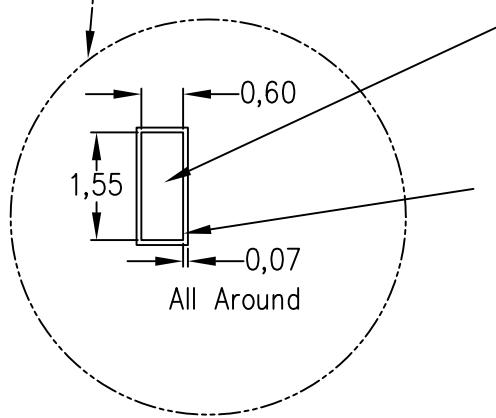
△C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0.15) each side.

△D Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0.43) each side.

E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)Stencil Openings
(Note D)Example
Non Soldermask Defined PadExample
Pad Geometry
(See Note C)Example
Solder Mask Opening
(See Note E)

4211283-2/E 08/12

NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Publication IPC-7351 is recommended for alternate designs.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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