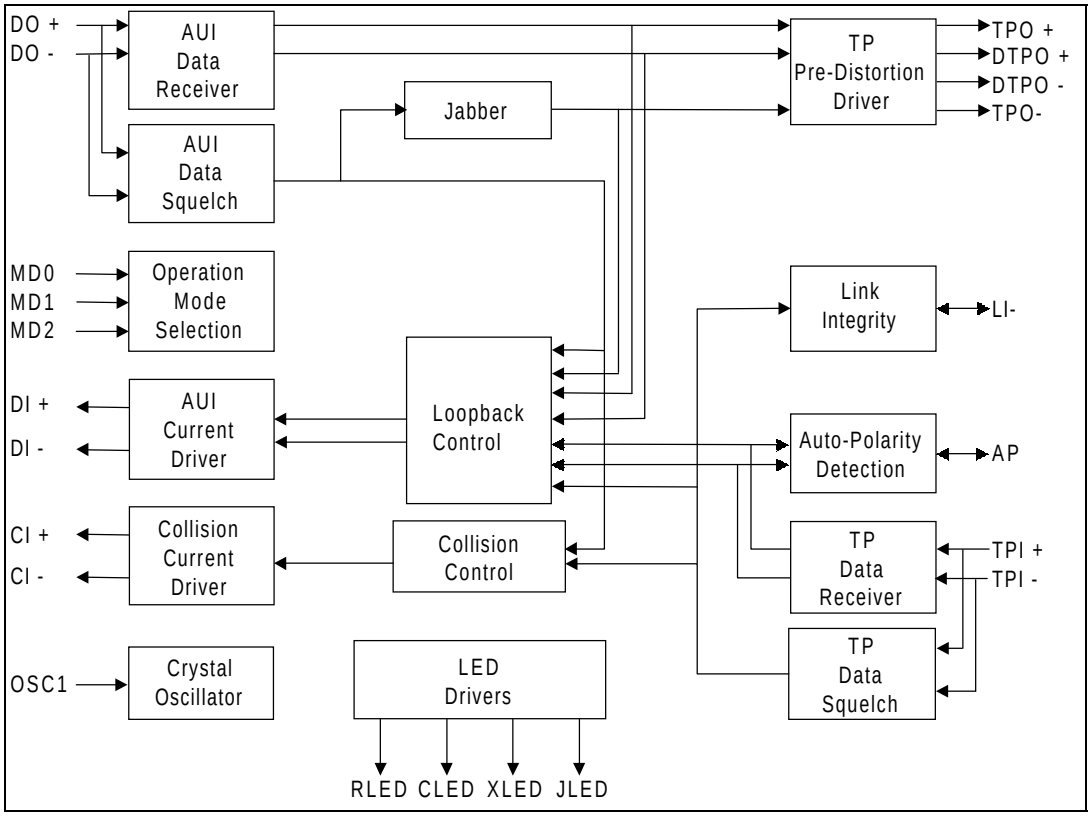
General Description

The DM9095 twisted-pair Media Attachment Unit (TPMAU) is designed to allow Ethernet connections to use existing Twisted-pair wiring plants through an Ethernet Attachment Unit Interface (AUI). The DM9095 provides the electrical interface between the AUI and the twisted-pair wire.

The DM9095's functions include level-shifted data pass-through from one transmission media to another, collision detection, transmitting pre-distortion generation, receiving squelch function, selectable signal-quality-error (SQE) test generation, a link-integrity strapping option, and automatic correction of polarity reversal on the twisted pair input. The DM9095 also includes LED drivers for transmit, receive, jabber, collision, reversed polarity detect and link status.

The DM9095 is an advanced CMOS device available in 28-pin PLCC packages.

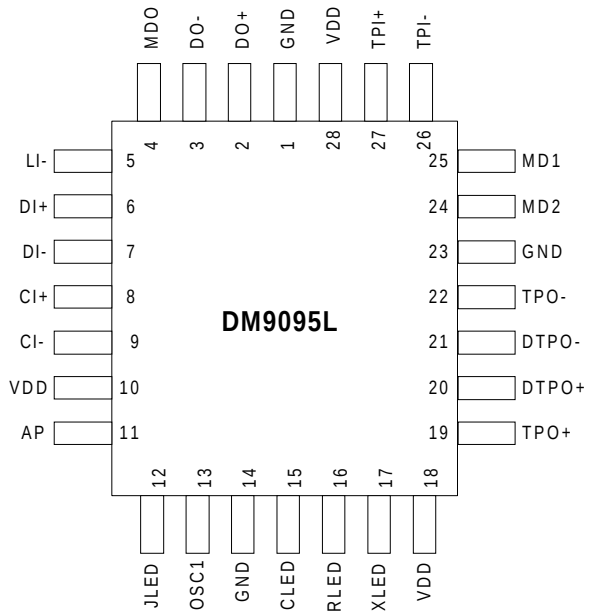
Block Diagram



Features

- Compatible with or exceeds IEEE 802.3 standards for AUI and 10BASE-T interfaces
- Internal pre-distortion generator for TP driver
- Smart squelch circuitry on all received data
- Selectable heartbeat function
- Selectable line-integrity test with LED indication
- LED indicator for transmit, receive, jabber, and collision
- Advanced analog CMOS process using single 5V supply
- Lower TP threshold option for long length application
- Selectable auto-polarity detection and correction function with LED indication
- Automatic AUI/RJ45 selection
- Power-down mode
- Full ESD protection

Pin Configuration : DM9095L



Pin Description

Pin No.	Pin Name	I/O	Description
1	GND	-	Ground
2 3	DO+ DO-	I	Transmitter input. A balanced differential line receiver input pair from the AUI circuit that receives 10 Mbits/s Manchester-encoded data and applies the data to the TP cable.
4	MD0	I	Operation mode selection pin. Pulled high internally.
5	LI-		Link-Integrity enable. The pin is a dual function pin that determines whether the link integrity function should be realized. When this pin, which is internally pulled-high, is configured as an input pin and tied low, the link integrity test function is enabled. While configured as an output pin, the pin drives low for link-fail state and drives high for link-pass state. The output pin can drive an LED status indicator, as in Figure 3(b) (page 6).
6 7	DI+ DI-	O	Receiver outputs. A balanced output current driver pair to the AUI transceiver cable with the 10 Mbits/s Manchester-encoded data received from the twisted-pair of the network.
8 9	CI+ CI-	O	Collision outputs. Balanced differential line driver outputs which send a 10MHz oscillation signal to the Manchester encoder/decoder in the event of a collision, jabber interrupt, or heartbeat test.
10	VDD	-	+5V Power Supply
11	AP	I/O	Auto Polarity. This pin is a dual function pin which determines if the auto-polarity function should be enabled. The function is enabled if the pin is HIGH. The pin is also capable of driving an LED if the function is enabled.
12	JLED	O	Jabber indicator. Normally off. It indicates a time-out transmission onto TP network. It turns on if the watchdog timer has timed out and the twisted-pair driver has been disabled.
13	OSC1	I	Crystal pin. This pin is a 20MHz frequency-reference terminal for internal chip timing.
14	GND	-	Ground

Pin Description (continued)

Pin No.	Pin Name	I/O	Description
15	LCED	O	Collision indicator. Normally off. It indicates a collision has been detected by the MAU. It turns on the LED if a collision occurs.
16	RLED	O	Receive Indicator. Normally on. It indicates a reception from the TP network is in progress. When LI- is disabled, RLED will turn off if the MAU receives a packet. When LI- is enabled, RLED will turn off as long as the link is broken.
17	XLED	O	Transmit indicator. Normally on. It indicates that a transmiwwion onto the TP network is in progress by turning off.
18	VDD	O	+5V Power Supply
19 20 21 22	TPO+ DTPO+ DTPO- TPO-	O	TP driver outputs. These four outputs provide the TP drivers with pre-distortion capability. The TPO+ /TPO- outputs generate 10Mbits/s Manchester-encoded data. The DTPO+ /DTPO- outputs are one-half bit time delayed and inverted with respect to TPO+ /TPO-.
23	GND	-	Ground
24	MD2	I	Operation mode selection pin. Pulled high internally
25	MD1	I	Operation mode selection pin. Pulled high internally
26 27	TPI- TPI+	I	TP Receive input. A differential receiver tied to the receive transformer pair of the twisted-pair wire. The receive pair of the twisted-pair medium is driven with 10Mbits/s Manchester-encoded data.
28	VDD	O	+ 5V Power Supply

Overview

The DM9095 provides the interface between an AUI and a TP wire. The receive, transmit, and collision detection functions of the DM9095 are designed to meet the IEEE 802.3 10BASE-T draft standard. The receive section transfers 10Mbits/s Manchester-encoded data from the twisted-pair to the AUI, while the transmit section transfers data from the AUI cable to the TP wire. The collision-detection function sends a 10MHz square wave onto the AUI_CI circuits after sensing data being simultaneously transmitted and received.

In addition to the these functions, there are three optional operating functions. Enabling the link-integrity function causes a pulse to be transmitted in the absence of data transmission. The Receiver recognized link-integrity pulses and connects the twisted-pair link. The link-integrity pin can be configured as an input or as an output. When the link-integrity pin is configured as an input, the function is enabled for proper setting. When the link-integrity pin is configured as an output, the function is enabled and the status of the link is indicated.

If the heartbeat function is enabled, it allows the SQE-test sequence to be transmitted to the DTE after every successful transmission on the TP wire. The option also enables normal or extended line length to be selected. When standard TP squelch levels are implemented, normal line length is used. When the TP squelch thresholds are lowered, extended line length is used.

The device also contains an auto-polarity function which can be determined if the receive twisted-pair has been wired with polarity reversal. If the twisted-pair is wired with polarity reversal, the device automatically corrects for this error condition. Also, the auto-polarity function can be used with an LED to display the polarity of the receive twisted-pair wire.

When power-down mode is set, the device shuts down, and the supply current is reduced to less than 10µA. The DM9095 automatically pulls AUI-DI, AUI_CI, and AUI-DO into high impedance state if the twisted-pair link is not connected. The function is used to provide the Encoder/Decoder chip to use coaxial MAU. The DM9095 also includes four drivers capable of driving four LEDs to indicate the status of the receive, transmit, collision, and jabber functions. Also, when configured correctly, two additional LEDs can display auto-polarity and link-integrity status.

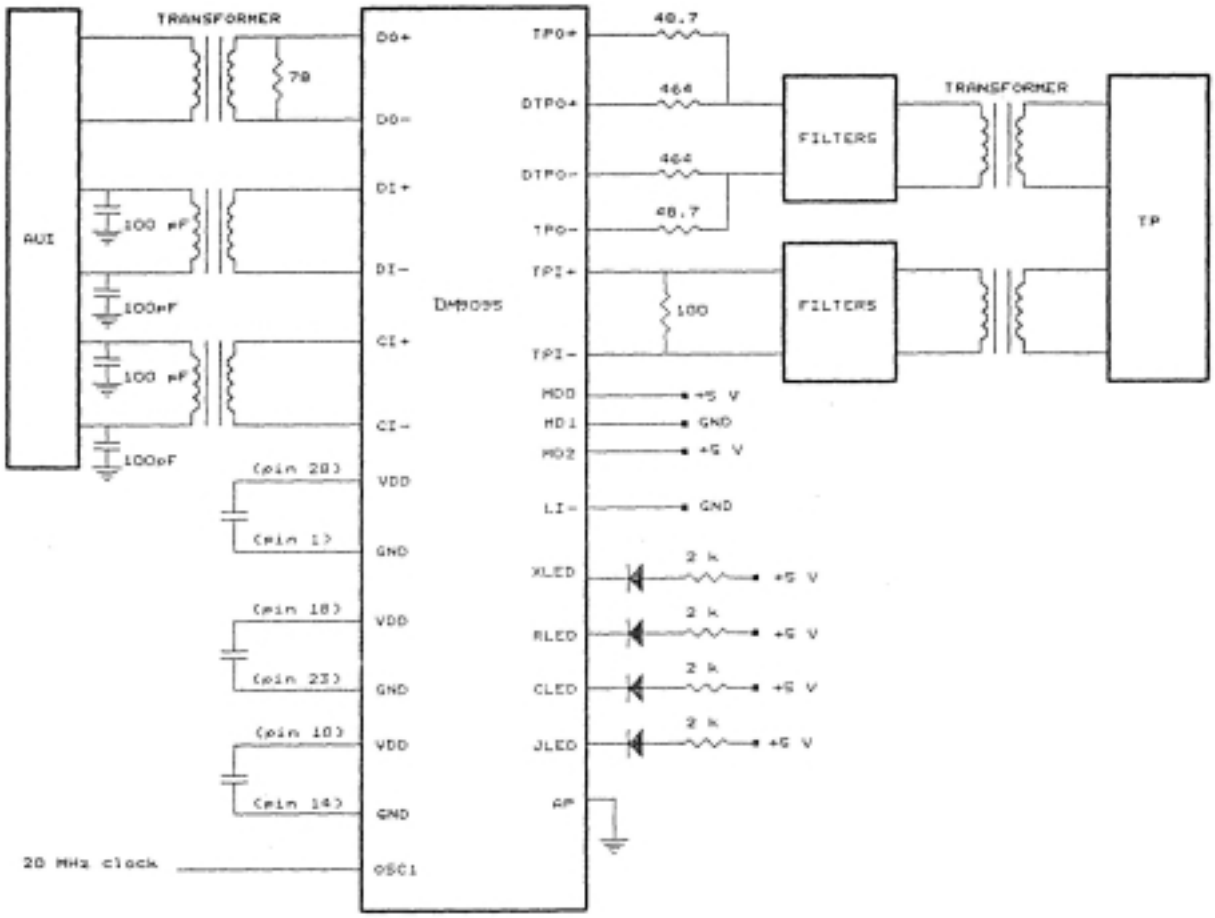


Figure 3 (a). Typical System Application for External TPMAU in Mode 5 (Where Link Integrity Test is enabled, Auto-polarity is disabled. LI- is input pin)

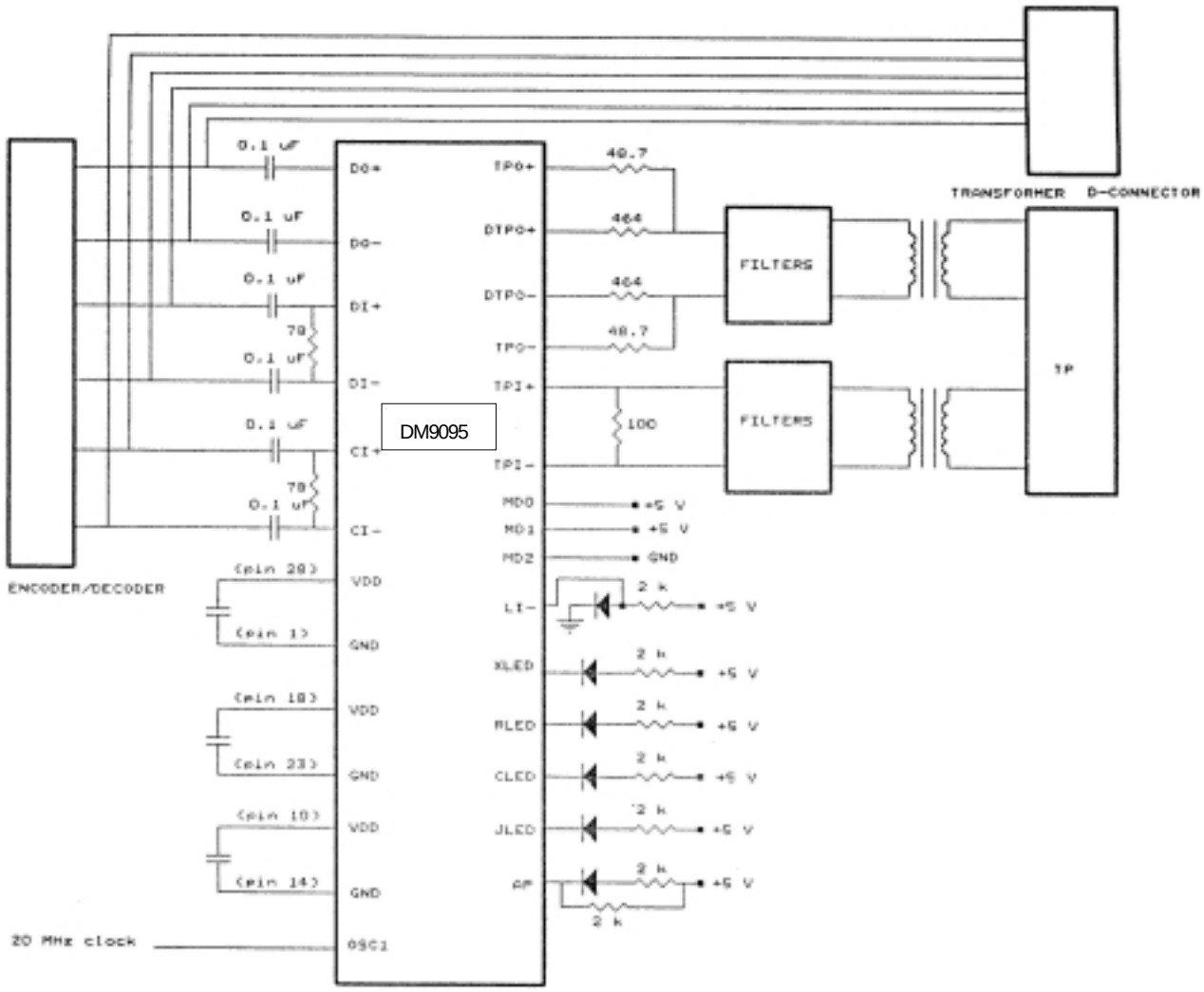


Figure 3 (b). Typical System Application for Internal TPMAU in Mode 6 (Where Link Integrity Test is enabled and Auto Polarity Function is enabled. LI- is output pin)

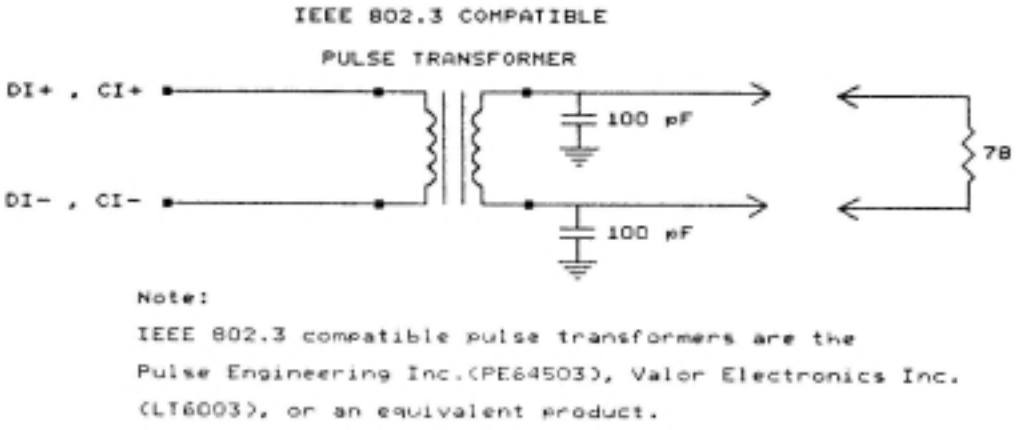
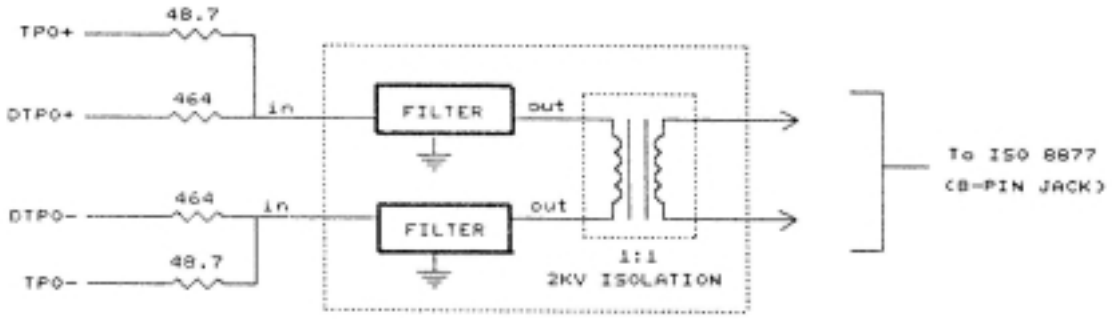


Figure 4. Typical Loading Conditions for DI± and CI±



Note:
1. Possible filters are the Pulse Engineering Inc. <PE32101> or an equivalent.
2. The 1:1 2KV isolation transformer can be a Pulse Engineering <PE65263> or Equivalent.
3. The filters and isolation transformer can be combined into one package. A possible source is Valor Electronics <PT3877> or an equivalent.

Figure 5. Example of Transmit Circuit

Function Description

Transmit Functions

The DM9095 receives transmit data from DO + /DO - and transfers it to the TP network. The input must be transformer-coupled to the AUI circuit. The receiver is able to pass differential signals as small as 300mV peak and as large as 1315mV. DC biasing is provided with internal common-mode, the common-mode is set to nominal 2.5V. An internal analog delay line is used to generate the pre-distortion signals at DTPO + and DTPO -. The DTPO + / DTPO - signal delays 50ns after TPO + / TPO -. A delay lock loop, referenced to the crystal clock, is used to generate the internal delay line. All TP output driver pins are driver low as a result of any of the following: there is an AUI IDL pulse of at least 200ns duration; the output driver is jabbered; the link-integrity option is enabled and there is a link failure; or an IDL pulse is not detected at the end of a packet and the input dose not exceed the detection threshold of 500ns$\pm$ 100ns. When the driver detects that it has finished sending an IDL pulse onto the TP, a timer of not more than 500ns is started. While this timer is active, activity on the DO + / DO - inputs is ignored.

Receive Functions

The TP receiver is connected to a band-limiting filter, whose input is transformer-coupled to the twisted-pair TPI + / TPI - pins. The receiver is able to resolve differential signals as small as 350mV peak. Common-mode input voltage is provided with internal common-mode, with the common-mode set to nominal 2.5V. The receiver squelch circuit prevents noise on the twisted-pair cable from falsely triggering the receiver in the absence of true data. The receiver will not be activated for signals at the buffer input having a peak amplitude below 300mV, a continuous frequency below 2 MHz, or a single cycle duration within the pass band of the receive filter. This driver differentially drives a current onto the load connected between the DI + and DI - pins. The current through the load results in an output voltage between $\pm$ 0.6V and $\pm$ 1.2V, measured differentially between the two pins. As in figure 4, it shows the typical loading for DI + / DI - driver. When the driver detects that it has finished sending an IDL pulse onto the AUI, a timer of not more than 500ns is started. While this timer is active, activity on the TPI + / TPI - inputs is ignored, and the AUI driver discharges the current stored on the inductive load.

Collision Functions

A collision state exists whenever there are valid inputs to the DM9095 from the network and from the DTE simultaneously and the device is not in a link-integrity failure state. The DM9095 reports collisions to the AUI by sending a 10 MHz signal over the CI + / CI - pair. The collision report signal is output no more than 9 BT after the chip detects a collision. If TPI + / TPI - become active while there is activity on the DO + / DO - pair, the loopback data on TPI + / TPI - switches from transmit data to receive data within 13 BT$\pm$ 3 BT. If a collision condition exits with TPI + / TPI - having gone idle while DO + / DO – are still active, SQE continues for 7 BT$\pm$ 2 BT. If a collision condition exits with DO + / DO – having gone idle while TPI + / TPI– are still active, SQE may continue for up to 9 BT.

Jabber Functions

Jabber is a self-interrupt function that keeps a damaged node from continously transmitting onto the network. The chip contains a nominal window of 50ms, during which time a normal data link frame can be transmitted. If a frame length exceeds this duration, the jabber function inhibits transmission and sends a collision signal on the CI + / CI – pair. When activity on the DO + / DO – pair has ceased, the chip continues to present the CSO signal to the CI + / CI – pair for 0.5s$\pm$ 50%. The transmission of link-integrity pulses from the TP drivers is not inhibited when the DM9095 is jabbed and the link integrity function is enabled.

SQE Test Functions

When the DO + / DO – pair has gone idle after a successful transmission and the heartbeat function is enabled, the chip presents the CSO signal to the CI + / CI – pair. After a successful transmission onto the network media, the chip presents the CSO signal within 11 BT$\pm$ 5 BT of the end of activity on the DO + / DO – pair. The CSO signal is presented for 10 BT$\pm$ 5 BT, after which the chip presents an IDL on the CI + / CI – pair and returns to the idle state.

Link Integrity Functions

In the absence of receive traffic, the twisted-pair receiver on the chip can detect periodic link-integrity pulse is a 100ns high signal with pre-distortion followed by a return to idle. The chip provides a link-integrity reception window, during which a link pulse is expected in the absence of receive traffic. The link-integrity window nominally opens 6.5ms after the receipt of a link-integrity pulse or the end of a data frame. The window closes nominally 104ms after the receipt of a link-integrity pulse or the end of a data frame. If a link pulse is received before the link-integrity reception window opens, it is ignored. If no link-integrity pulse is received while the link-integrity reception window is open, there is a link failure. The RLED indicator is turned off, and the chip's transmit, loopback, and receive functions are disabled. If a link-integrity pulse or receive traffic is received while the link-integrity reception window is open, the timers involved are reset. Once the DM9095 has detected a link failure, one of two events must occur before the DM9095 re-enables transmission and reception of data. The first possible event is the reception of two consecutive link-integrity pulses that both fall within the link-integrity reception window and are separated by at least a nominal 6.5ms. The second possible event is the reception of a data packet from the twisted pair. With either of these events, the TPMAU enters a wait state and continues to disable loopback, transmit, and receive functions. This continues until the DM9095 determines that there is no traffic going in either the transmit or receive direction and then enters the idle state. When the link integrity function is enabled, the DM9095 also transmits link-integrity pulses onto the transmit twisted-pair link. In the absence of transmit traffic, a link-integrity pulse is transmitted at a nominal rate of once per 16ms. Link-integrity pulses continue to be transmitted when the part is jabbed by the watchdog timer or there is link-integrity failure.

Auto-Polarity Detection and Correction Functions

The DM9095 can determine if the receive twisted pair has been wired with a polarity reversal. If so, the DM9095 automatically corrects for this error condition, when the correction function is enabled. Also, the AP pin itself can be connected to an LED to display the status of the polarity of the receive twisted pair. When enabled, the DM9095 powers up the function in the normal state and determines if the receive wires are reversed. The DM9095 examines either the IDL pulse at the end of each receive packet or the link pulse when the link integrity function is enabled and uses this information to sense the polarity. If the DM9095 determines that the incoming IDL pulse is of the proper polarity, it remains in normal state. If the DM9095 detects two consecutive reverse IDL pulses or two reverse link pulses, it enters reverse state. If the DM9095 determines that the polarity of the link is reversed, it internally corrects for the polarity, ensuring that all follow-on packets are sent up the AUI with the correct polarity.

Automatic AUI and RJ45 Connector Selection Functions

The chip provides the designer of a 10BASE-T Ethernet interface card with the ability to design a card without having to provide a switch or jumper array to change between AUI and twisted-pair connections. The DM9095 provides automatic changeover whenever the external cable connection is changed. When the link integrity function is enabled and twisted-pair cable is disconnected, all incoming receive signals disappear and the device places the CI + / CI – and DI + / DI – outputs in their high-impedance state. In addition, DO + / DO – inputs are high-impedance inputs.

Power-Down Mode Function

The power-down function is ideal for embedded, laptop computer applications. In power-down mode, the chip pulls within 10uA. When the device is reactivated from power-down mode, normal transceiver operation will resume after the 3.2ms calibration sequence is completed.

Power-On Reset Function

The DM9095 uses a power-on reset sequence to place itself into a known digital state, to allow the analog sections to stabilize, and to calibrate the internal delay line. Depending on the power-down condition, initialization requires the following lengths of time:

- Power-on reset: 3.2 ms
- Power-down mode: 3.2 ms

Crystal Oscillator

An external TTL-Level clock can be applied to the OSC1 pin which is crystal oscillator input. A resistor should be added in series with the clock source to limit the amplitude of the voltage swing seen by the pin. A 500Ω resistor works well in most cases.

LED Status Functions

The LED drivers require an external resistor in series with the LED, which is in turn connected to VDD. The driver pulls the pin low to light the LED and can sink up to 15mA of drive current from the resistor with an output impedance of less than 50Ω. The DM9095 provides three types LED drivers, as follows. Output LED Drivers: The LED outputs XLED, RLED, JLED, and CLED are output LED drivers. These signals are used for status information only. XLED drives high when the DM9095 is transmitting a packet. XLED is not asserted if the DM9095 has detected a jabber function or is in a link-fail state. RLED drives high when the DM9095 is receiving a packet. RLED is not asserted when the DM9095 is in a link-fail state. JLED drives low when the DM9095 has detected a jabber condition. CLED drives low when the DM9095 has detected a collision condition. Sampled LED Driver: The AP pin is used to set the configuration of the DM9095 and drive the LED status indicators. Every 26ms, the pin is configured as an input pin for 6.5• s. During this time, it is sampled by the DM9095. Outside the sampling window, the driver is placed in an output state and used to drive the LED indicators. AP is driven low to indicate that a reversed twisted pair has been detected on the receive circuit and corrected. If AP is tied low, DM9095 disables the auto-polarity function; when AP is pulled high externally, the function is enabled. Input / Output LED Driver: LI-pin is an input/output pin, depending on the mode selection. When configured as an input pin, LI-controls the link integrity test option. If LI- is connected to GND, the link integrity function is enabled. If LI- is connected to VDD or left floating (internal pull-high), the link integrity function is disabled. When configured as an output pin, the pin drives low for link-fail state and drives high for link-pass state. The output pin can drive an LED status indicator.

Power

There are six power connections to the DM9095, including three VDD and three GND connections. Pins 1 and 28 are used for analog supplies, including squelch circuits, receiver, and the internal delay circuit. Pins 10 and 14 are used for digital circuits, the I/O buffer, the control logic for analog circuits, and the crystal oscillator circuit. Pins 18 and 23 are used for the Twisted Pair driver output buffer.

Operating Modes

The mode selection pins are used to select one of eight operating modes. These modes are summarized in the table below.

The modes referred to in the table are the following:

- Heartbeat: A Yest means that the heartbeat function is enabled; A No means the heartbeat function is disabled.
- Line Length: “Extended” indicates that TP receive squelch thresholds have been lowered to 300mV for use with longer line lengths; Normal indicates that the standard 10BASE-T TP receive squelch threshold of 450mV will be used.
- LI-: The LI- pin can be configured to be an input pin, whereby the link-integrity function can be enabled or disabled. The LI- pin can also be configured as an output pin to indicate the status of the link, where the link-integrity is enabled.

Mode	MD0	MD1	MD2	Mode Description			
				Heartbeat	Line Length	LI-	Application
0	0	0	0	No	Extended	I	Long wire TP
1	0	0	1	No	Normal	I	Normal wire TP
2	0	1	0	No	Normal	O	LI pin LED output
3	0	1	1	Poer-down mode			
4	1	0	0	Yes	Extended	I	Long wire TP
5	1	0	1	Yes	Normal	I	Normal wire TP
6	1	1	0	Yes	Normal	O	LI pin LED output
7	1	1	1	Power-down mode			

AC Electrical Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit
Transmit Timing					
t_{TD}	Transmit delay from $DO^{\pm}$ to $TPO^{\pm}$	0		200	ns
t_{TLB}	Loopback delay from $DO^{\pm}$ to $DI^{\pm}$	0		500	ns
t_{TPDY}	DTPO - to TPO + and DTPO + to TPO - delay	47		53	ns
t_{TOFF}	DO + high to idle time	200			ns
t_{TIDL}	TPO + high to idle time	250		350	ns
Receive Timing					
t_{RD}	Receive delay from $TPI^{\pm}$ to $DI^{\pm}$	0		500	ns
t_{ROFF}	TPI + high to idle time	200			ns
t_{RIDL}	DI + high to idle time	250		350	ns
Collision Timing					
t_{CB}	Collision turn-on time	0		900	ns
t_{CE}	Collision turn-off time	0		900	ns
t_{CLB}	Loopback delay when switching from $DO^{\pm}$ to $TPI^{\pm}$	1000		1600	ns
t_{CIDL}	CI + high to idle time	250		350	ns
t_{CPH}	Collision high-pulse width	40	50	60	ns
t_{CP}	Collision period	80	100	120	ns
Jabber Timing					
t_{JMT}	Maximum transmit time for $TPO^{\pm}$	45	50	55	ms
t_{JCB}	Time from Jabber to enable $CI^{\pm}$ output	0		900	ns
t_{JU}	Unjab time	250	450	750	ms

AC Electrical Characteristics (continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit
Link Integrity Timing					
t_{LP}	Transmitted link integrity pulse period	8	16	24	ms
t_{LPWT}	Link integrity pulse width for TPO +	80	100	120	ns
t_{LPWD}	Link integrity pulse width for DTPO$^{\pm}$	40	50	60	ns
Heartbeat Timing					
t_{HD}	Heartbeat turn-on time	600		1600	ns
t_{HCS}	Heartbeat active time for CI$^{\pm}$ output	500		1500	ns
LED Timing					
t_{XSET}	XLED turn-off time			10	• s
t_{XOFF}	XLED off time	90		110	ms
t_{XON}	XLED minimum on time	4		8	ms
t_{ROFF}	RLED off time	90		110	ms
t_{RON}	RLED minimum on time	4		8	ms
t_{RLFSET}	RLED turn-off time for link fail	50		150	ms
t_{RLFOFF}	RLED off time for link fail				
t_{RLFON}	RLED on time for link success	0.5		1.5	s
t_{CSET}	CLED turn-on time			10	• s
t_{CON}	CLED nominal on time	10		20	ms
t_{JSET}	JLED turn-on time			10	• s
t_{JON}	JLED on time	250		750	ms

Timing Waveforms

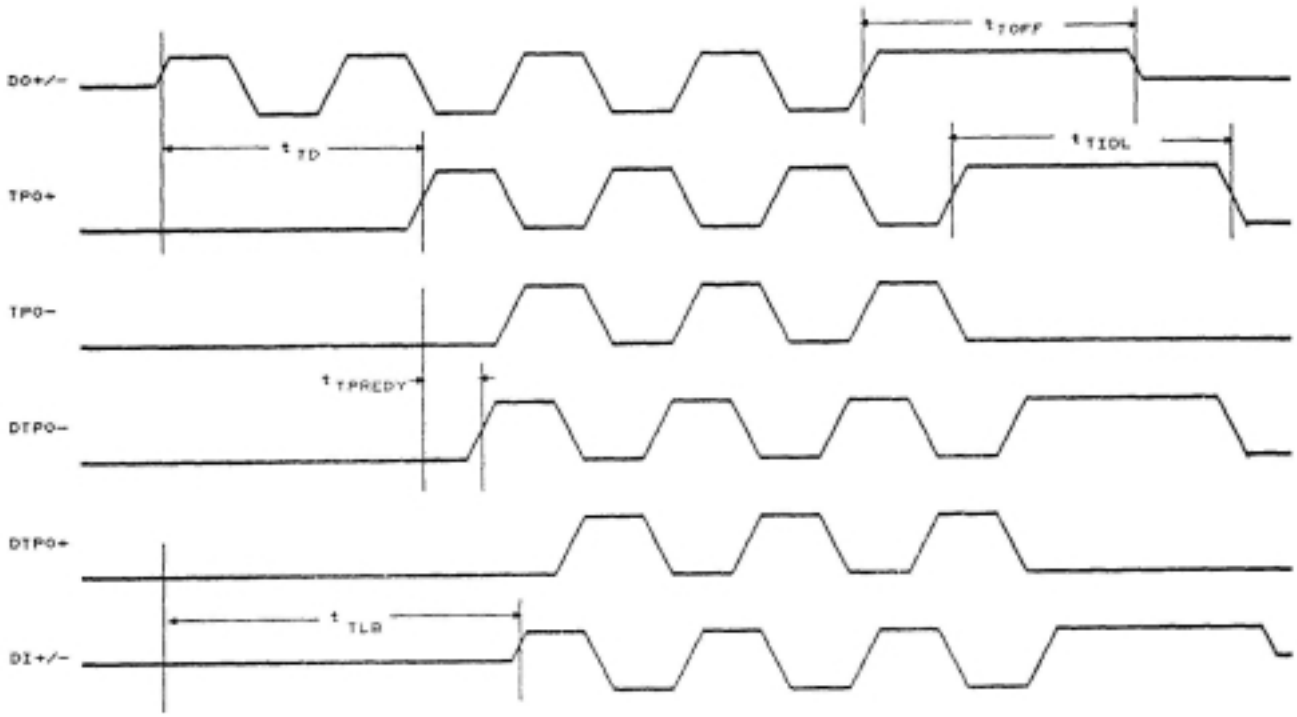


Figure 6. Transmit timing

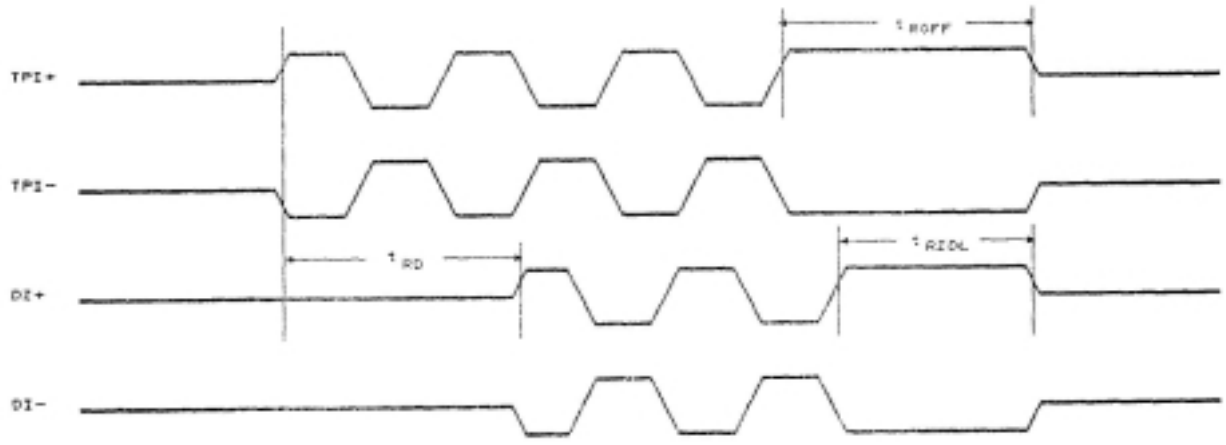


Figure 7. Receive timing

Timing Waveforms (continued)

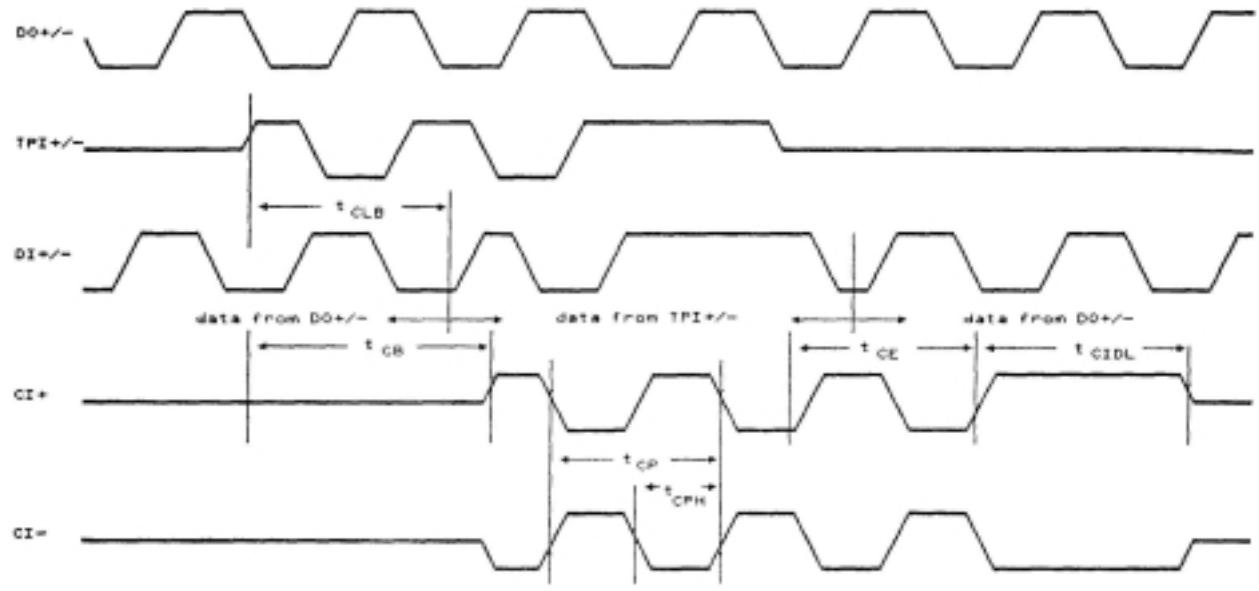


Figure 8. Collision timing

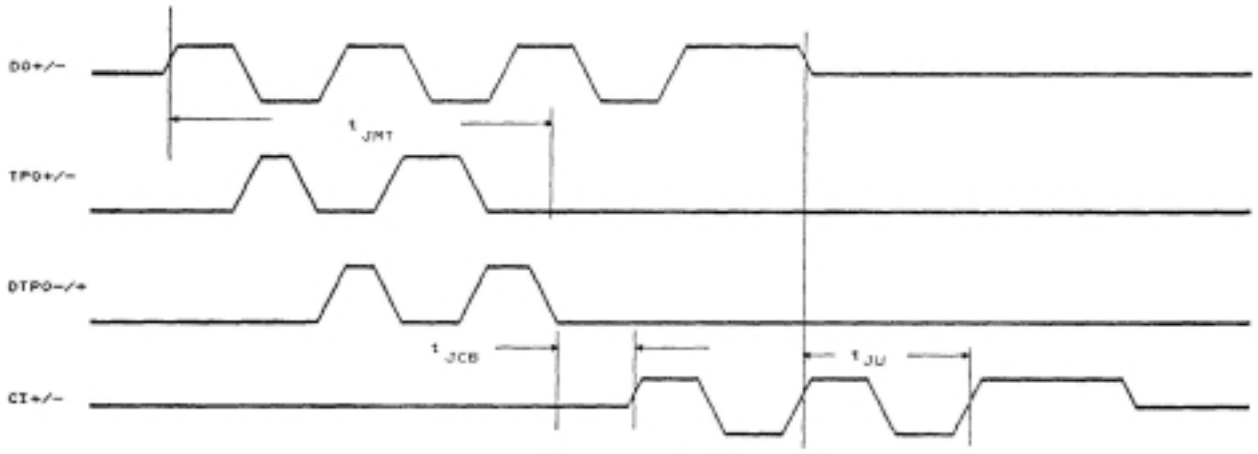


Figure 9. Jabber timing

Timing Waveforms (continued)

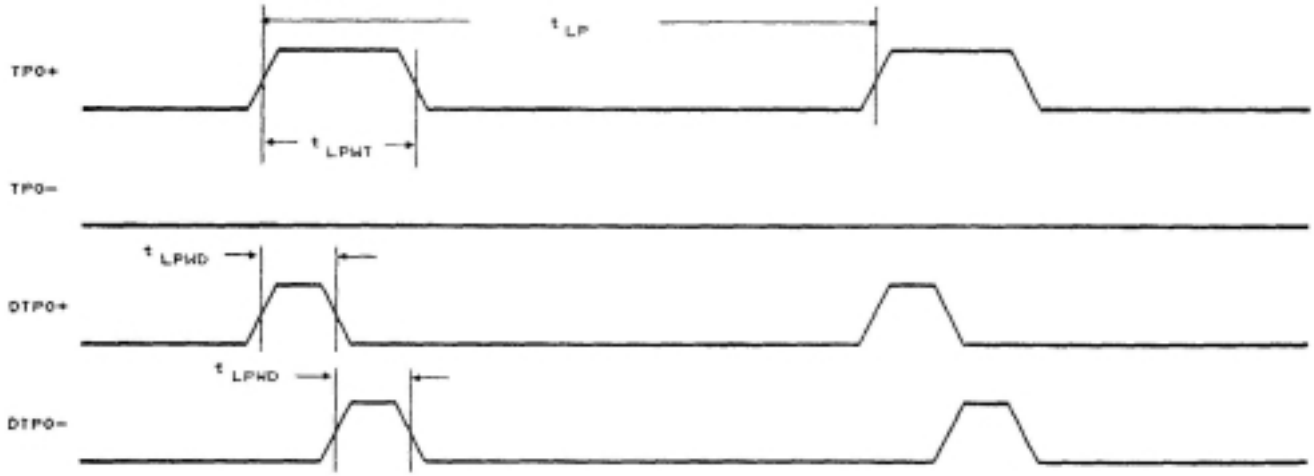


Figure 10. Transmitted link integrity pulse timing

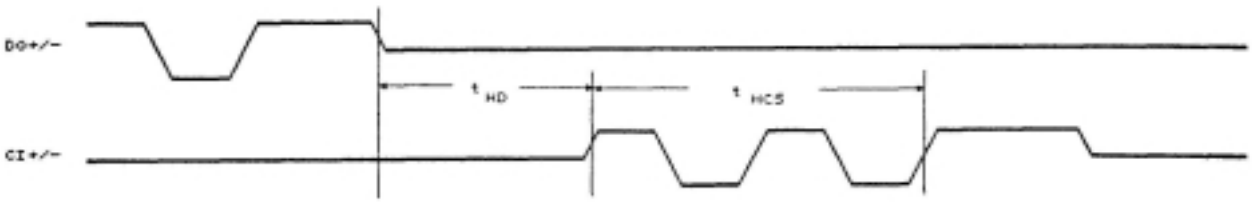


Figure 11. Heartbeat timing

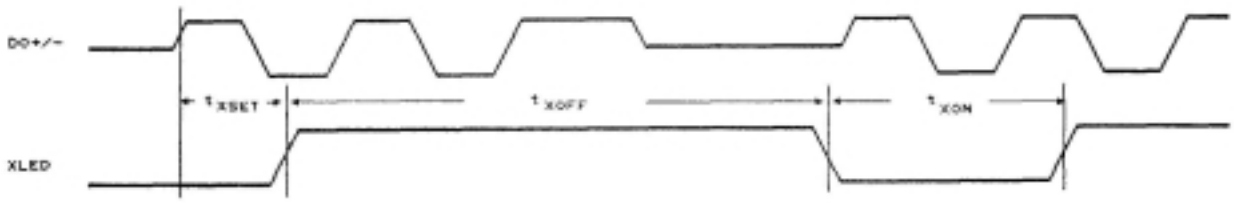


Figure 12. XLED timing

Timing Waveforms (continued)

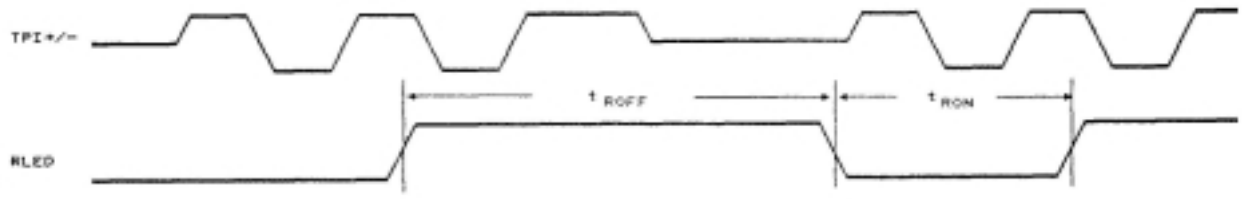


Figure 13. RLED timing for consecutive receive packets

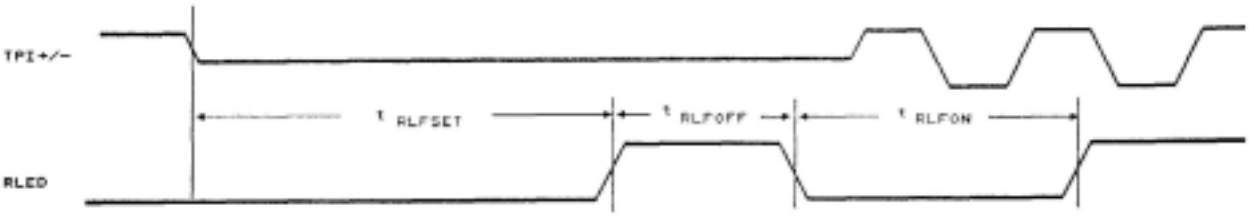


Figure 14. RLED timing for link fail and link success

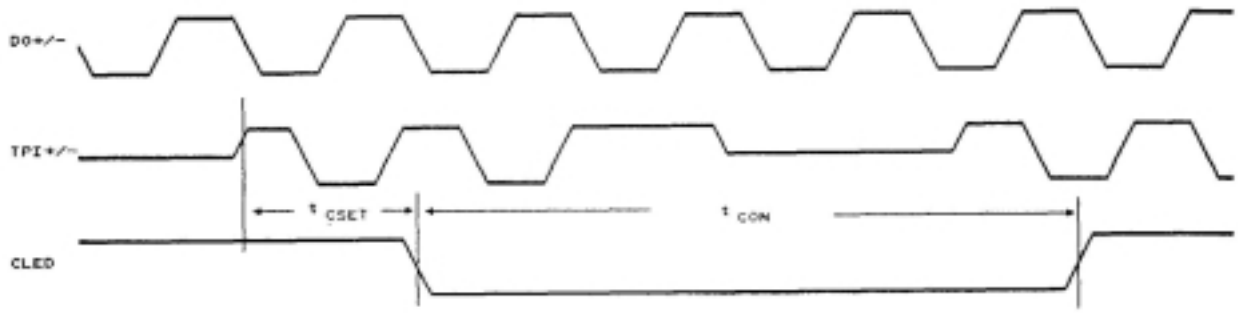


Figure 15. CLED timing

Timing Waveforms (continued)

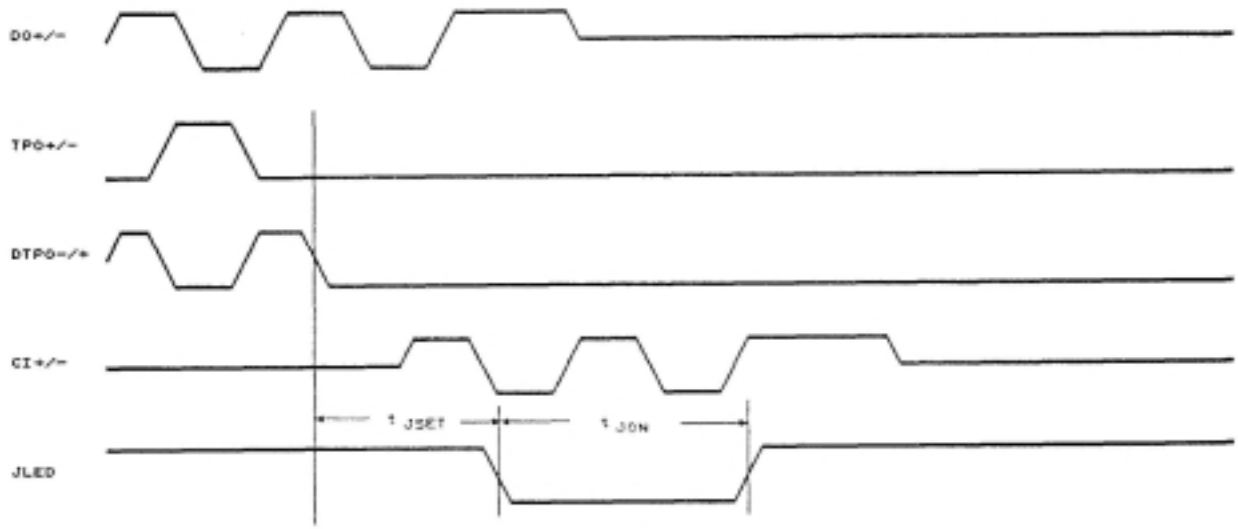
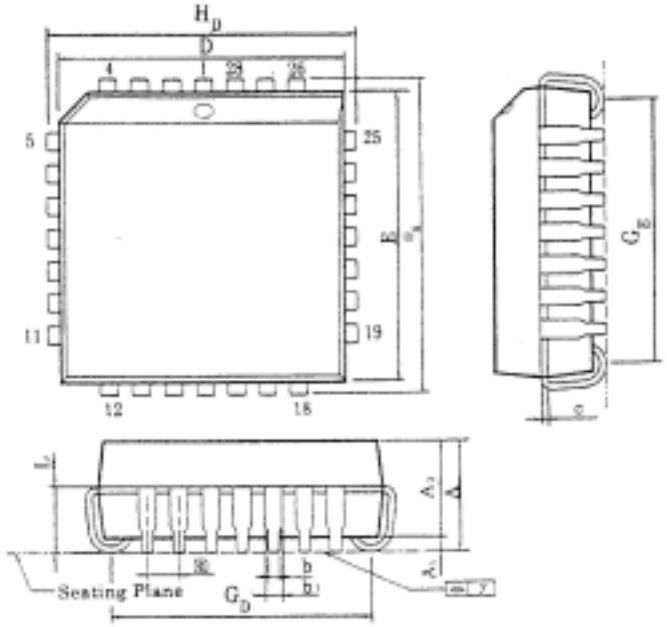


Figure 16. JLED timing

Package Information

PLCC 28L Outline Dimensions **unit: inch/mm**



Symbol	Dimensions in inches	Dimensions in mm
A	0.185 Max.	4.70 Max.
A_1	0.020 Min.	0.51 Min.
A_2	0.150 ± 0.005	3.81 ± 0.13
b_1	$0.028^{+0.004}_{-0.002}$	$0.71^{+0.10}_{-0.05}$
b	$0.018^{+0.004}_{-0.002}$	$0.46^{+0.10}_{-0.05}$
c	$0.010^{+0.004}_{-0.002}$	$0.25^{+0.10}_{-0.05}$
D	0.453 ± 0.010	11.51 ± 0.25
E	0.453 ± 0.010	11.51 ± 0.25
e	0.050 ± 0.006	1.27 ± 0.15
G_D	0.410 ± 0.020	10.41 ± 0.51
G_E	0.410 ± 0.020	10.41 ± 0.51
H_D	0.490 ± 0.010	12.45 ± 0.25
H_E	0.490 ± 0.010	12.45 ± 0.25
L	0.100 ± 0.010	2.54 ± 0.25
y	0.006 Max.	0.15 Max.

Note:

1. **Dimension D & E do not include resin fin.**
2. **Dimensions G_D & G_E are for PC Board surface mount pad pitch design reference only.**

Ordering Information

Part Number	Pin Count	Package
DM9095L	28	PLCC

Disclaimer

The information appearing in this publication is believed to be accurate. Integrated circuits sold by DAVICOM Semiconductor are covered by the warranty and patent indemnification provisions stipulated in the terms of sale only. DAVICOM makes no warranty, express, statutory, implied or by description regarding the information in this publication or regarding the information in this publication or regarding the freedom of the described chip(s) from patent infringement. FURTHER, DAVICOM MAKES NO WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PURPOSE. DAVICOM deserves the right to halt production or alter the specifications and prices at any time without notice. Accordingly, the reader is cautioned to verify that the data sheets and other information in this publication are current before placing orders. Products described herein are intended for use in normal commercial applications. Applications involving unusual environmental or reliability requirements, e.g. military equipment or medical life support equipment, are specifically not recommended without additional processing by DAVICOM for such applications. Please note that application circuits illustrated in this document are for reference purposes only.

DAVICOM's terms and conditions printed on the order acknowledgment govern all sales by DAVICOM. DAVICOM will not be bound by any terms inconsistent with these unless DAVICOM agrees otherwise in writing. Acceptance of the buyer's orders shall be based on these terms.

Company Overview

DAVICOM Semiconductor, Inc. develops and manufactures integrated circuits for integration into data communication products. Our mission is to design and produce IC products that re the industry's best value for Data, Audio, Video, and Internet/Intranet applications. To achieve this goal, we have built an organization that is able to develop chipsets in response to the evolving technology requirements of our customers while still delivering products that meet their cost requirements.

Products

We offer only products that satisfy high performance requirements and which are compatible with major hardware and software standards. Our currently available and soon to be released products are based on our proprietary designs and deliver high quality, high performance chipsets that comply with modem communication standards and Ethernet networking standards.

Contact Windows

For additional information about DAVICOM products, contact the sales department at:

Headquarters

Hsin-chu Office:
3F, No. 7-2, Industry E. Rd., IX,
Science-based Park,
Hsin-chu City, Taiwan, R.O.C.
TEL: 886-3-5798797
FAX: 886-3-5798858

Taipei Sales & Marketing Office:
8F, No. 3, Lane 235, Bao-chiao Rd.,
Hsin-tien, Taipei, Taiwan, R.O.C.
TEL: 886-2-29153030
FAX: 886-2-29157575
Email: sales@davicom.com.tw

Davicom USA

Sunnyvale, California
1135 Kern Ave., Sunnyvale,
CA94085, U.S.A.
TEL: 1-408-7368600
FAX: 1-408-7368688
Email: sales@davicom8.com

WARNING
Conditions beyond those listed for the absolute maximum may destroy or damage the products. In addition, conditions for sustained periods at near the limits of the operating ranges will stress and may temporarily (and permanently) affect and damage structure, performance and/or function.