

# FDMC86260

## N-Channel Power Trench® MOSFET 150 V, 16 A, 34 mΩ

### Features

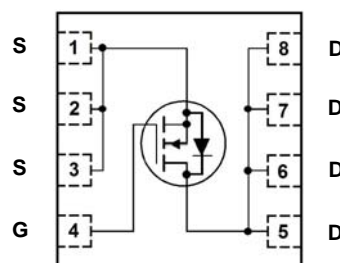
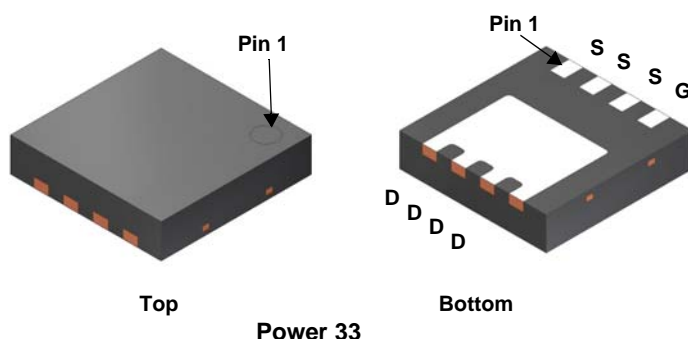
- Max  $r_{DS(on)}$  = 34 mΩ at  $V_{GS} = 10$  V,  $I_D = 5.4$  A
- Max  $r_{DS(on)}$  = 44 mΩ at  $V_{GS} = 6$  V,  $I_D = 4.8$  A
- High performance technology for extremely low  $r_{DS(on)}$
- 100% UIL Tested
- Termination is Lead-free
- RoHS Compliant

### General Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced Power Trench® process that has been especially tailored to minimize the on-state resistance and yet maintain superior switching performance.

### Application

- DC-DC Conversion



### MOSFET Maximum Ratings $T_A = 25$ °C unless otherwise noted

Symbol	Parameter	Ratings	Units
$V_{DS}$	Drain to Source Voltage	150	V
$V_{GS}$	Gate to Source Voltage	±20	V
$I_D$	Drain Current -Continuous $T_C = 25$ °C	16	A
	-Continuous $T_A = 25$ °C (Note 1a)	5.4	
	-Pulsed	48	
$E_{AS}$	Single Pulse Avalanche Energy (Note 3)	121	mJ
$P_D$	Power Dissipation $T_C = 25$ °C	54	W
	Power Dissipation $T_A = 25$ °C (Note 1a)	2.3	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	°C

### Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case (Note 1)	2.3	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	53	

### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMC86260	FDMC86260	Power33	13 "	12 mm	3000 units

**Electrical Characteristics**  $T_J = 25\text{ }^{\circ}\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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**Off Characteristics**

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250\text{ }\mu\text{A}$ , $V_{GS} = 0\text{ V}$	150			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , referenced to $25\text{ }^{\circ}\text{C}$		110		mV/ $^{\circ}\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 120\text{ V}$ , $V_{GS} = 0\text{ V}$			1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{ V}$ , $V_{DS} = 0\text{ V}$			$\pm 100$	nA

**On Characteristics**

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$ , $I_D = 250\text{ }\mu\text{A}$	2	2.7	4	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , referenced to $25\text{ }^{\circ}\text{C}$		-9		mV/ $^{\circ}\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{ V}$ , $I_D = 5.4\text{ A}$		27	34	m $\Omega$
		$V_{GS} = 6\text{ V}$ , $I_D = 4.8\text{ A}$		31	44	
		$V_{GS} = 10\text{ V}$ , $I_D = 5.4\text{ A}$ , $T_J = 125\text{ }^{\circ}\text{C}$		55	69	
$g_{FS}$	Forward Transconductance	$V_{DD} = 10\text{ V}$ , $I_D = 5.4\text{ A}$		19		S

**Dynamic Characteristics**

$C_{iss}$	Input Capacitance	$V_{DS} = 75\text{ V}$ , $V_{GS} = 0\text{ V}$ , $f = 1\text{ MHz}$		1000	1330	pF
$C_{oss}$	Output Capacitance			105	140	pF
$C_{rss}$	Reverse Transfer Capacitance			4.8	10	pF
$R_g$	Gate Resistance		0.1	0.6	1.8	$\Omega$

**Switching Characteristics**

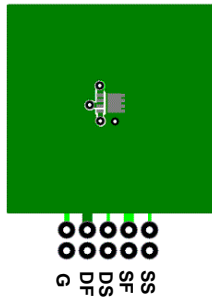
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 75\text{ V}$ , $I_D = 5.4\text{ A}$ , $V_{GS} = 10\text{ V}$ , $R_{GEN} = 6\text{ }\Omega$		9.5	19	ns
$t_r$	Rise Time			2	10	ns
$t_{d(off)}$	Turn-Off Delay Time			17	30	ns
$t_f$	Fall Time			3.3	10	ns
$Q_{g(TOT)}$	Total Gate Charge	$V_{GS} = 0\text{ V to }10\text{ V}$	$V_{DD} = 75\text{ V}$ , $I_D = 5.4\text{ A}$	15	21	nC
$Q_{g(TOT)}$	Total Gate Charge	$V_{GS} = 0\text{ V to }6\text{ V}$		9.7	14	nC
$Q_{gs}$	Total Gate Charge			4.0		nC
$Q_{gd}$	Gate to Drain "Miller" Charge			3.1		nC

**Drain-Source Diode Characteristics**

$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}$ , $I_S = 5.4\text{ A}$ (Note 2)		0.77	1.3	V
		$V_{GS} = 0\text{ V}$ , $I_S = 1.9\text{ A}$ (Note 2)		0.72	1.2	V
$t_{rr}$	Reverse Recovery Time	$I_F = 5.4\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$		64	102	ns
$Q_{rr}$	Reverse Recovery Charge			85	137	nC

Notes:

1.  $R_{\theta JA}$  is determined with the device mounted on a 1 in<sup>2</sup> pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a. 53  $^{\circ}\text{C}/\text{W}$  when mounted on a 1 in<sup>2</sup> pad of 2 oz copper



b. 125  $^{\circ}\text{C}/\text{W}$  when mounted on a minimum pad of 2 oz copper

2. Pulse Test: Pulse Width < 300  $\mu\text{s}$ , Duty cycle < 2.0%.

3.  $E_{AS}$  of 121 mJ is based on starting  $T_J = 25\text{ }^{\circ}\text{C}$ ,  $L = 3\text{ mH}$ ,  $I_{AS} = 9\text{ A}$ ,  $V_{DD} = 150\text{ V}$ ,  $V_{GS} = 10\text{ V}$ . 100% test at  $L = 0.1\text{ mH}$ ,  $I_{AS} = 22\text{ A}$ .

## Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

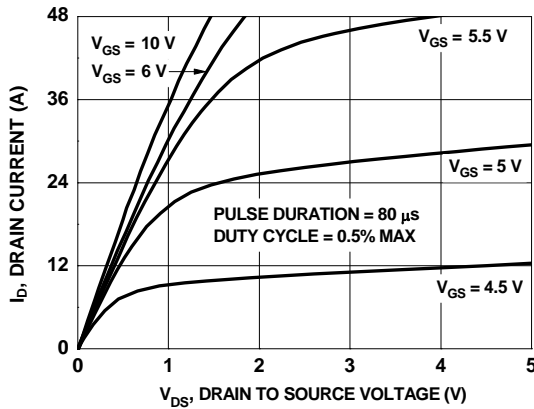


Figure 1. On-Region Characteristics

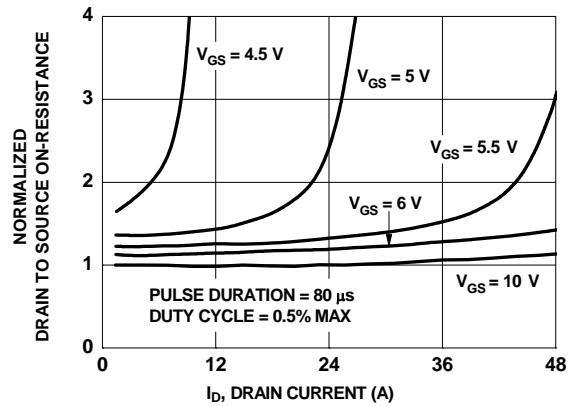


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

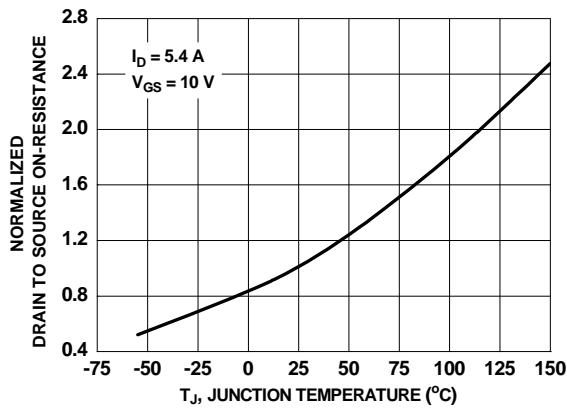


Figure 3. Normalized On-Resistance vs Junction Temperature

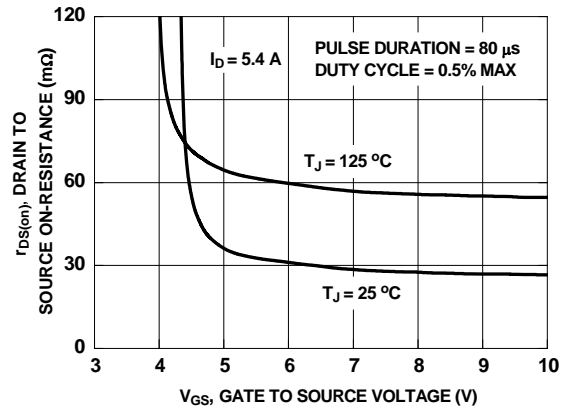


Figure 4. On-Resistance vs Gate to Source Voltage

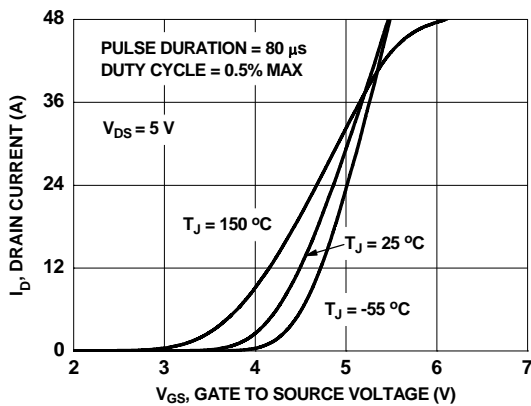


Figure 5. Transfer Characteristics

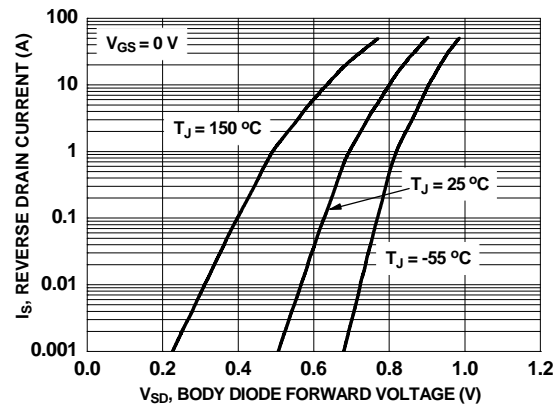


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

## Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

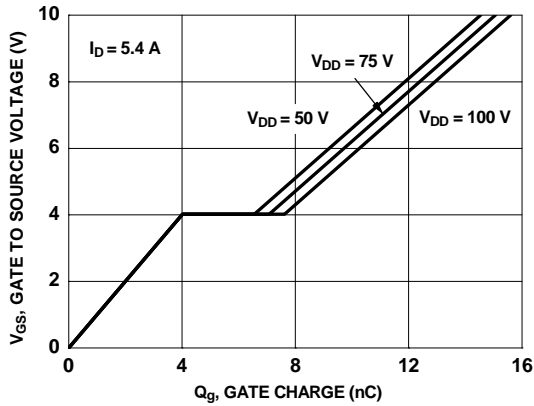


Figure 7. Gate Charge Characteristics

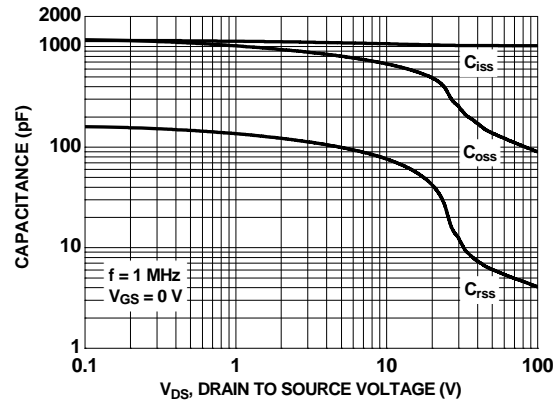


Figure 8. Capacitance vs Drain to Source Voltage

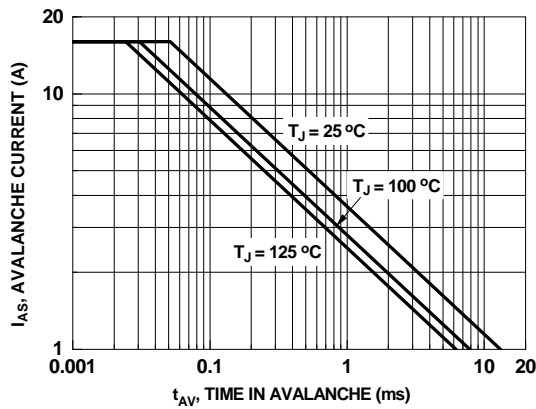


Figure 9. Unclamped Inductive Switching Capability

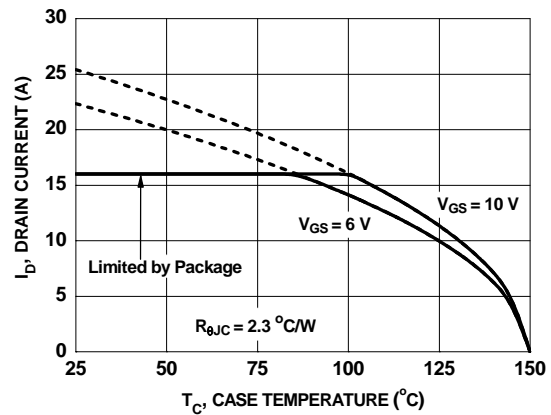


Figure 10. Maximum Continuous Drain Current vs Case Temperature

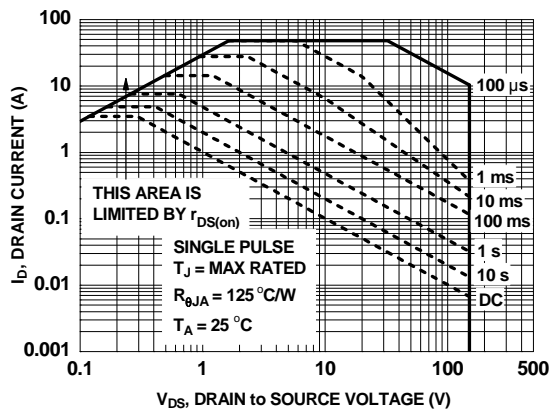


Figure 11. Forward Bias Safe Operating Area

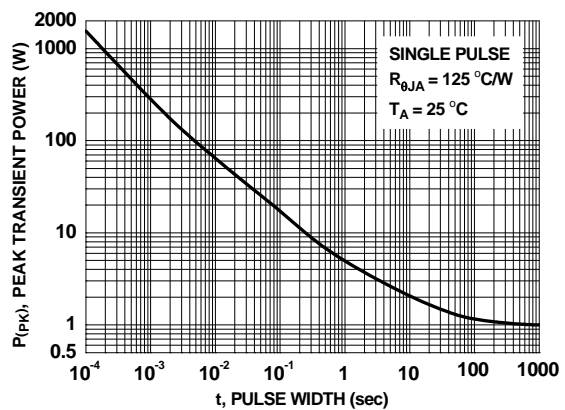
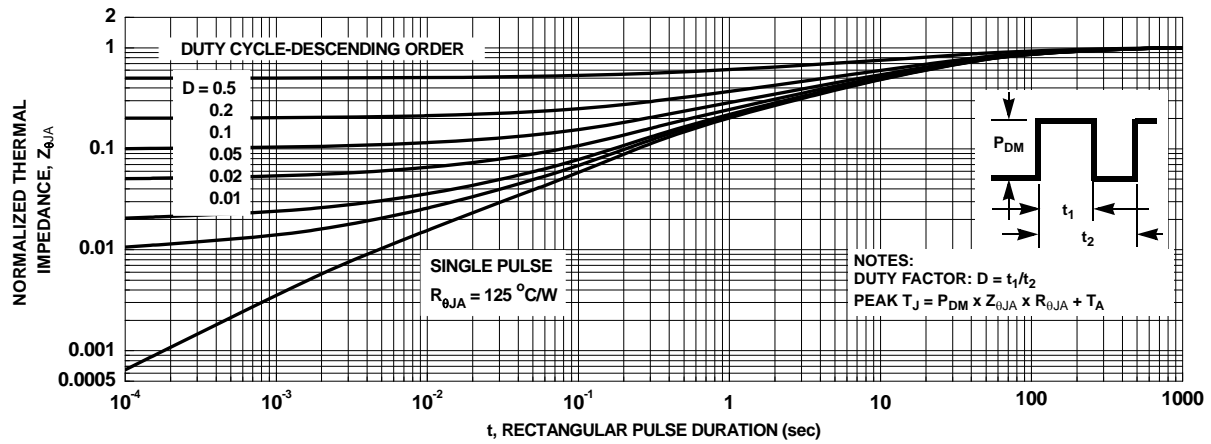
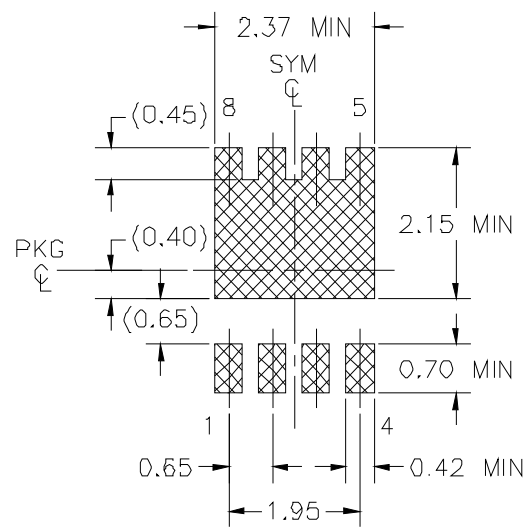
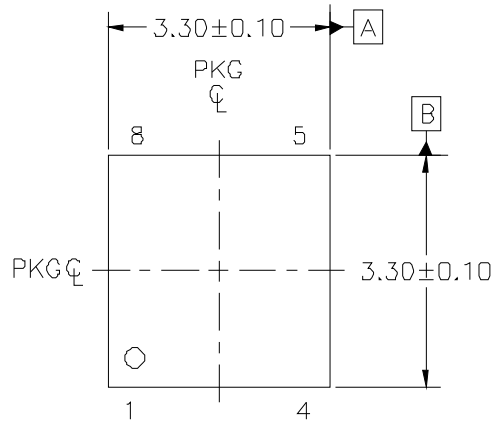


Figure 12. Single Pulse Maximum Power Dissipation

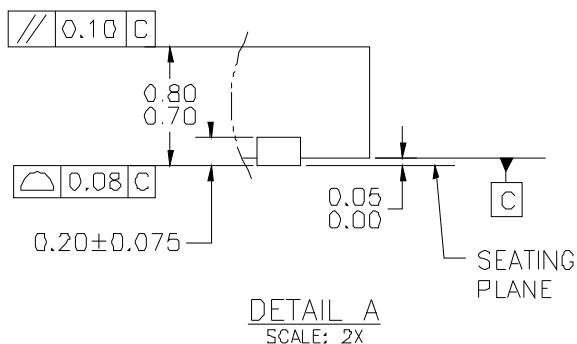
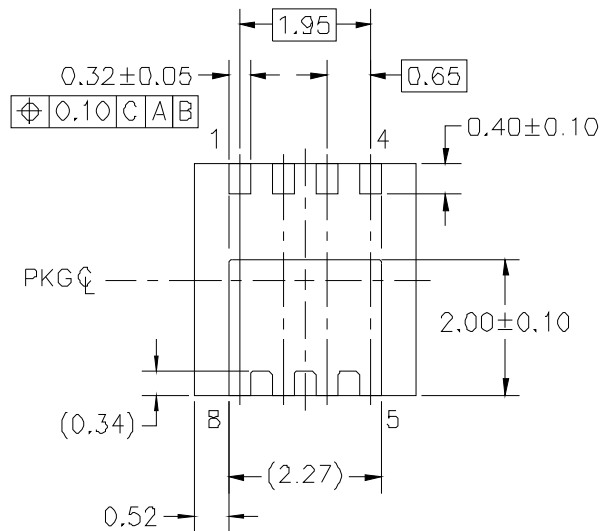
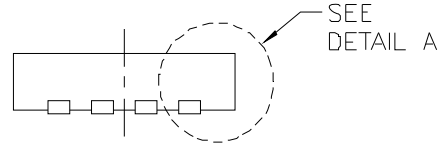
# Typical Characteristics $T_J = 25\text{ }^{\circ}\text{C}$ unless otherwise noted



# Dimensional Outline and Pad Layout



LAND PATTERN  
RECOMMENDATION





NOTES: UNLESS OTHERWISE SPECIFIED

- A) PACKAGE STANDARD REFERENCE:  
JEDEC MO-240, ISSUE A, VAR. BA,  
DATED OCTOBER 2002.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE BURRS  
OR MOLD FLASH. MOLD FLASH OR  
BURRS DOES NOT EXCEED 0.10MM.
- D) DIMENSIONING AND TOLERANCING PER  
ASME Y14.5M-1994.

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No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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