

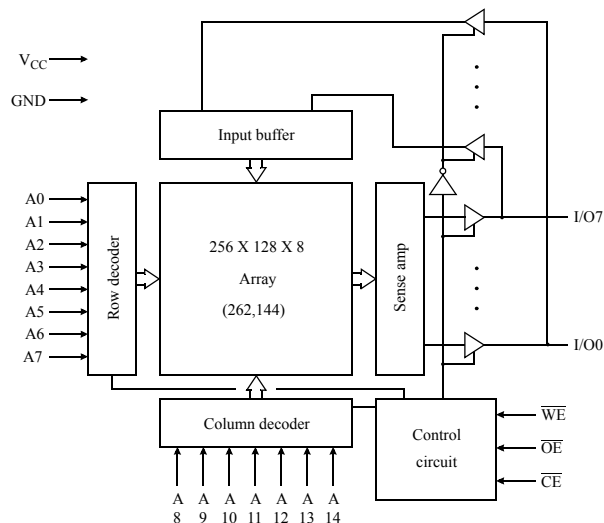


5V 32K X 8 CMOS SRAM (Common I/O)

Features

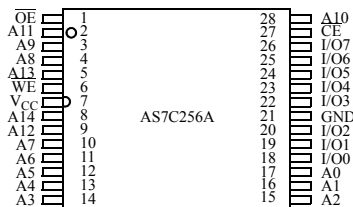
- Pin compatible with AS7C256
- Industrial and commercial temperature options
- Organization: 32,768 words × 8 bits
- High speed
 - 10/12/15/20 ns address access time
 - 5, 6, 7, 8 ns output enable access time
- Very low power consumption: ACTIVE
 - 412.5 mW max @ 10 ns
- Very low power consumption: STANDBY
 - 11 mW max CMOS I/O
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ inputs
- TTL-compatible, three-state I/O
- 28-pin JEDEC standard packages
 - 300 mil SOJ
 - 8 × 13.4 mm TSOP 1
- ESD protection ≥ 2000 volts
- Latch-up current ≥ 200 mA
- 2.0V Data retention

Logic block diagram

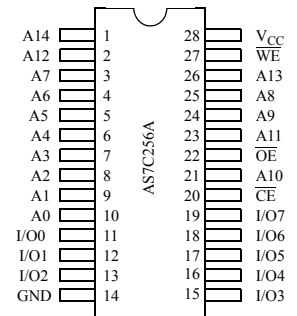


Pin arrangement

28-pin TSOP 1 (8×13.4 mm)



28-pin SOJ (300 mil)



Selection guide

	-10	-12	-15	-20	Unit
Maximum address access time	10	12	15	20	ns
Maximum output enable access time	5	6	7	8	ns
Maximum operating current	75	70	65	60	mA
Maximum CMOS standby current	2	2	2	2	mA



Functional description

The AS7C256A is a 5.0V high-performance CMOS 262,144-bit Static Random-Access Memory (SRAM) device organized as 32,768 words $\times$ 8 bits. It is designed for memory applications requiring fast data access at low voltage, including Pentium™, PowerPC™, and portable computing. Alliance's advanced circuit design and process techniques permit 5.0V operation without sacrificing performance or operating margins.

The device enters *standby mode* when $\overline{CE}$ is high. CMOS standby mode consumes ≤ 11 mW. Normal operation offers 75% power reduction after initial access, resulting in significant power savings during CPU idle, suspend, and stretch mode.

Equal address access and cycle times (t_{AA} , t_{RC} , t_{WC}) of 10/12/15/20 ns with output enable access times (t_{OE}) of 5, 6, 7, 8 ns are ideal for high-performance applications. The chip enable ($\overline{CE}$) input permits easy memory expansion with multiple-bank memory organizations.

A write cycle is accomplished by asserting chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) LOW. Data on the input pins I/O0-I/O7 is written on the rising edge of $\overline{WE}$ (write cycle 1) or $\overline{CE}$ (write cycle 2). To avoid bus contention, external devices should drive I/O pins only after outputs have been disabled with output enable ($\overline{OE}$) or write enable ($\overline{WE}$).

A read cycle is accomplished by asserting chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) LOW, with write enable ($\overline{WE}$) high. The chip drives I/O pins with the data word referenced by the input address. When chip enable or output enable is high, or write enable is low, output drivers stay in high-impedance mode.

All chip inputs and outputs are TTL-compatible. Operation is from a single 5.0 $\pm$ 0.5V supply. The AS7C256A is packaged in high volume industry standard packages.

Absolute maximum ratings

Parameter	Symbol	Min	Max	Unit
Voltage on V_{CC} relative to GND	V_{t1}	-0.5	+7.0	V
Voltage on any pin relative to GND	V_{t2}	-0.5	$V_{CC} + 0.5$	V
Power dissipation	P_D	—	1.0	W
Storage temperature (plastic)	T_{stg}	-65	+150	°C
Ambient temperature with V_{CC} applied	T_{bias}	-55	+125	°C
DC current into outputs (low)	I_{OUT}	—	20	mA

Stresses greater than those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Truth table

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	Data	Mode
H	X	X	High Z	Standby (I_{SB} , I_{SB1})
L	H	H	High Z	Output disable (I_{CC})
L	H	L	D_{OUT}	Read (I_{CC})
L	L	X	D_{IN}	Write (I_{CC})

Key: X = Don't care, L = Low, H = High



Recommended operating conditions

Parameter		Symbol	Min	Typical	Max	Unit
Supply voltage		V_{CC}	4.5	5.0	5.5	V
Input voltage		V_{IH}^{**}	2.2	—	$V_{CC}+0.5$	V
		V_{IL}^*	-0.5	—	0.8	V
Ambient operating temperature	commercial	T_A	0	—	70	°C
	industrial	T_A	-40	—	85	°C

* V_{IL} min = -1.0V for pulse width less than 5ns.

** V_{IH} max = $V_{CC} + 2.0V$ for pulse width less than 5ns.

DC operating characteristics (over the operating range)¹

Parameter	Sym	Test conditions	-10		-12		-15		-20		Unit	Notes
			Min	Max	Min	Max	Min	Max	Min	Max		
Input leakage current	$ I_{LI} $	$V_{CC} = \text{Max}, V_{in} = \text{GND to } V_{CC}$	—	1	—	1	—	1	—	1	μA	
Output leakage current	$ I_{LO} $	$V_{CC} = \text{Max}, V_{OUT} = \text{GND to } V_{CC}$	—	1	—	1	—	1	—	1	μA	
Operating power supply current	I_{CC}	$V_{CC} = \text{Max}, \overline{CE} \leq V_{IL}$ $f = f_{\text{Max}}, I_{OUT} = 0\text{mA}$	—	75	—	70	—	65	—	60	mA	
Standby power supply current	I_{SB}	$V_{CC} = \text{Max}, \overline{CE} \geq V_{IH}$ $f = f_{\text{Max}}$	—	45	—	45	—	40	—	40	mA	
	I_{SB1}	$V_{CC} = \text{Max}, \overline{CE} \geq V_{CC}-0.2V$ $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC}-0.2V, f = 0$	—	2.0	—	2.0	—	2.0	—	2.0	mA	
Output voltage	V_{OL}	$I_{OL} = 8 \text{ mA}, V_{CC} = \text{Min}$	—	0.4	—	0.4	—	0.4	—	0.4	V	4
	V_{OH}	$I_{OH} = -4 \text{ mA}, V_{CC} = \text{Min}$	2.4	—	2.4	—	2.4	—	2.4	—	V	4

Capacitance ($f = 1\text{MHz}$, $T_A = \text{room temperature}$, $V_{CC} = \text{NOMINAL}$)⁴

Parameter	Symbol	Signals	Test conditions	Max	Unit
Input capacitance	C_{IN}	A, $\overline{CE}$, $\overline{WE}$, $\overline{OE}$	$V_{in} = 0V$	5	pF
I/O capacitance	$C_{I/O}$	I/O	$V_{in} = V_{out} = 0V$	7	pF

Parameter	Symbol	-10		-12		-15		-20		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Read cycle time	t _{RC}	10	—	12	—	15	—	20	—	ns	
Address access time	t _{AA}	—	10	—	12	—	15	—	20	ns	2
Chip enable ($\overline{\text{CE}}$) access time	t _{ACE}	—	10	—	12	—	15	—	20	ns	2
Output enable ($\overline{\text{OE}}$) access time	t _{OE}	—	5	—	6	—	7	—	8	ns	
Output hold from address change	t _{OH}	3	—	3	—	3	—	3	—	ns	4
$\overline{\text{CE}}$ LOW to output in low Z	t _{CLZ}	3	—	3	—	3	—	3	—	ns	3,4
$\overline{\text{CE}}$ HIGH to output in high Z	t _{CHZ}	—	3	—	3	—	4	—	5	ns	3,4
$\overline{\text{OE}}$ LOW to output in low Z	t _{OLZ}	0	—	0	—	0	—	0	—	ns	3,4
$\overline{\text{OE}}$ HIGH to output in high Z	t _{OHZ}	—	3	—	3	—	4	—	5	ns	3,4
Power up time	t _{PU}	0	—	0	—	0	—	0	—	ns	3,4
Power down time	t _{PD}	—	10	—	12	—	15	—	20	ns	3,4

 Rising input
 Falling input
 Undefined output/don't care

The diagram illustrates the timing for a memory read operation. The **Address** signal is shown as a horizontal line that transitions from a low state to a high state. The time from the rising edge of the Address signal to the point where the **D_{out}** signal becomes valid is labeled t_{AA} . The time from the rising edge of the Address signal to the point where the **D_{out}** signal becomes invalid is labeled t_{RC} . The time from the falling edge of the Address signal to the point where the **D_{out}** signal becomes invalid is labeled t_{OH} . The **D_{out}** signal is shown as a horizontal line that transitions from a low state to a high state, labeled "Data valid", and then returns to a low state. The time from the rising edge of the Address signal to the point where the **D_{out}** signal becomes invalid is labeled t_{RC} .

The timing diagram illustrates the relationship between the $\overline{\text{CE}}$, $\overline{\text{OE}}$, D_{out} , and Supply current signals. Key timing parameters are defined as follows:

- t_{RC}^1 : Delay from $\overline{\text{CE}}$ falling edge to $\overline{\text{OE}}$ rising edge.
- t_{OE} : Delay from $\overline{\text{OE}}$ falling edge to D_{out} becoming valid.
- t_{OLZ} : Delay from $\overline{\text{OE}}$ rising edge to D_{out} becoming high-impedance.
- t_{ACE} : Delay from $\overline{\text{CE}}$ falling edge to D_{out} becoming valid.
- t_{CHZ} : Delay from $\overline{\text{OE}}$ rising edge to D_{out} becoming high-impedance.
- t_{CLZ} : Delay from $\overline{\text{CE}}$ falling edge to D_{out} becoming high-impedance.
- t_{PU} : Delay from $\overline{\text{CE}}$ falling edge to Supply current rising to 50%.
- t_{PD} : Delay from $\overline{\text{OE}}$ rising edge to Supply current falling to 50%.

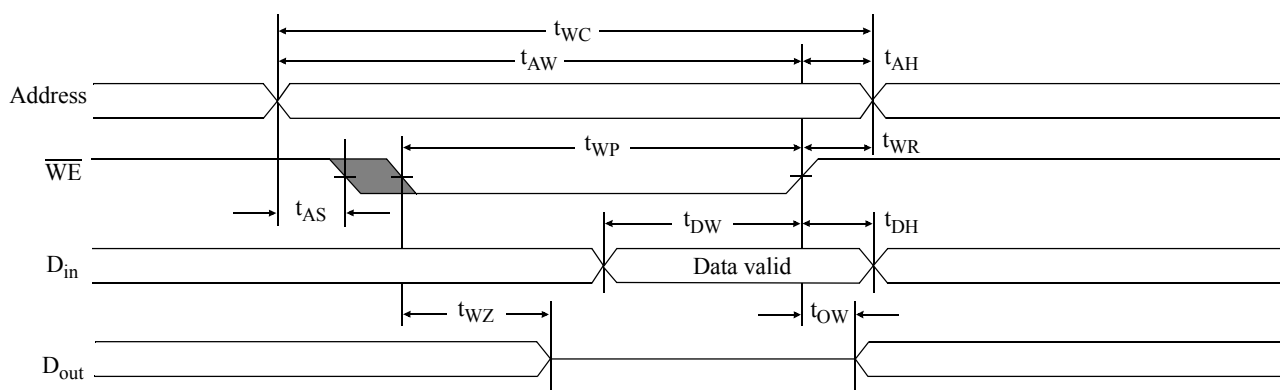
The D_{out} signal is shown as a white box labeled "Data valid" between the t_{OE} and t_{OLZ} intervals. The Supply current signal transitions from a low level to 50% of I_{CC} and then to I_{CC} when $\overline{\text{CE}}$ falls, and back to 50% of I_{SB} when $\overline{\text{OE}}$ rises.



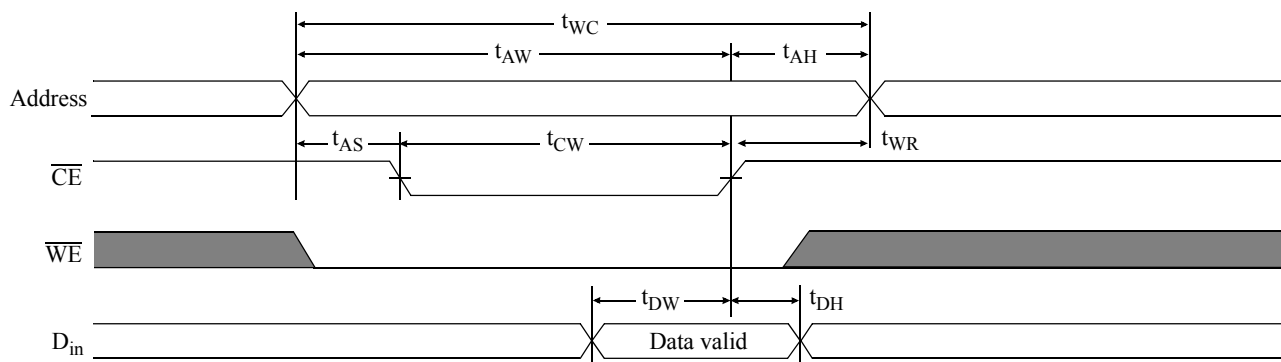
Write cycle (over the operating range)⁹

Parameter	Symbol	-10		-12		-15		-20		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Write cycle time	t_{WC}	10	–	12	–	15	–	20	–	ns	
Chip enable to write end	t_{CW}	8	–	8	–	10	–	12	–	ns	
Address setup to write end	t_{AW}	8	–	8	–	10	–	12	–	ns	
Address setup time	t_{AS}	0	–	0	–	0	–	0	–	ns	
Write pulse width	t_{WP}	7	–	8	–	9	–	12	–	ns	
Write recovery time	t_{WR}	0	–	0	–	0	–	0	–	ns	
Address hold from end of write	t_{AH}	0	–	0	–	0	–	0	–	ns	
Data valid to write end	t_{DW}	5	–	6	–	8	–	10	–	ns	
Data hold time	t_{DH}	0	–	0	–	0	–	0	–	ns	3,4
Write enable to output in high Z	t_{WZ}	–	5	–	6	–	7	–	8	ns	3,4
Output active from write end	t_{OW}	3	–	3	–	3	–	3	–	ns	3,4

Write waveform 1 ($\overline{WE}$ controlled)⁹



Write waveform 2 ($\overline{CE}$ controlled)⁹





AC test conditions

- Output load: see Figure B
- Input pulse level: GND to V_{CC} See Figure A.
- Input rise and fall times: 2 ns. See Figure A.
- Input and output timing reference levels: 1.5V.

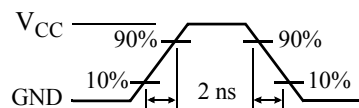


Figure A: Input pulse

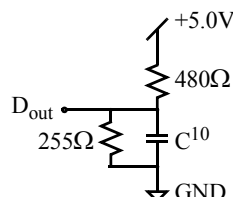
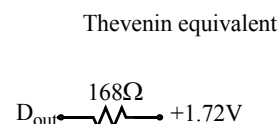


Figure B: Output load



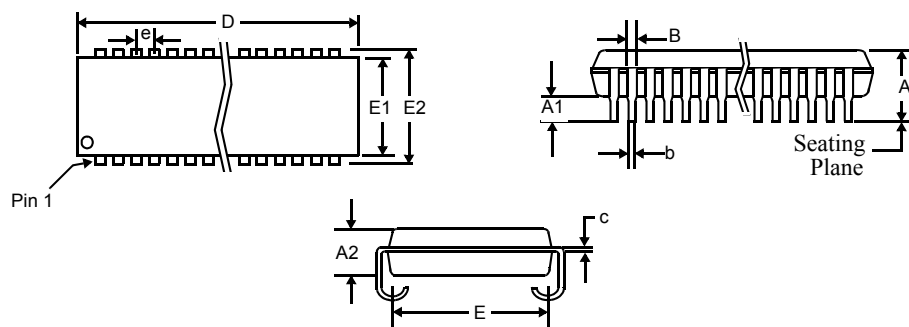
Notes

- 1 During V_{CC} power-up, a pull-up resistor to V_{CC} on $\overline{CE}$ is required to meet I_{SB} specification.
- 2 For test conditions, see *AC Test Conditions*, Figures A, B.
- 3 These parameters are specified with $C_L = 5\text{pF}$, as in Figures B. Transition is measured $\pm 500\text{mV}$ from steady-state voltage.
- 4 This parameter is guaranteed, but not tested.
- 5 $\overline{WE}$ is High for read cycle.
- 6 $\overline{CE}$ and $\overline{OE}$ are Low for read cycle.
- 7 Address valid prior to or coincident with $\overline{CE}$ transition Low.
- 8 All read cycle timings are referenced from the last valid address to the first transitioning address.
- 9 All write cycle timings are referenced from the last valid address to the first transitioning address.
- 10 $C = 30\text{pF}$, except on High Z and Low Z parameters, where $C = 5\text{pF}$.



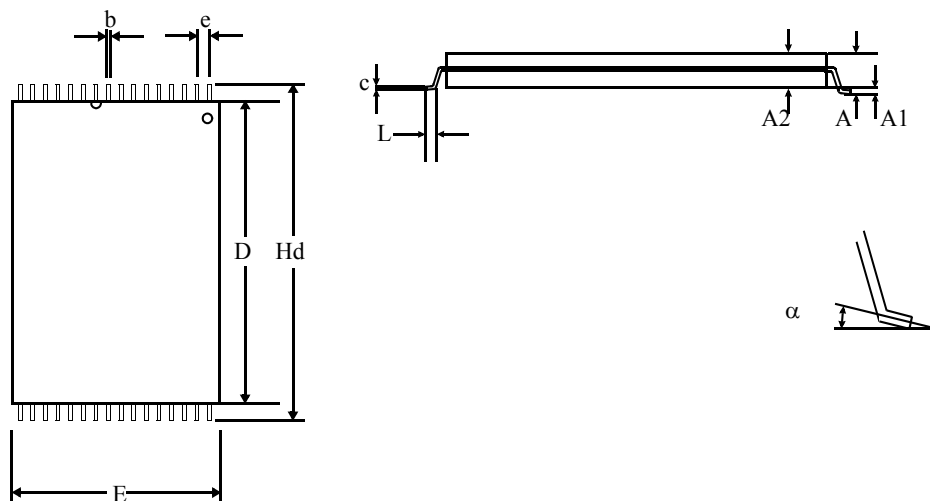
Package diagrams

28-pin SOJ



28-pin SOJ		
	Min	Max
in inches		
A	0.128	0.148
A1	0.026	-
A2	0.095	0.105
B	0.026	0.032
b	0.016	0.020
c	0.007	0.010
D	0.720	0.730
E	0.255	0.275
E1	0.295	0.305
E2	0.330	0.340
e	0.050 BSC	

28-pin TSOP1



28-pin TSOP1 8×13.4 mm		
	Min	Max
A	1.00	1.20
A1	0.05	0.15
A2	0.91	1.05
b	0.17	0.27
c	0.10	0.20
D	11.70	11.90
e	0.55 nominal	
E	7.90	8.10
Hd	13.20	13.60
L	0.50	0.70
α	0°	5°



Ordering information

Package / Access time	Temperature	10 ns	12 ns	15 ns	20 ns
Plastic SOJ, 300 mil	Commercial	AS7C256A-10JC	AS7C256A-12JC	AS7C256A-15JC	AS7C256A-20JC
	Industrial	AS7C256A-10JI	AS7C256A-12JI	AS7C256A-15JI	AS7C256A-20JI
TSOP 8x13.4mm	Commercial	AS7C256A-10TC	AS7C256A-12TC	AS7C256A-15TC	AS7C256A-20TC
	Industrial	AS7C256A-10TI	AS7C256A-12TI	AS7C256A-15TI	AS7C256A-20TI

Note: Add suffix 'N' to the above part number for lead free parts. (Ex. AS7C256A-10JIN)

Part numbering system

AS7C	256A	-XX	X	C or I	X
SRAM prefix	Device number	Access time	Packages: J = SOJ 300 mil T = TSOP 8x13.4mm	Temperature range: C = 0 °C to 70 °C I = -40C to 85C	N= Lead Free Part



AS7C256A



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Part Number: AS7C256A
Document Version: v.1.2

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