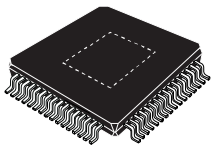
L9907A

FET driver for 3 phase BLDC motor

Data brief



TQFP64 (exposed pad down)

GAPGPS00129

Features

- Supply voltage from 6 V to 36 V for working in 12 V and 24 V systems
- The device can withstand -7 V to 75 V at the FET high-side Driver pins
- Low standby current consumption
- 3.3 V internal regulator supplied by Vcc pin
- Boost regulator for full Rdson down to 6 V and over voltage protection
- 3 low-side + 3 high-side drivers:
  - PWM operation up to 20 kHz
  - Gate driver current adjustable via SPI in 4 steps. Range set via external resistor. Maximum gate controlled current 600 mA
  - Source connection to each MOSFET
- Input pin for each gate driver
- 2-differential current sense amplifiers:
  - Output offset selectable via SPI (0.2*V_{CC} offset for ground shunt resistors connection, 0.5*V_{CC} offset for phase shunt resistors connection)
  - All the amplifier gain factors are programmable (10, 30, 50, 100)

8 MHz, 16-bit SPI:

- Full diagnostic
- Programmable parameters:
  - Cross conduction dead time with a fixed minimum value;
  - 4 current steps driving the PowerMOS gates (25%, 50%, 75%, 100%);
  - Phase or ground selection of current sense amplifier;
  - Gain values for the current sense amplifiers;
  - Zero current output voltage (offset) for the current sense amplifiers;
  - Over voltage threshold selection for single or double battery operation;
  - Short circuit detection thresholds for the low-side and the high-side MOSFETs (drain to source voltage monitor).

Protection and diagnostic:

- FET driver:
  - FET driver supply Undervoltage (UV) diagnostic;
  - Gate to source output voltage limit;
  - Gate to source passive switch off.
- Power supply pins V_B and V_{CC}
  - Overvoltage (OV), Undervoltage (UV) diagnostic and protection
- All logic pins withstand 35 V
- Power MOSFET drain to source voltage drop measurement for overcurrent protection
- Over-temperature diagnostic and shutdown
- Fault status flag output

Table 1: Device summary

Order code	Package	Packing
L9907A	TQFP64 (10x10x1.0 mm)	Tray
L9907ATR		Tape & reel

Contents

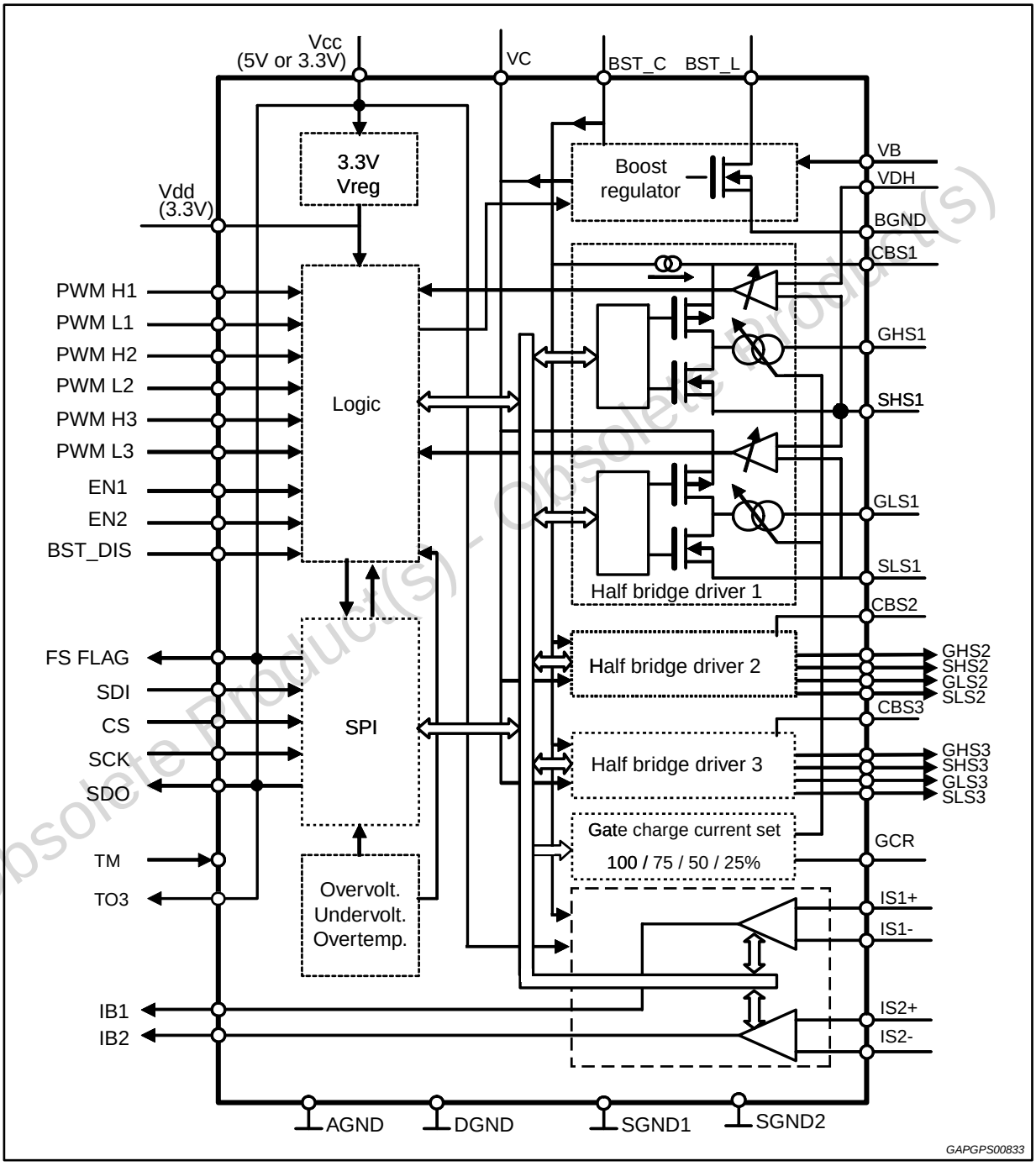
1 Description

L9907A is a smart power device realized in STMicroelectronics advanced BCD-6s technology. It is able to drive all PowerMOS transistors for 3-phase BLDC motor applications. The circuit is suitable to operate in environments with high supply voltage such as double battery. Supply related pins are capable of withstanding up to 75 V. Moreover, the device is able to control the six pre-driver channels independently. In this way it is possible to implement all kind of electric motor control strategies. The integrated boost regulator provides sufficient gate charge for all PowerMOS down to a battery voltage of 6 V. All pre-drivers have dedicated connections with the MOSFET sources. The device offers programmability for a base gate output current via an external resistor. Moreover, via SPI, it is possible to select among 4 gate output current levels even while the application is running. All channels are protected against short circuit and the device is protected against overtemperature condition. Moreover, the boost converter implements an over voltage protection to allow safe functionality of pre-drivers in all battery voltage condition. During over voltage condition, BST_C voltage is limited by temporarily switching off the boost regulator and pre-drivers are allowed to operate. Boost will be self reenabled as soon as the output voltage decreases to an acceptable value. The device is equipped with 2 current sense amplifiers. Both have SPI selectable amplifier gain (10, 30, 50 and 100) and output offset voltage level in order to allow max flexibility for phase or ground current sense strategy. All I/O pins are 35 V compatible. Full diagnostic is available through SPI. The device is available in TQFP64 and bare die, according to the application requirements. The device is protected against Shoot Through events.

2 Block diagram and pin description

2.1 Block diagram

Figure 1: Block diagram



2.2 Pin description

Figure 2: Pin connection diagram

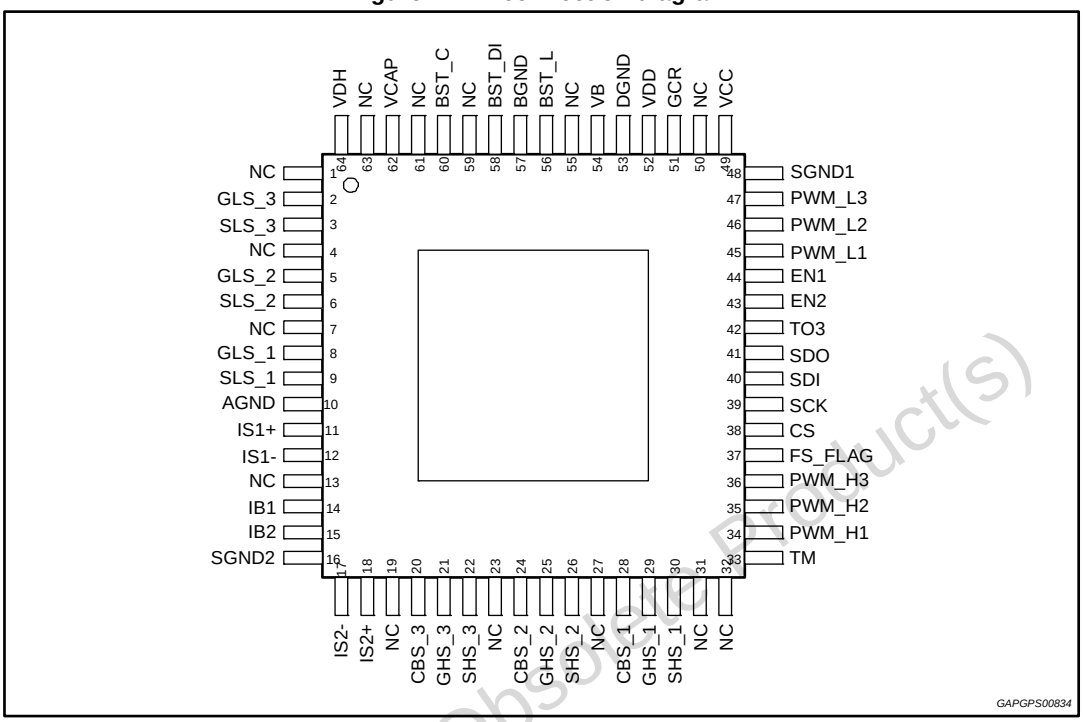


Table 2: Pin function

Pin #	Pin name	Description	I/O Type
1	NC	NC	-
2	GLS_3	Gate connection for low-side MOSFET, phase 3	O
3	SLS_3	Source connection for low-side MOSFET, phase 3	I
4	NC	NC	-
5	GLS_2	Gate connection for low-side MOSFET, phase 2	O
6	SLS_2	Source connection for low-side MOSFET, phase 2	I
7	NC	NC	-
8	GLS_1	Gate connection for low-side MOSFET, phase 1	O
9	SLS_1	Source connection for low-side MOSFET, phase 1	I
10	AGND	Analog ground	GND
11	IS1+	Positive input for current sense amplifier 1	I
12	IS1-	Negative input for current sense amplifier 1	I
13	NC	NC	-
14	IB1	Output for current sense amplifier 1 (Test mode digital output #1)	O
15	IB2	Output for current sense amplifier 2 (Test mode digital output #2)	O
16	SGND2	Substrate (and ESD_GND) connection 2	GND
17	IS2-	Negative input for current sense amplifier 2	I
18	IS2+	Positive input for current sense amplifier 2	i

Pin #	Pin name	Description	I/O Type
19	NC	NC	-
20	CBS_3	Bootstrap capacitor for high-side MOSFET, phase 3	I
21	GHS_3	Gate connection for high-side MOSFET, phase 3	O
22	SHS_3	Source connection for high-side MOSFET, phase 3	I
23	NC	NC	-
24	CBS_2	Bootstrap capacitor for high-side MOSFET, phase 2	I
25	GHS_2	Gate connection for high-side MOSFET, phase 2	O
26	SHS_2	Source connection for high-side MOSFET, phase 2	I
27	NC	NC	-
28	CBS_1	Bootstrap capacitor for high-side MOSFET, phase 1	I
29	GHS_1	Gate connection for high-side MOSFET, phase 1	O
30	SHS_1	Source connection for high-side MOSFET, phase 1	I
31	NC	NC	-
32	NC	NC	-
33	TM (1)	Test mode enable input	I
34	PWM_H1	PWM command input for high-side phase 1	I
35	PWM_H2	PWM command input for high-side phase 2	I
36	PWM_H3	PWM command input for high-side phase 3	I
37	FS_FLAG	Fault status flag output	O
38	CS	SPI chip select input	I
39	SCK	SPI serial clock input	I
40	SDI	SPI Serial data input	I
41	SDO	SPI serial data output	O
42	TO3	Test output	O
43	EN2	Enable Input 2 (ANDed with EN1 to enable any gate drive output).	I
44	EN1	Enable Input 1 (ANDed with EN2 to enable any gate drive output).	I
45	PWM_L1	PWM command input for low-side phase 1	I
46	PWM_L2	PWM command input for low-side phase 2	I
47	PWM_L3	PWM command input for low-side phase 3	I
48	SGND1	Substrate (and ESD_GND) connection 1	GND
49	Vcc	5 V / 3.3 V power supply input	I
50	NC	NC	-
51	GCR	Connection to resistor for current selection of gate driver	O
52	Vdd	3.3 V power supply output (for IC internal purpose only)	O
53	DGND	Digital ground	GND
54	VB	Protected battery monitor	I
55	NC	NC	-

Pin #	Pin name	Description	I/O Type
56	BST_L	Boost regulator inductance connection	O
57	BGND	Boost ground	GND
58	BST_DIS	Boost disable	I
59	NC	NC	-
60	BST_C	Boost regulator capacitance connection	I
61	NC	NC	-
62	VCAP	Decoupling capacitor for power supply of low-side drivers	I
63	NC	NC	-
64	VDH	High-side drain voltage sense	I

Notes:

(1)TM pin has to be connected to ground in the application.

3 Electrical specifications

3.1 Absolute maximum ratings

Maximum ratings are absolute ratings; exceeding any one of these values may cause permanent damage to the integrated circuit.

Table 3: Absolute maximum ratings

Parameter	Condition	Min	Max	Unit
Monitor supply pin	Pin VB	-0.3	75	V
		-10	10	mA
Power supply pins	BST_C	-0.3	75	V
		-100	100	mA
	Pin: BST_L	-0.3	75	V
		-2.5(1)	75	V
		-100	100	mA
	Pin V_{cc}	-0.3	35	V
		-10	25	mA
	Pin V_{dd}	-0.3	4.6	V
		-10	15	mA
	Pin VCAP	-0.3	20	V
		-100	100	mA
Miscellaneous Analog/Digital I/O pins	PWM_H1 to 3, PWM_L1 to 3, IB1, IB2, EN1, EN2, FS_FLAG, BST_DIS,TM, CS, SCK, SDI, SDO, TO3	-0.3	35(2)	V
		-10	10	mA
Gate current selection pin	Pin GCR	-0.3	4.6	V
		-10	10	mA
Current sense amplifier pins	IS1+,IS1-,IS2+,IS2-	-7	75	V
		-10	10	mA
Differential voltage between ISx +/-	Abs |ISx+ - ISx-|	-	15	V
High-side drain sense	Pin VDH	-4	75	V
		-10	10	mA
FET driver pins	HS Bootstrap Cap pins: CBS_1 to 3	-0.3	75	V
	Differential gate to source HS pins: V(GHS_x) - V(SHS_x), x = 1 to 3	-0.3	20	V
	Source HS pins: SHS_1 to 3	-7	75	V
	Source LS pins: SLS_1 to 3	-7	10	V
	Differential gate to source LS pins: V(GLS_x) - V(SLS_x), x = 1 to 3	-0.3	20	V

Parameter	Condition	Min	Max	Unit
Current sense amplifier differential voltage	BST_C-ISxx	-0.3	75	V
GND pins	Pins BGND and DGND	-0.3	4.6	V
	Pin AGND and EP	-0.3	0.3	V

Notes:

(1)-2.5 V for t < 1 µs.

(2)In standard battery level application (12 V systems) the I/O pins and Vcc pin can stand a short to battery up to 35 V. A short to 35 V battery on any I/O pin also forces the Vcc to approximately 35 V. Care must be taken in order to avoid that under such condition the Vcc pin is strongly pulled down to 5 V (or 3.3 V) with a current exceeding the absolute maximum ratings level.

3.2 ESD protection

Table 4: ESD protection

Parameter	Condition	Min	Max	Unit
Logic and power pins	Human body model (HBM)(1)	-2	2	kV
FET driver pins	Human body model	-2	2	kV
All pins but corner pins	Charge device model	-250	250	V
Corner pins	Charge device model	-750	750	V

Notes:

(1)HBM according to MIL 883C, Method 3015.7 or EIA/JESD22-A114_A. HBM with all unzapped pins grounded.

3.3 Temperature ranges and thermal data

Table 5: Temperature ranges and thermal data

Symbol	Parameter	Min	Max	Unit
T_j	Operating junction temperature	-40	150	°C
	100 hours over lifetime temperature(1)	-	175	°C
T_{stg}	Storage temperature	-55	150	°C
T_{ot}	Thermal shutdown temperature	175	205	°C
T_{hys}	Thermal shudown temperature hysteresis(2)	10	-	°C
$R_{th\ j\text{-}amb}$	Thermal resistance junction-to-ambient (3)	-	23	°C/W
$R_{th\ j\text{-}case}$	Thermal resistance junction-to-case	-	3	°C/W

Notes:

(1)Functionality is guaranteed, the specified limits may be exceeded.

(2)Guaranteed by design.

(3)IC soldered on 2s2p PCB thermally enhanced.

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

4.1 TQFP64 (10x10x1 mm exp. pad down) package information

Figure 3: TQFP64 (10x10x1 mm exp. pad down) package outline

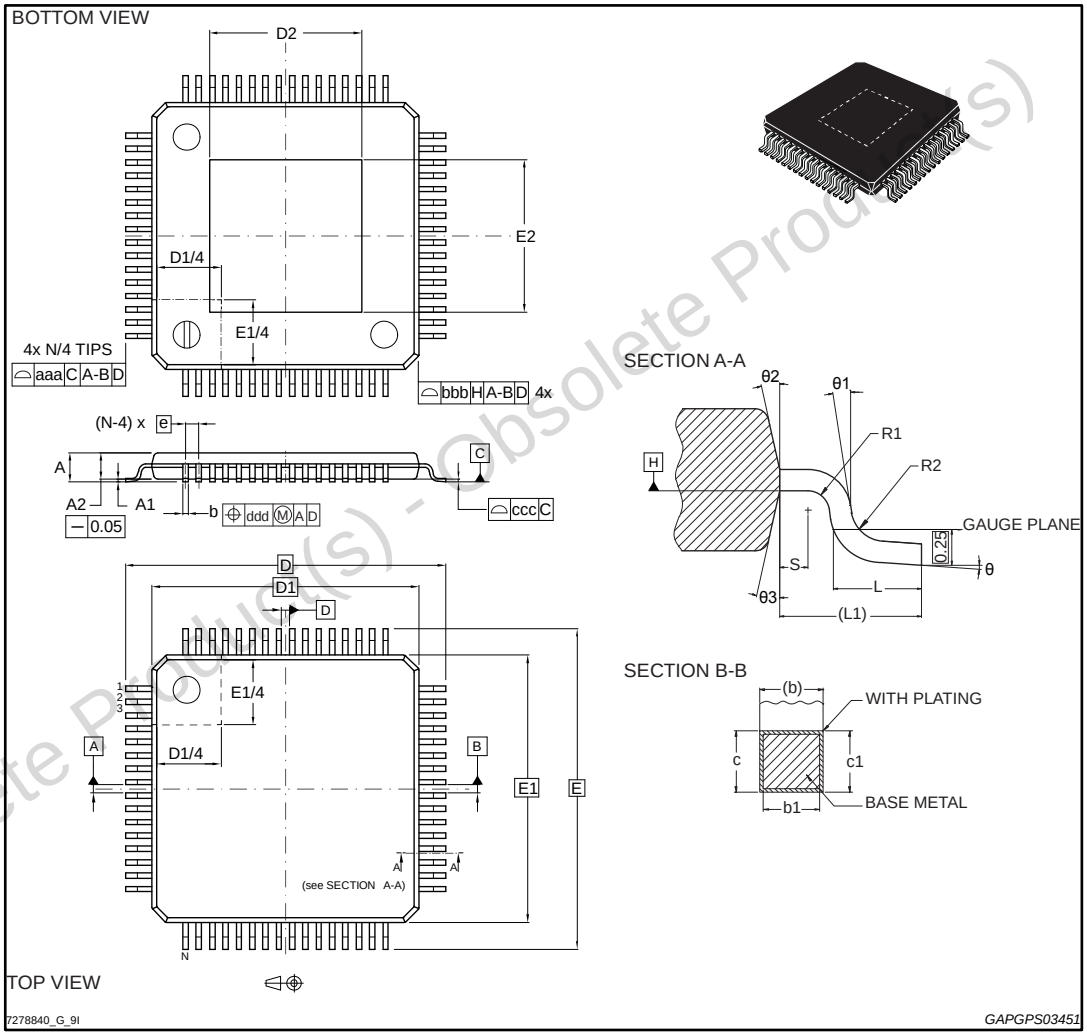


Table 6: TQFP64 (10x10x1 mm exp. pad down) mechanical data

Symbol	Milimeters			Inches[(1)]		
	Min	Typ	Max	Min	Typ	Max
θ	0°	3.5°	6°	0°	3.5°	6°
θ1	0°	-	-	0°	-	-
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°

Symbol	Milimeters			Inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.2	-	-	0.0472
A1	0.05	-	0.15	0.002	-	0.0059
A2	0.95	1	1.05	0.0374	0.0394	0.0413
b	0.17	0.22	0.27	0.0067	0.0079	0.0091
b1	0.17	0.2	0.23	0.0067	0.0079	0.0091
c	0.9	-	0.2	0.0354	-	0.0079
c1	0.9	-	0.16	0.0354	-	0.0063
D	-	12.00 BSC	-	-	0.4724 BSC	-
D1[2]	-	10.00 BSC	-	-	0.3937 BSC	-
D2	VARIATION					
e	-	0.50 BSC	-	-	0.0197 BSC	-
E	-	12.00 BSC	-	-	0.4724 BSC	-
E1[2]	-	10.00 BSC	-	-	0.3937 BSC	-
E2	VARIATION					
L	0.45	0.6	0.75	0.0177	0.0236	0.0295
L1	-	1.00 REF	-	-	0.0394 REF	-
N	-	64	-	-	2.5197	-
R1	0.08	-	-	0.0031	-	-
R2	0.08	-	0.2	0.0031	-	0.0079
S	0.2	-	-	0.0079	-	-
TOLERANCE OF FORM AND POSITION						
aaa	-	0.2	-	-	0.0079	-
bbb	-	0.2	-	-	0.0079	-
ccc	-	0.08	-	-	0.0031	-
ddd	-	0.07	-	-	0.0028	-
VARIATIONS						
Option A						
D2	-	4.5	-	-	0.1772	-
E2	-	4.5	-	-	0.1772	-
Option B						
D2	-	6	-	-	0.2362	-
E2	-	6	-	-	0.2362	-

Notes:

[1]Values in inches are converted from mm and rounded to 4 decimal digits.

[2]Dimensions D1 and E1 do not include mold flash or protrusions. Allowable mold flash or protrusion is “0.25 mm” per side.

5 Revision history

Table 7: Document revision history

Date	Revision	Changes
16-Feb-2015	1	Initial release.
23-Feb-2015	2	Updated supply voltage from 35 V to 36 V for working in 24 V system, in *Section "Features"*.

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