INTEGRATED CIRCUITS

DATA SHEET

TDA7056B

5 W mono BTL audio amplifier with DC volume control

Product specification
Supersedes data of 1996 May 28
File under Integrated Circuits, IC01

1997 Aug 15

Philips Semiconductors

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FEATURES

- DC volume control
- Few external components
- Mute mode
- Thermal protection
- Short-circuit proof
- No switch-on and switch-off clicks
- Good overall stability
- Low power consumption
- Low HF radiation
- ESD protected on all pins.

GENERAL DESCRIPTION

The TDA7056B is a mono Bridge-Tied Load (BTL) output amplifier with DC volume control.
It is designed for use in TV and monitors, but is also suitable for battery-fed portable recorders and radios.
The device is contained in a 9-pin medium power package.

A Missing Current Limiter (MCL) is built in. The MCL circuit is activated when the difference in current between the output terminal of each amplifier exceeds 100 mA (300 mA typ.). This level of 100 mA allows for headphone applications (single-ended).

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage		4.5	–	18	V
P_O	output power	V_P = 12 V				
		R_L = 16 Ω	3	3.5	–	W
		R_L = 8 Ω	5	5.5	–	W
$G_{v(max)}$	maximum total voltage gain		39.5	40.5	41.5	dB
ϕ	gain control		68	73.5	–	dB
$I_{q(tot)}$	total quiescent current	V_P = 12 V; R_L = ∞	–	9.2	13	mA
THD	total harmonic distortion	P_O = 0.5 W	–	0.3	1	%

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA7056B	SIL9MPF	plastic single in-line medium power package with fin; 9 leads	SOT110-1

BLOCK DIAGRAM

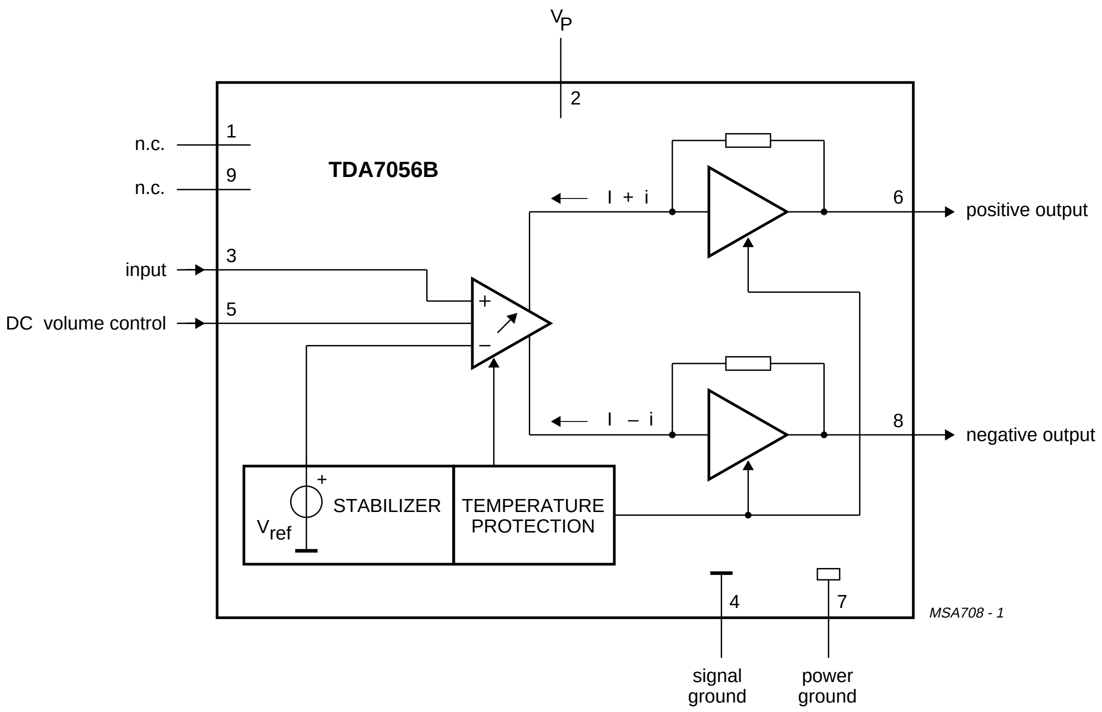


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
n.c.	1	not connected
V_P	2	positive supply voltage
V_I	3	voltage input
GND1	4	signal ground
VC	5	DC volume control
OUT+	6	positive output
GND2	7	power ground
OUT–	8	negative output
n.c.	9	not connected

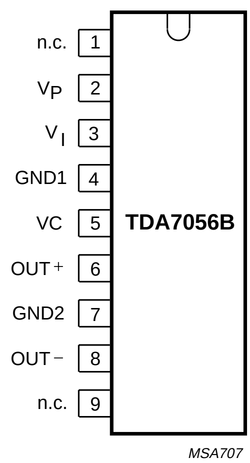


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TDA7056B is a mono BTL output amplifier with DC volume control, designed for use in TV and monitor but is also suitable for battery-fed portable recorders and radios.

In conventional DC volume circuits the control or input stage is AC coupled to the output stage via external capacitors to keep the offset voltage low. In the TDA7056B the DC volume control stage is integrated into the input stage so that no coupling capacitors are required. With this configuration, a low offset voltage is still maintained and the minimum supply voltage remains low.

The BTL principle offers the following advantages:

- Lower peak value of the supply current
- The frequency of the ripple on the supply voltage is twice the signal frequency.

Consequently, a reduced power supply with smaller capacitors can be used which results in cost reductions. For portable applications there is a trend to decrease the supply voltage, resulting in a reduction of output power at conventional output stages. Using the BTL principle increases the output power.

The maximum gain of the amplifier is fixed at 40.5 dB. The DC volume control stage has a logarithmic control characteristic. Therefore, the total gain can be controlled from 40.5 dB to –33 dB. If the DC volume control voltage falls below 0.4 V, the device will switch to the mute mode.

The amplifier is short-circuit proof to ground, V_P and across the load. Also a thermal protection circuit is implemented. If the crystal temperature rises above +150 °C the gain will be reduced, thereby reducing the output power. Special attention is given to switch-on and switch-off clicks, low HF radiation and a good overall stability.

Power dissipation

Assume V_P = 12 V; R_L = 16 Ω.
The maximum sine wave dissipation is = 1.8 W.

The $R_{th\ vj\text{-}a}$ of the package is 55 K/W.
Therefore $T_{amb\ (max)} = 150 - 55 \times 1.8 = 51$ °C.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	supply voltage		–	18	V
$V_{3,5}$	input voltage pins 3 and 5		–	5	V
I_{ORM}	repetitive peak output current		–	1.25	A
I_{OSM}	non-repetitive peak output current		–	1.5	A
P_{tot}	total power dissipation	T_{case} < 60 °C	–	9	W
T_{amb}	operating ambient temperature		–40	+85	°C
T_{stg}	storage temperature		–55	+150	°C
T_{vj}	virtual junction temperature		–	+150	°C
T_{sc}	short-circuit time		–	1	h

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	55	K/W
$R_{th\ j\text{-}c}$	thermal resistance from junction to case	10	K/W

CHARACTERISTICS

V_P = 12 V; V_{DC} = 1.4 V; f = 1 kHz; R_L = 16 Ω; T_{amb} = 25 °C; unless otherwise specified (see Fig.13).

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	positive supply voltage		4.5	–	18	V
$I_{q(tot)}$	total quiescent current	note 1; $R_L = \infty$	–	9.2	13	mA
Maximum gain (V_5 = 1.4 V)						
P_O	output power	THD = 10%; R_L = 16 Ω	3	3.5	–	W
		THD = 10%; R_L = 8 Ω	5	5.5	–	W
THD	total harmonic distortion	P_O = 0.5 W	–	0.3	1	%
$G_{v(max)}$	maximum total voltage gain		39.5	40.5	41.5	dB
V_I	input signal handling (RMS value)	$G_{v(max)}$ = 0 dB; THD < 1%	1.0	–	–	V
V_{no}	noise output voltage (RMS value)	note 2; f = 500 kHz	–	210	–	µV
B	bandwidth	at –1 dB	–	0.02 to 300	–	kHz
SVRR	supply voltage ripple rejection	note 3	34	38	–	dB
$\|\Delta V_O\|$	DC output offset voltage	$\|V_8 - v_6\|$	–	0	200	mV
Z_I	input impedance (pin 3)		15	20	25	kΩ
Mute position						
V_O	output voltage in mute position	note 4; $V_5 \leq 0.4$ V; V_I = 1.0 V	–	35	45	µV
DC volume control; note 5						
ϕ	gain control		68	73.5	–	dB
I_5	control current	V_5 = 0 V	–20	–25	–30	µA

Notes

1. With a load connected to the outputs the quiescent current will increase, the maximum value of this increase being equal to the DC output offset voltage divided by R_L.
2. The noise output voltage (RMS value) at f = 500 kHz is measured with R_S = 0 Ω and B = 5 kHz.
3. The ripple rejection is measured with R_S = 0 Ω and f = 100 Hz to 10 kHz. The ripple voltage V_R of 200 mV (RMS value) is applied to the positive supply rail.
4. The noise output voltage (RMS value) is measured with R_S = 5 kΩ unweighted.
5. The DC volume control can be configured in several ways. Two possible circuits are shown in Figs 14 and 15. The circuits at the volume control pin will influence the switch-on and switch-off behaviour and the maximum voltage gain.

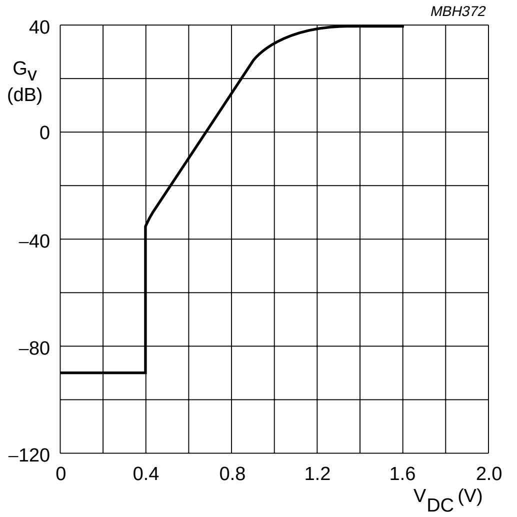
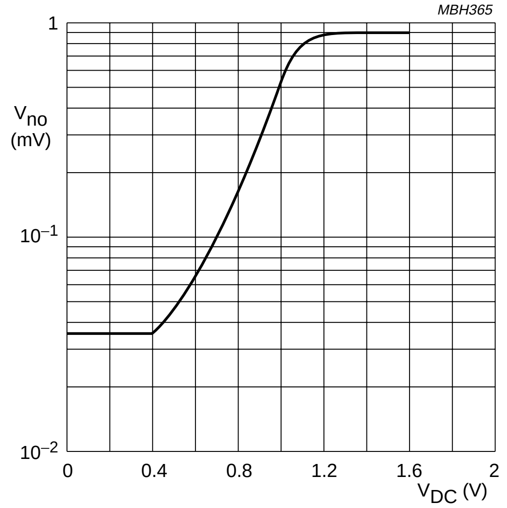


Fig.3 Gain control as a function of DC volume control.



Measured with R_S = 5 kΩ unweighted.
Frequency range is 22 Hz to 22 kHz.

Fig.4 Noise output voltage as a function of DC volume control.

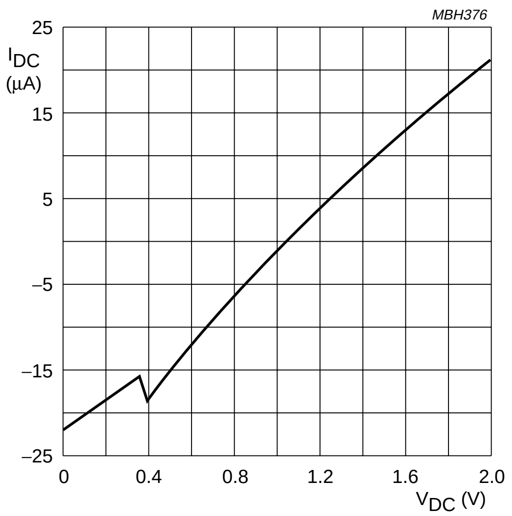
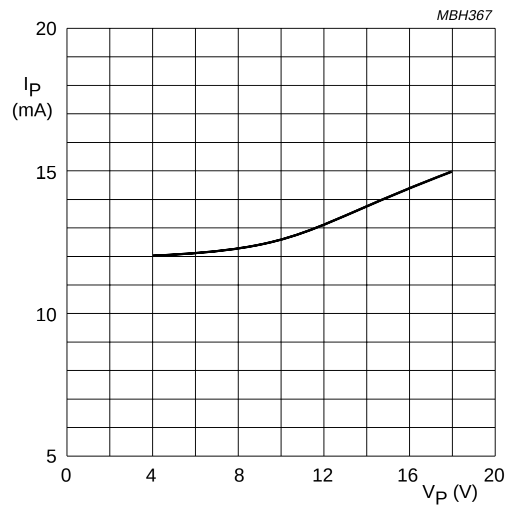
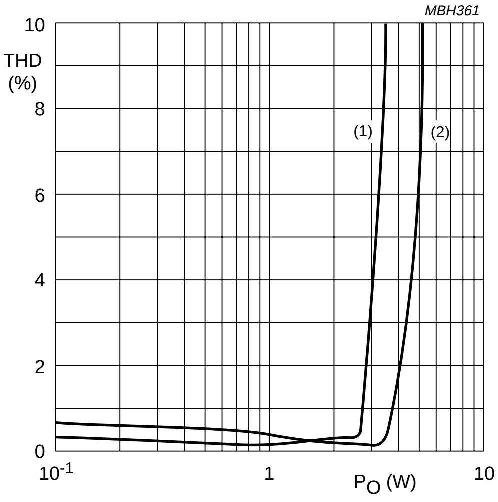


Fig.5 Control current as a function of DC volume control.



Measured with $R_L = \infty$.

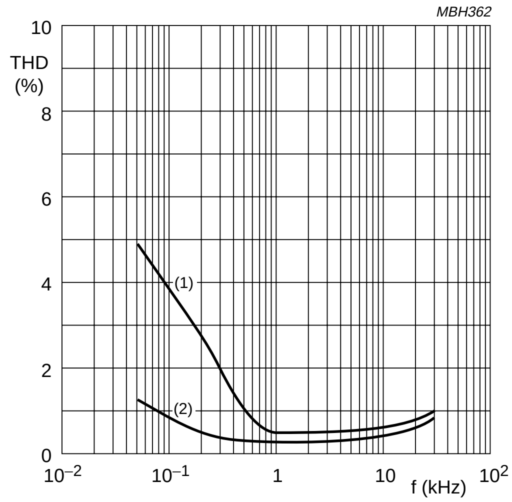
Fig.6 Quiescent current versus supply voltage.



(1) R_L 16 Ω.

(2) R_L = 8 Ω.

Fig.7 Total harmonic distortion versus output power.

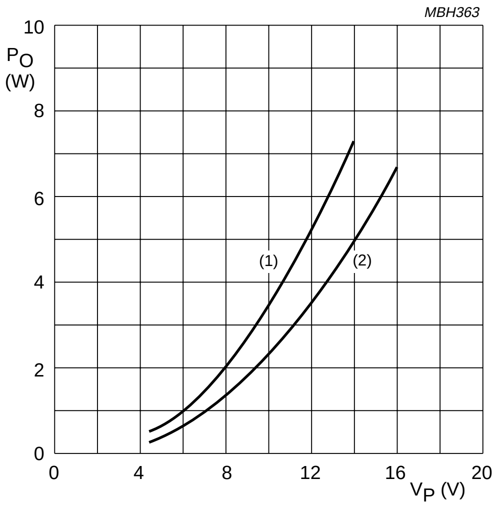


P_O = 0.1 W.

(1) $G_{v(max)}$ = 40 dB.

(2) $G_{v(max)}$ = 30 dB.

Fig.8 Total harmonic distortion versus frequency.

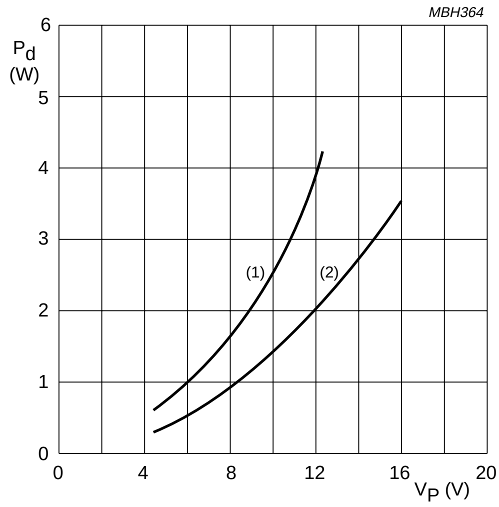


Measured at a THD of 10%. The maximum output power is limited by the maximum power dissipation and the maximum available output current.

(1) R_L = 8 Ω.

(2) R_L = 16 Ω.

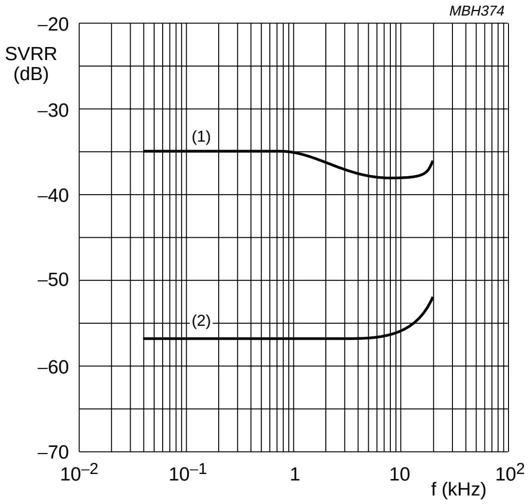
Fig.9 Output power versus supply voltage.



(1) R_L = 8 Ω.

(2) R_L = 16 Ω.

Fig.10 Total worst case power dissipation versus supply voltage.

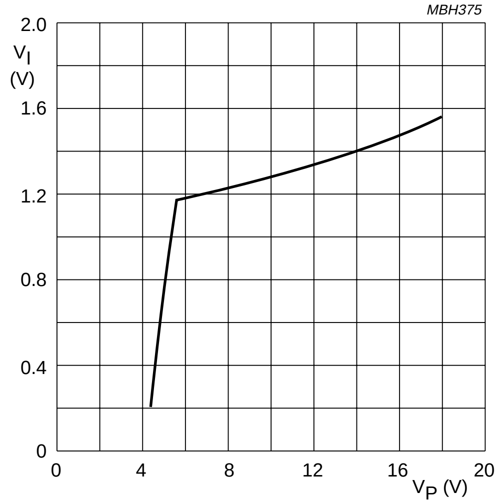


Measured with V_R = 0.2 V.

(1) V_{DC} = 1.4 V.

(2) V_{DC} = 0.4 V.

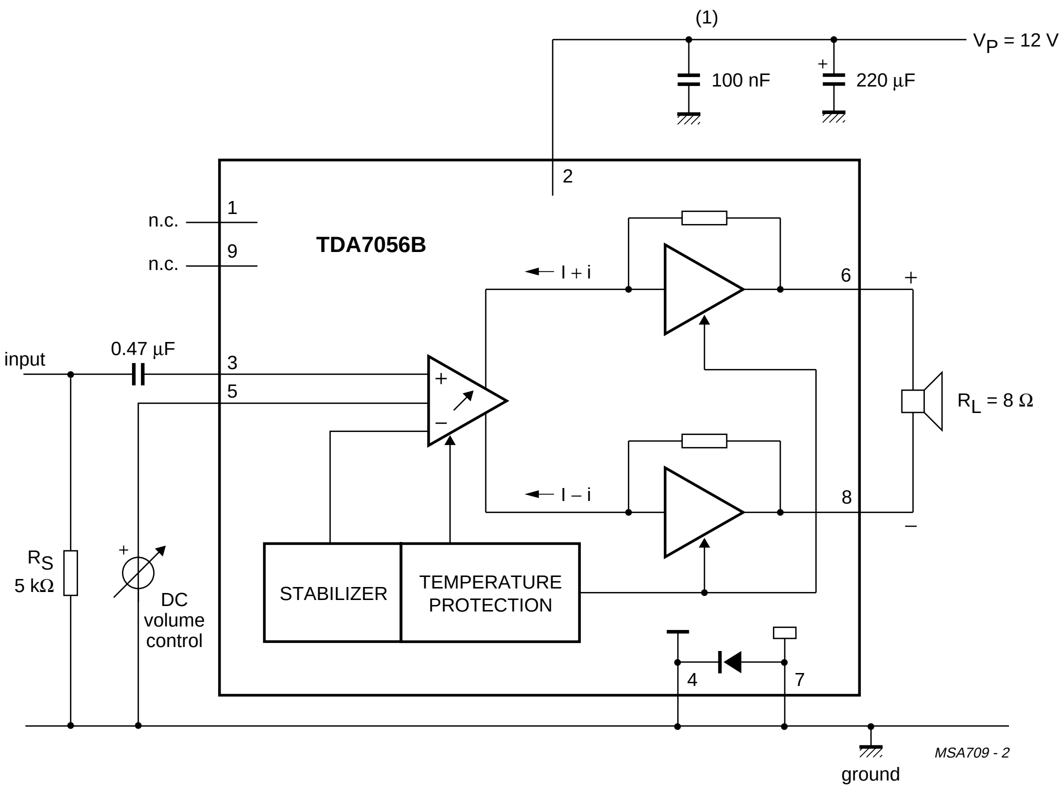
Fig.11 Supply voltage ripple rejection versus frequency.



Measured at a THD of 1% and a voltage gain of 0 dB.

Fig.12 Input signal handling.

TEST AND APPLICATION INFORMATION



To avoid instabilities and too high distortion, the input- and power ground must be separated as long as possible and connected together as close as possible to the IC.

(1) This capacitor can be omitted if the 220 µF electrolytic capacitor is connected close to pin 2.

Fig.13 Test and application diagram.

For single-end application the output peak current may not exceed 100 mA; at higher output currents the short circuit protection (MLC) will be activated.

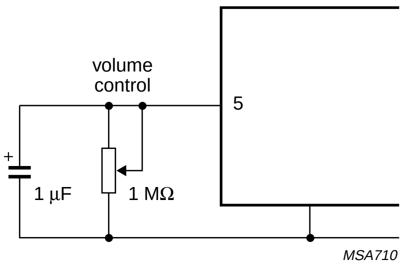


Fig.14 Application with potentiometer as volume control; maximum gain = 34 dB.

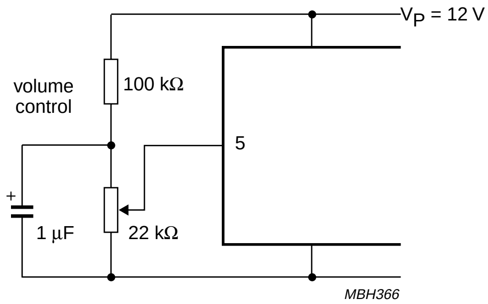
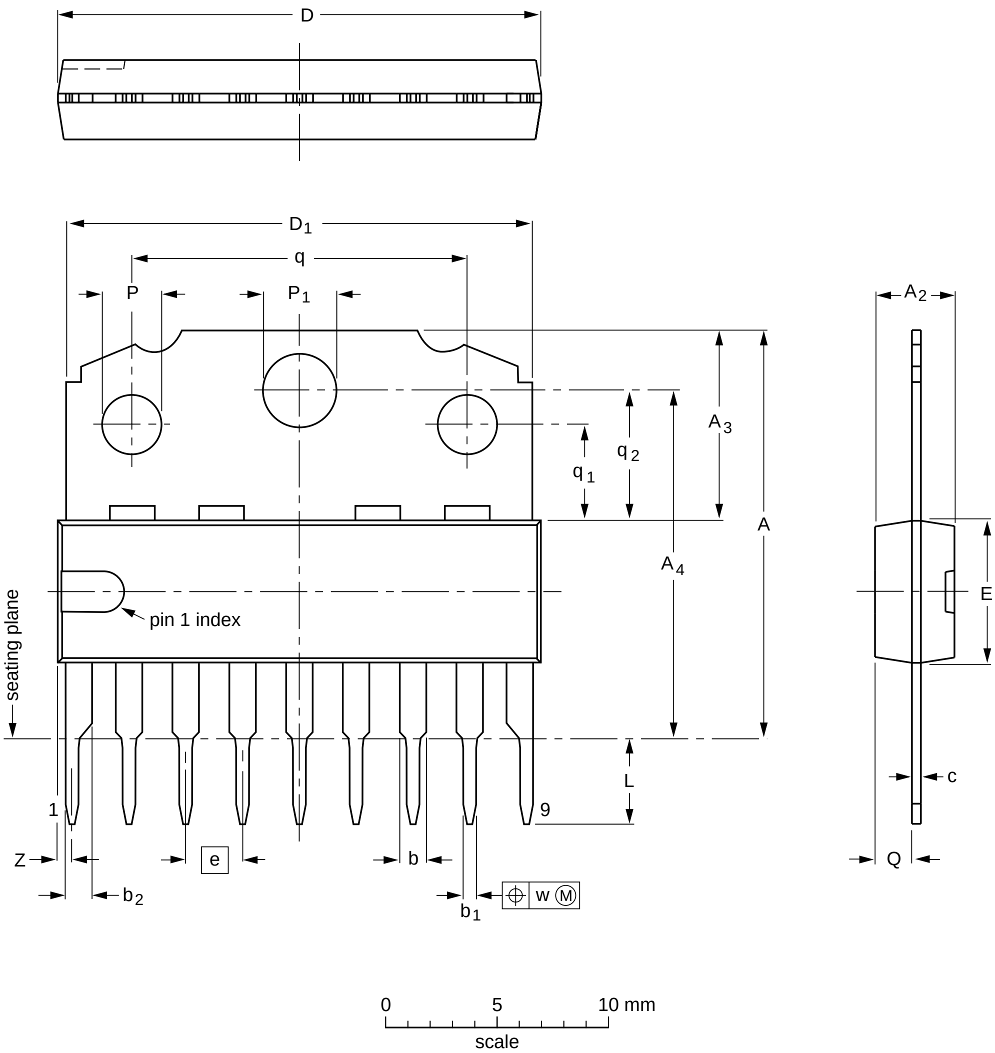


Fig.15 Application with potentiometer as volume control; maximum gain = 40 dB.

PACKAGE OUTLINE

SIL9MPF: plastic single in-line medium power package with fin; 9 leads **SOT110-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_2 max.	A_3	A_4	b	b_1	b_2	c	D(1)	D_1	E(1)	e	L	P	P_1	Q	q	q_1	q_2	w	Z(1) max.
mm	18.5 17.8	3.7	8.7 8.0	15.8 15.4	1.40 1.14	0.67 0.50	1.40 1.14	0.48 0.38	21.8 21.4	21.4 20.7	6.48 6.20	2.54	3.9 3.4	2.75 2.50	3.4 3.2	1.75 1.55	15.1 14.9	4.4 4.2	5.9 5.7	0.25	1.0

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT110-1						~~92-11-17~~ 95-02-25

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Soldering by dipping or by wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

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