ON Semiconductor®

FAN5236
Dual Mobile-Friendly DDR / Dual-Output PWM Controller

Features

- Highly Flexible, Dual Synchronous Switching PWM Controller that Includes Modes for:
  - DDR Mode with In-phase Operation for Reduced Channel Interference
  - 90° Phase-shifted, Two-stage DDR Mode for Reduced Input Ripple
  - Dual Independent Regulators, 180° Phase Shifted
- Complete DDR Memory Power Solution
  - V_{TT} Tracks $V_{DDQ/2}$
  - $V_{DDQ/2}$ Buffered Reference Output
- Lossless Current Sensing on Low-side MOSFET or Precision Over-Current Using Sense Resistor
- V_{CC} Under-Voltage Lockout
- Converters can Operate from +5V or 3.3V or Battery Power Input (5V to 24V)
- Excellent Dynamic Response with Voltage Feedforward and Average-Current-Mode Control
- Power-Good Signal
- Supports DDR-II and HSTL
- Light-Load Hysteretic Mode Maximizes Efficiency
- TSSOP28 Package

Applications

- DDR V_{DDQ} and V_{TT} Voltage Generation
- Mobile PC Dual Regulator
- Server DDR Power i
- Hand-held PC Power

Related Resources

- http://www.onsemi.com/pub/Collateral/AN-6002.pdf.pdf
- http://www.onsemi.com/pub/Collateral/AN-1029.pdf.pdf

Description

The FAN5236 PWM controller provides high efficiency and regulation for two output voltages adjustable in the range of 0.9V to 5.5V required to power I/O, chip-sets, and memory banks in high-performance notebook computers, PDAs, and Internet appliances. Synchronous rectification and hysteretic operation at light loads contribute to high efficiency over a wide range of loads. The Hysteretic Mode can be disabled separately on each PWM converter if PWM Mode is desired for all load levels. Efficiency is enhanced by using MOSFET $R_{DS(ON)}$ as a current-sense component.

Feedforward ramp modulation, average-current-mode control scheme, and internal feedback compensation provide fast response to load transients. Out-of-phase operation with 180-degree phase shift reduces input current ripple. The controller can be transformed into a complete DDR memory power supply solution by activating a designated pin. In DDR mode, one of the channels tracks the output voltage of another channel and provides output current sink and source capability — essential for proper powering of DDR chips. The buffered reference voltage required by this type of memory is also provided. The FAN5236 monitors these outputs and generates separate PGx (power good) signals when the soft-start is completed and the output is within ±10% of the set point. Built-in over-voltage protection prevents the output voltage from going above 120% of the set point. Normal operation is automatically restored when the over-voltage conditions cease. Under-voltage protection latches the chip off when output drops below 75% of the set value after the soft-start sequence for this output is completed. An adjustable over-current function monitors the output current by sensing the voltage drop across the lower MOSFET. If precision current-sensing is required, an external current-sense resistor may be used.

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Publication Order Number:
FAN5236/D

Ordering Information

Part Number	B Operating Temperature Range	Package	Packing Method
FAN5236MTCX	-10 to +85°C	28-Lead Thin-Shrink Small-Outline Package (TSSOP)	Tape and Reel

Block Diagrams

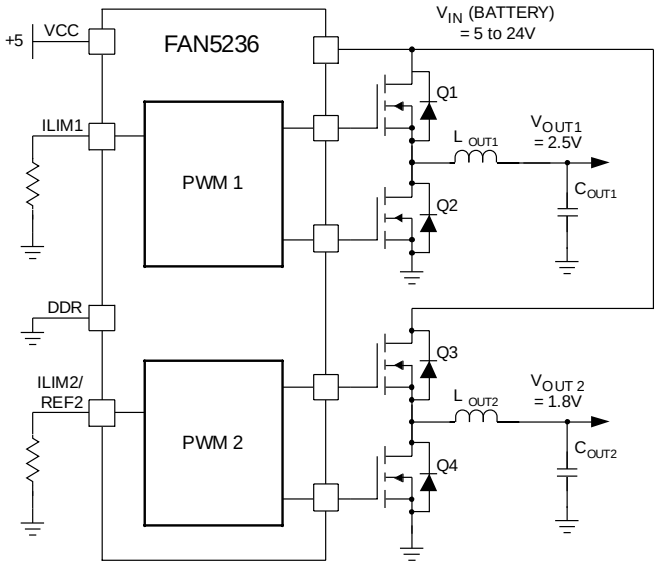


Figure 1. Dual-Output Regulator

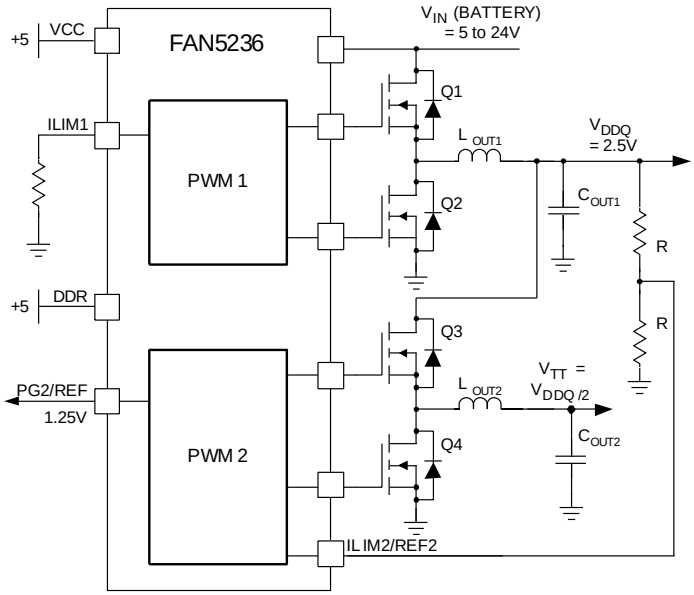


Figure 2. Complete DDR Memory Power Supply

Pin Configuration

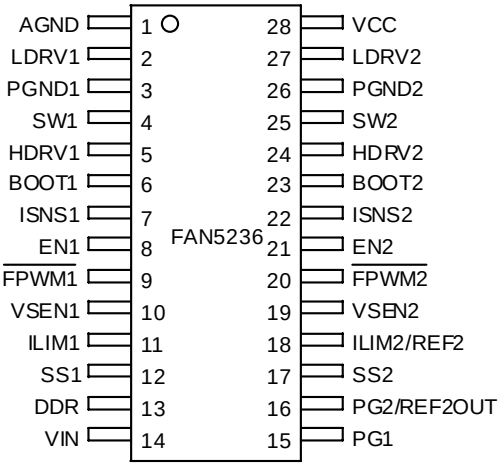


Figure 3. Pin Configuration

Pin Definitions

Pin #	Name	Description
1	AGND	**Analog Ground**. This is the signal ground reference for the IC. All voltage levels are measured with respect to this pin.
2	LDRV1	**Low-Side Drive**. The low-side (lower) MOSFET driver output. Connect to gate of low-side MOSFET.
27	LDRV2	
3	PGND1	**Power Ground**. The return for the low-side MOSFET driver. Connect to source of low-side MOSFET.
26	PGND2	
4	SW1	**Switching Node**. Return for the high-side MOSFET driver and a current sense input. Connect to source of high-side MOSFET and low-side MOSFET drain.
25	SW2	
5	HDRV1	**High-Side Drive**. High-side (upper) MOSFET driver output. Connect to gate of high-side MOSFET.
24	HDRV2	
6	BOOT1	**BOOT**. Positive supply for the upper MOSFET driver. Connect as shown in Figure 4.
23	BOOT2	
7	ISNS1	**Current-Sense Input**. Monitors the voltage drop across the lower MOSFET or external sense resistor for current feedback.
22	ISNS2	
8	EN1	**Enable**. Enables operation when pulled to logic HIGH. Toggling EN resets the regulator after a latched fault condition. These are CMOS inputs whose state is indeterminate if left open.
21	EN2	
9	FPWM1	**Forced PWM Mode**. When logic LOW, inhibits the regulator from entering Hysteretic Mode; otherwise tie to V_{OUT}. The regulator uses V_{OUT} on this pin to ensure a smooth transition from Hysteretic Mode to PWM Mode. When V_{OUT} is expected to exceed V_{CC}, tie to V_{CC}.
20	FPWM2	
10	VSEN1	**Output Voltage Sense**. The feedback from the outputs. Used for regulation as well as PG, under-voltage, and over-voltage protection and monitoring.
19	VSEN2	
11	ILIM1	**Current Limit 1**. A resistor from this pin to GND sets the current limit.
12	SS1	**Soft Start**. A capacitor from this pin to GND programs the slew rate of the converter during initialization. During initialization, this pin is charged with a 5mA current source.
17	SS2	

Pin Descriptions (Continued)

Pin #	Name	Description
13	DDR	**DDR Mode Control**. HIGH = DDR Mode. LOW = two separate regulators operating 180° out of phase.
14	VIN	**Input Voltage**. Normally connected to battery, providing voltage feedforward to set the amplitude of the internal oscillator ramp. When using the IC for two-step conversion from 5V input, connect through 100KΩ resistor to ground, which sets the appropriate ramp gain and synchronizes the channels 90° out of phase.
15	PG1	**Power Good Flag**. An open-drain output that pulls LOW when V_{SEN} is outside a ±10% range of the 0.9V reference.
16	PG2 / REF2OUT	**Power Good 2**. When not in DDR Mode, open-drain output that pulls LOW when the V_{OUT} is out of regulation or in a fault condition. **Reference Out 2**. When in DDR Mode, provides a buffered output of REF2. Typically used as the $V_{DDQ/2}$ reference.
18	ILIM2 / REF2	**Current Limit 2**. When not in DDR Mode, a resistor from this pin to GND sets the current limit. **Reference** for reg #2 when in DDR Mode. Typically set to $V_{OUT1/2}$.
28	VCC	**VCC**. This pin powers the chip as well as the LDRV buffers. The IC starts to operate when voltage on this pin exceeds 4.6V (UVLO rising) and shuts down when it drops below 4.3V (UVLO falling).

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	V_{CC} Supply Voltage		6.5	V
V_{IN}	V_{IN} Supply Voltage		27	V
	BOOT, SW, ISNS, HDRV		33	V
	BOOTx to SWx		6.5	V
	All Other Pins	-0.3	V_{CC}+0.3	V
T_J	Junction Temperature	-40	+150	°C
T_{STG}	Storage Temperature	-65	+150	°C
T_L	Lead Temperature (Soldering,10 Seconds)		+300	°C

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. ON Semiconductor does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	V_{CC} Supply Voltage	4.75	5.00	5.25	V
V_{IN}	V_{IN} Supply Voltage			24	V
T_A	Ambient Temperature	-10		+85	°C
Θ_{JA}	Thermal Resistance, Junction to Ambient			90	°C/W

Electrical Characteristics

Recommended operating conditions, unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Power Supplies						
I_{VCC}	V_{CC} Current	LDRV, HDRV Open, V_{SEN} Forced Above Regulation Point		2.2	3.0	µA
		Shutdown (EN-0)			30	µA
I_{SINK}	V_{IN} Current, Sinking	V_{IN} = 24V	10		30	µA
I_{SOURCE}	V_{IN} Current, Sourcing	V_{IN} = 0V		-15	-30	µA
I_{SD}	V_{IN} Current, Shutdown				1	µA
V_{UVLO}	UVLO Threshold	Rising V_{CC}	4.30	4.55	4.75	V
		Falling	4.10	4.25	4.45	V
V_{UVLOH}	UVLO Hysteresis			300		mV
Oscillator						
f_{osc}	Frequency		255	300	345	KHz
V_{PP}	Ramp Amplitude	V_{IN} = 16V		2		V
		V_{IN} = 5V		1.25		V
V_{RAMP}	Ramp Offset			0.5		V
G	Ramp / V_{IN} Gain	$V_{IN} \leq 3V$		125		mV/V
		$1V < V_{IN} < 3V$		250		mV/V
Reference and Soft Start						
V_{REF}	Internal Reference Voltage		0.891	0.900	0.909	V
I_{SS}	Soft-Start Current	At Startup		5		µA
V_{SS}	Soft-Start Complete Threshold			1.5		V
PWM Converters						
	Load Regulators	I_{OUTX} from 0 to 5A, V_{IN} from 5 to 24V	-2		+2	%
I_{SEN}	V_{SEN} Bias Current		50	80	120	nA
	VOUT Pin Input Impedance		45	55	65	KΩ
$UVLO_{TSD}$	Under-Voltage Shutdown	% of Set Point, 2µs Noise Filter	70	75	80	%
UVLO	Over-Voltage Threshold	% of Set Point, 2µs Noise Filter	115	120	125	%
I_{SNS}	Over-Current Threshold	R_{ILIM}= 68.5KΩ, Figure 12	112	140	168	µA
Output Drivers						
	HDRV Output Resistance	Sourcing		12.0	15.0	Ω
		Sinking		2.4	4.0	
	LDRV Output Resistance	Sourcing		12.0	15.0	Ω
		Sinking		1.2	2.0	

Continued on following page…

Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Power-Good Output and Control Pins						
	Lower Threshold	% of Set Point, 2µs Noise Filter	-86		-94	%
	Upper Threshold	% of Set Point, 2µs Noise Filter	108		116	%
	PG Output Low	IPG = 4mA			0.5	V
	Leakage Current	V_{PULLUP} = 5V			1	µA
	PG2/REF2OUT Voltage	DDR = 1, 0mA < $I_{REF2OUT}$ ≤10mA	99.00		1.01	% V_{REF2}
DDR, EN Inputs						
V_{INH}	Input High		2			V
V_{INL}	Input Low				0.8	V
FPWM Inputs						
	FPWM Low				0.1	V
	FPWM High	FPWM Connected to Output	0.9			V

Block Diagram

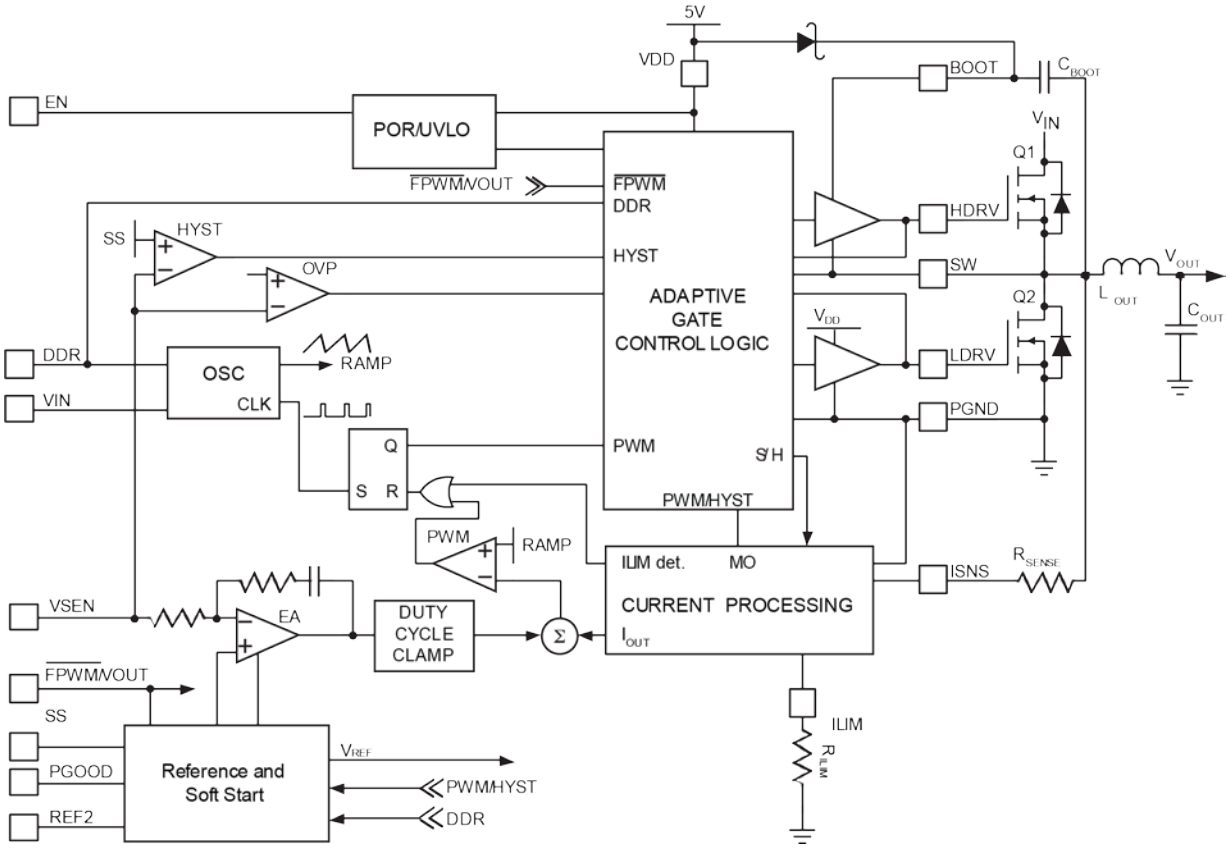


Figure 4. IC Block Diagram

Typical Application

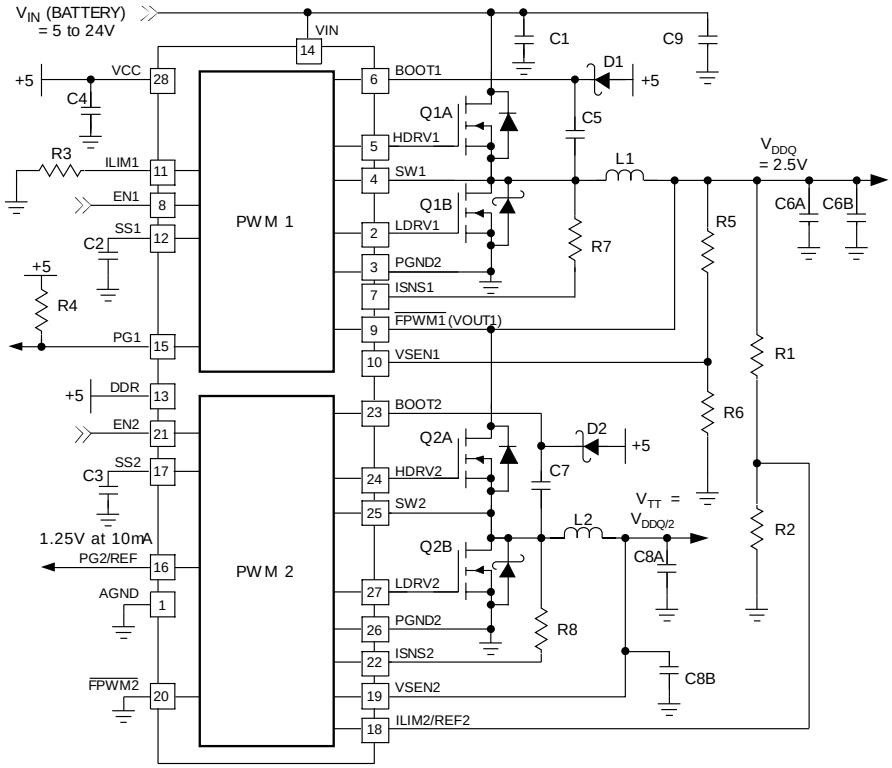


Figure 5. DDR Regulator Application

Table 1. DDR Regulator BOM

Description	Qty.	Ref.	Vendor	Part Number
Capacitor 68µf, Tantalum, 25V, ESR 150mΩ	1	C1	AVX	TPSV686*025#0150
Capacitor 10nf, Ceramic	2	C2, C3	Any	
Capacitor 68µf, Tantalum, 6V, ESR 1.8Ω	1	C4	AVX	TAJB686*006
Capacitor 150nF, Ceramic	2	C5, C7	Any	
Capacitor 180µf, Specialty Polymer 4V, ESR 15mΩ	2	C6A, C6B	Panasonic	EEFUE0G181R
Capacitor 1000µf, Specialty Polymer 4V, ESR 10mΩ	1	C8	Kemet	T510E108(1)004AS4115
Capacitor 0.1µF, Ceramic	2	C9	Any	
18.2KΩ, 1% Resistor	3	R1, R2	Any	
1.82KΩ, 1% Resistor	1	R6	Any	
56.2KΩ, 1% Resistor	2	R3	Any	
10KΩ, 5% Resistor	2	R4	Any	
3.24KΩ, 1% Resistor	1	R5	Any	
1.5KΩ, 1% Resistor	2	R7, R8	Any	
Schottky Diode 30V	2	D1, D2	ON Semiconductor	BAT54
Inductor 6.4µH, 6A, 8.64mΩ	1	L1	Panasonic	ETQ-P6F6R4HFA
Inductor 0.8µH, 6A, 2.24mΩ	1	L2	Panasonic	ETQ-P6F0R8LFA
Dual MOSFET with Schottky	1	Q1, Q2	ON Semiconductor	FDS6986AS(1)
DDR Controller	1	U1	ON Semiconductor	FAN5236

Note:

1. Suitable for typical notebook computer application of 4A continuous, 6A peak for V_{DDQ}. If continuous operation above 6A is required, use single SO-8 packages. *For more information, refer to the Power MOSFET Selection Section and use AN-6002 for design calculations.*

Typical Applications (Continued)

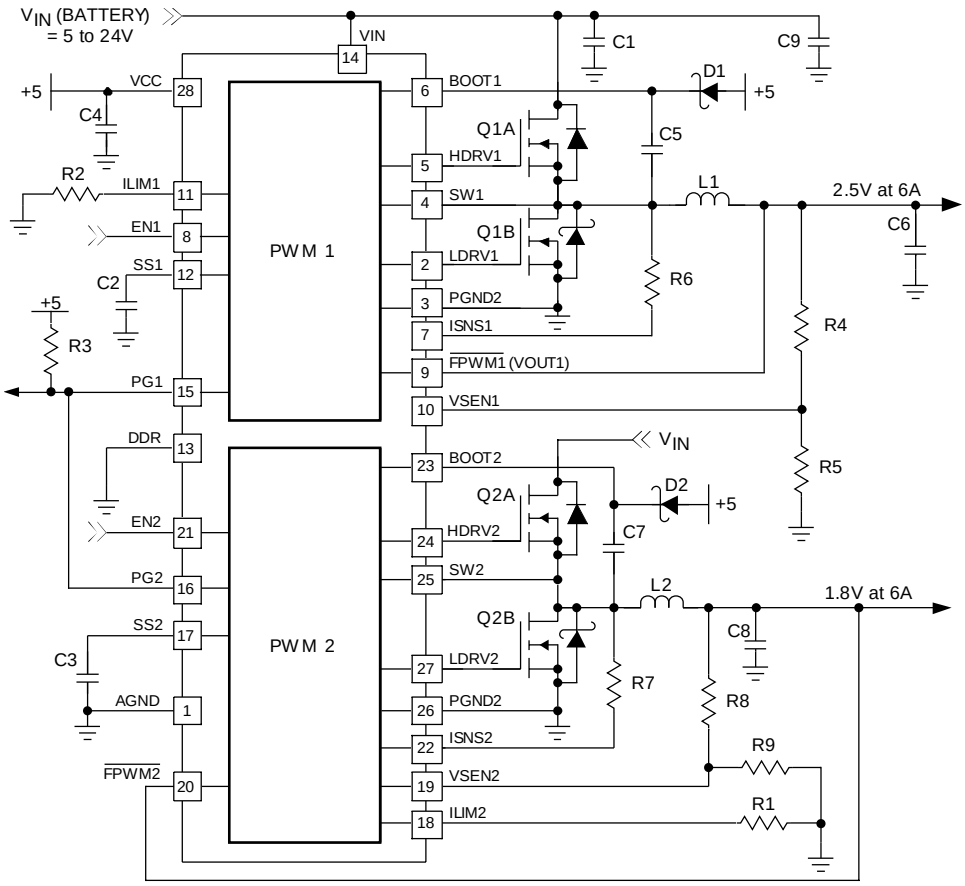


Figure 6. Dual Regulator Application

Table 2. DDR Regulator BOM

Item	Description	Qty.	Ref.	Vendor	Part Number
1	Capacitor 68µf, Tantalum, 25V, ESR 95mΩ	1	C1	AVX	TPSV686*025#095
2	Capacitor 10nf, Ceramic	2	C2, C3	Any	
3	Capacitor 68µf, Tantalum, 6V, ESR 1.8Ω	1	C4	AVX	TAJB686*006
4	Capacitor 150nF, Ceramic	2	C5, C7	Any	
5	Capacitor 330µf, Poscap, 4V, ESR 40mΩ	2	C6, C8	Sanyo	4TPB330ML
5	Capacitor 0.1µF, Ceramic	2	C9	Any	
11	56.2KΩ, 1% Resistor	2	R1, R2	Any	
12	10KΩ, 5% Resistor	2	R3	Any	
13	3.24KΩ, 1% Resistor	1	R4	Any	
14	1.82KΩ, 1% Resistor	3	R5, R8, R9	Any	
15	1.5KΩ, 1% Resistor	2	R6, R7	Any	
27	Schottky Diode 30V	2	D1, D2	ON Semiconductor	BAT54
28	Inductor 6.4µH, 6A, 8.64mΩ	1	L1, L2	Panasonic	ETQ-P6F6R4HFA
29	Dual MOSFET with Schottky	1	Q1	ON Semiconductor	FDS6986AS(2)
30	DDR Controller	1	U1	ON Semiconductor	FAN5236

Note:

2. If currents above 4A continuous are required, use single SO-8 packages. *For more information, refer to the Power MOSFET Selection Section and AN-6002 for design calculations.*

Circuit Description

Overview

The FAN5236 is a multi-mode, dual-channel PWM controller intended for graphic chipset, SDRAM, DDR DRAM, or other low-voltage power applications in modern notebook, desktop, and sub-notebook PCs. The IC integrates control circuitry for two synchronous buck converters. The output voltage of each controller can be set in the range of 0.9V to 5.5V by an external resistor divider.

The two synchronous buck converters can operate from either an unregulated DC source (such as a notebook battery), with voltage ranging from 5.0V to 24V, or from a regulated system rail of 3.3V to 5.0V. In either mode, the IC is biased from a +5V source. The PWM modulators use an average-current-mode control with input voltage feedforward for simplified feedback loop compensation and improved line regulation. Both PWM controllers have integrated feedback loop compensation that reduces the external components needed.

Depending on the load level, the converters can operate in fixed-frequency PWM Mode or in a Hysteretic Mode. Switch-over from PWM to Hysteretic Mode improves the converters' efficiency at light loads and prolongs battery run time. In Hysteretic Mode, comparators are synchronized to the main clock, which allows seamless transition between the modes and reduces channel-to-channel interaction. The Hysteretic Mode can be inhibited independently for each channel if variable frequency operation is not desired.

The FAN5236 can be configured to operate as a complete DDR solution. When the DDR pin is set HIGH, the second channel provides the capability to track the output voltage of the first channel. The PWM2 converter is prevented from going into Hysteretic Mode if the DDR pin is set HIGH. In DDR Mode, a buffered reference voltage (buffered voltage of the REF2 pin), required by DDR memory chips, is provided by the PG2 pin.

Converter Modes and Synchronization

Table 3. Converter Modes and Synchronization

Mode	V_{IN}	VIN Pin	DDR Pin	PWM 2 w.r.t. PWM1
DDR1	Battery	V_{IN}	HIGH	IN PHASE
DDR2	+5V	R to GND	HIGH	+90°
DUAL	ANY	V_{IN}	LOW	+180°

When used as a dual converter, as shown in Figure 6, out-of-phase operation with 180-degree phase shift reduces input current ripple.

For "two-step" conversion (where the V_{TT} is converted from V_{DDQ} as in Figure 5) used in DDR Mode, the duty cycle of the second converter is nominally 50% and the optimal phasing depends on V_{IN}. The objective is to keep noise generated from the switching transition in one converter from influencing the "decision" to switch in the other converter.

When V_{IN} is from the battery, it's typically higher than 7.5V. As shown in Figure 7, 180° operation is undesirable because the turn-on of the V_{DDQ} converter occurs very near the decision point of the V_{TT} converter.

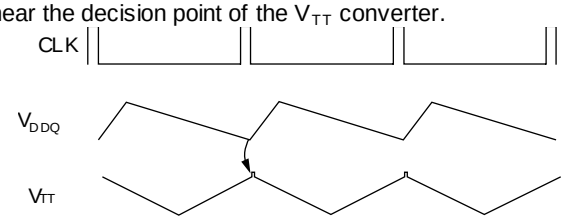
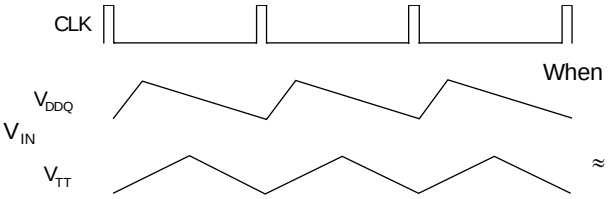


Figure 7. Noise-Susceptible 180° Phasing for DDR1

In-phase operation is optimal to reduce inter-converter interference when V_{IN} is higher than 5V (when V_{IN} is from a battery), as shown in Figure 8. Because the duty cycle of PWM1 (generating V_{DDQ}) is short, the switching point occurs far away from the decision point for the V_{TT} regulator, whose duty cycle is nominally 50%.

Figure 8. Optimal In-Phase Operation for DDR1



When $V_{IN} \approx$ 5V, 180° phase-shifted operation can be rejected for the reasons demonstrated in Figure 7.

In-phase operation with $V_{IN} \approx 5V$ is even worse, since the switch point of either converter occurs near the switch point of the other converter, as seen in Figure 9. In this case, as V_{IN} is a little higher than 5V, it tends to cause early termination of the V_{TT} pulse width. Conversely, the V_{TT} switch point can cause early termination of the V_{DDQ} pulse width when V_{IN} is slightly lower than 5V.

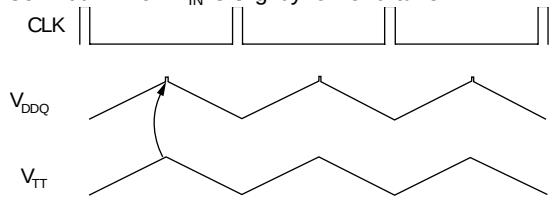


Figure 9. Noise-Susceptible In-Phase Operation for DDR2

These problems are solved by delaying the second converter's clock by 90°, as shown in Figure 10. In this way, all switching transitions in one converter take place far away from the decision points of the other converter.

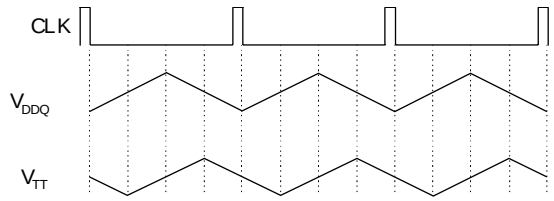


Figure 10. Optimal 90° Phasing for DDR

Initialization and Soft Start

Assuming EN is HIGH, FAN5236 is initialized when V_{CC} exceeds the rising UVLO threshold. Should V_{CC} drop below the UVLO threshold, an internal power-on reset function disables the chip.

The voltage at the positive input of the error amplifier is limited by the voltage at the SS pin, which is charged with a 5μA current source. Once C_{SS} has charged to V_{REF} (0.9V) the output voltage is in regulation. The time it takes SS to reach 0.9V is:

$$t_{0.9} = \frac{0.9xC_{SS}}{5} \quad (1)$$

where $t_{0.9}$ is in seconds if C_{SS} is in μF.

When SS reaches 1.5V, the power-good outputs are enabled and Hysteretic Mode is allowed. The converter is forced into PWM Mode during soft-start.

Operation Mode Control

The mode-control circuit changes the converter mode from PWM to hysteretic and vice versa, based on the voltage polarity of the SW node when the lower MOSFET is conducting and just before the upper MOSFET turns on. For continuous inductor current, the SW node is negative when the lower MOSFET is conducting and the converters operate in fixed-frequency PWM Mode, as shown in Figure 11. This mode achieves high efficiency at nominal load. When the load current decreases to the point where the inductor current flows through the lower MOSFET in the 'reverse' direction, the SW node becomes positive and the mode is changed to hysteretic, which achieves higher efficiency at low currents by decreasing the effective switching frequency.

To prevent accidental mode change or "mode chatter," the transition from PWM to Hysteretic Mode occurs when the SW node is positive for eight consecutive clock cycles, as shown in Figure 11. The polarity of the SW node is sampled at the end of the lower MOSFET conduction time. At the transition between PWM and Hysteretic Mode, the upper and lower MOSFETs are turned off. The phase node "rings" based on the output inductor and the parasitic capacitance on the phase node and settles out at the value of the output voltage.

The boundary value of inductor current, where current becomes discontinuous, can be estimated by the following expression:

$$I_{LOAD(DIS)} = \left(\frac{(V_{IN} - V_{OUT})V_{OUT}}{2F_{SW}L_{OUT}V_{IN}} \right) \quad (2)$$

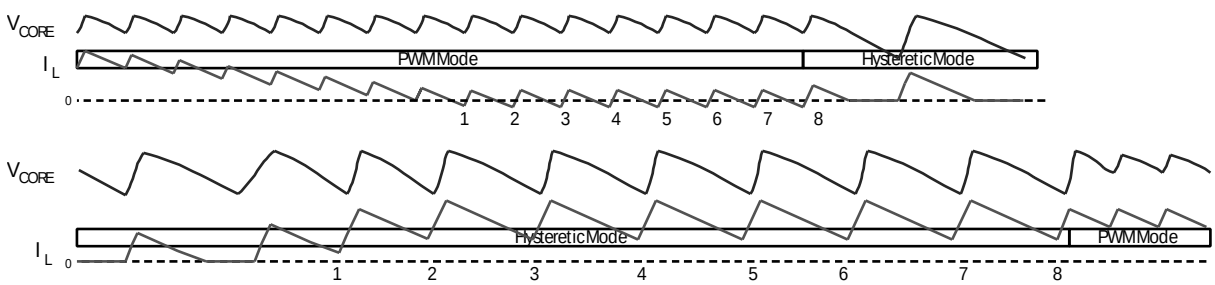


Figure 11. Transitioning Between PWM and Hysteretic Mode

Hysteretic Mode

Conversely, the transition from Hysteretic Mode to PWM Mode occurs when the SW node is negative for eight consecutive cycles.

A sudden increase in the output current causes a change from Hysteretic to PWM Mode. This load increase causes an instantaneous decrease in the output voltage due to the voltage drop on the output capacitor ESR. If the load causes the output voltage (as presented at V_{SNS}) to drop below the hysteretic regulation level (20mV below V_{REF}), the mode is changed to PWM on the next clock cycle.

In Hysteretic Mode, the PWM comparator and the error amplifier that provide control in PWM Mode are inhibited and the hysteretic comparator is activated. In Hysteretic Mode, the low-side MOSFET is operated as a synchronous rectifier, where the voltage across $V_{DS(ON)}$ is monitored and switched off when $V_{DS(ON)}$ goes positive (current flowing back from the load), allowing the diode to block reverse conduction.

The hysteretic comparator initiates a PFM signal to turn on HDRV at the rising edge of the next oscillator clock, when the output voltage (at V_{SNS}) falls below the lower threshold (10mV below V_{REF}) and terminates the PFM signal or when V_{SNS} rises over the higher threshold (5mV above V_{REF}). The switching frequency is primarily a function of:

- Spread between the two hysteretic thresholds
- I_{LOAD}
- Output inductor and capacitor ESR.

A transition back to PWM continuous conduction mode (CCM) mode occurs when the inductor current rises sufficiently to stay positive for eight consecutive cycles. This occurs when:

$$I_{LOAD(CCM)} = \left(\frac{\Delta V_{HYSTERESIS}}{2\,ESR}\right) \quad (3)$$

where $\Delta V_{HYSTERESIS}$ = 15mV and ESR is the equivalent series resistance of C_{OUT}.

Because of the different control mechanisms, the value of the load current where transition into CCM operation takes place is typically higher compared to the load level at which transition into Hysteretic Mode occurs. Hysteretic Mode can be disabled by setting the FPWM pin LOW.

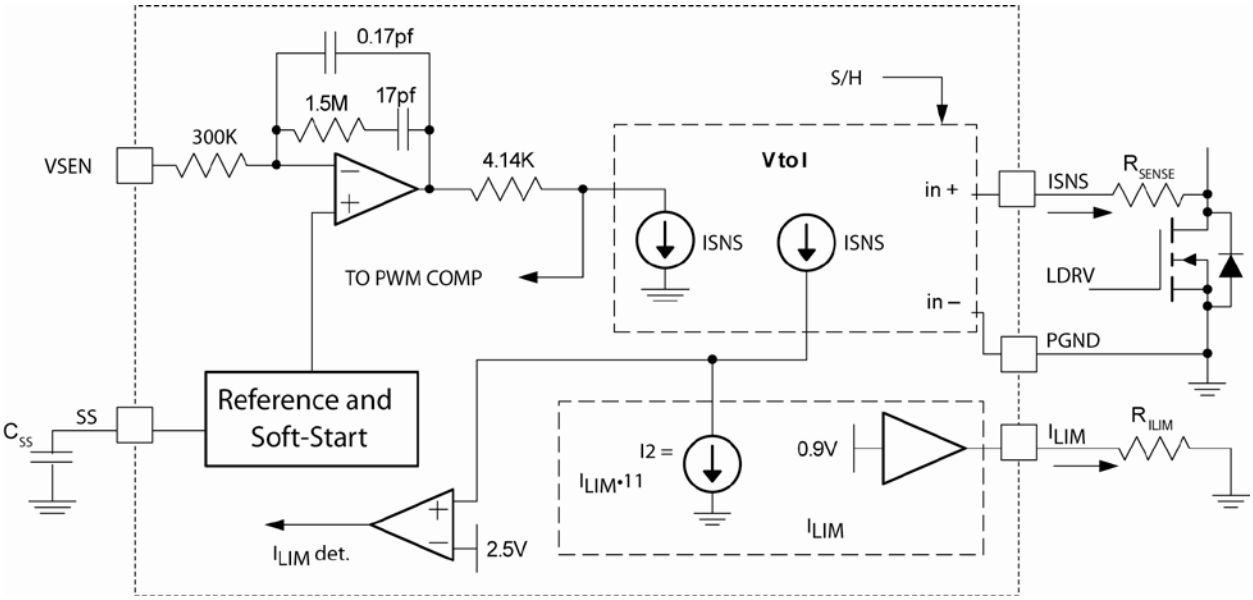


Figure 12. Current Limit / Summing Circuits

Current Processing Section

The current through the R_{SENSE} resistor (I_{SNS}) is sampled (typically 400ns) after Q2 is turned on, as shown in Figure 12. That current is held and summed with the output of the error amplifier. This effectively creates a current-mode control loop. The resistor connected to ISNSx pin (R_{SENSE}) sets the gain in the current feedback loop. The following expression estimates the recommended value of R_{SENSE} as a function of the maximum load current ($I_{LOAD(MAX)}$) and the value of the MOSFET $R_{DS(ON)}$:

$$R_{SENSE} = \left(\frac{I_{LOAD(MAX)} \bullet R_{DS(ON)}}{75\mu A} - 100\right) \quad (4)$$

R_{SENSE} must, however, be kept higher than 700Ω even if the number calculated comes out to be less than 700Ω.

Setting the Current Limit

A ratio of I_{SNS} is compared to the current established when a 0.9V internal reference drives the ILIM pin:

$$R_{LIM} = \frac{11}{I_{LOAD}} x \left(\frac{(100 + R_{SENSE})}{R_{DS(ON)}}\right) \quad (5)$$

Since the tolerance on the current limit is largely dependent on the ratio of the external resistors, it is fairly accurate if the voltage drop on the switching-node side of R_{SENSE} is an accurate representation of the load current. When using the MOSFET as the sensing element, the variation of $R_{DS(ON)}$ causes proportional variation in the I_{SNS}. This value varies from device to device and has a typical junction temperature coefficient of about 0.4%/°C (consult the MOSFET datasheet for actual values), so the actual current limit set point decreases proportional to increasing MOSFET die temperature. A factor of 1.6 in the current limit set point should compensate for MOSFET $R_{DS(ON)}$ variations, assuming the MOSFET heat sinking keeps its operating die temperature below 125°C.

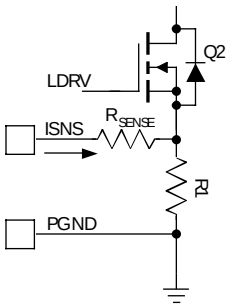


Figure 13. Improving Current-Sensing Accuracy

More accurate sensing can be achieved by using a resistor (R1) instead of the $R_{DS(ON)}$ of the FET, as shown in Figure 13. This approach causes higher losses, but yields greater accuracy in both V_{DROOP} and I_{LIMIT}. R1 is a low value resistor (e.g. 10mΩ).

Current limit (I_{LIMIT}) should be set high enough to allow inductor current to rise in response to an output load transient. Typically, a factor of 1.2 is sufficient. In addition, since I_{LIMIT} is a peak current cut-off value, multiply $I_{LOAD(MAX)}$ by the inductor ripple current (e.g. 25%). For example, in Figure 6, the target for I_{LIMIT}:

$$I_{LIMIT} > 1.2 \times 1.25 \times 1.6 \times 6A \approx 14.5A \quad (6)$$

Duty Cycle Clamp

During severe load increase, the error amplifier output can go to its upper limit, pushing a duty cycle to almost 100% for significant amount of time. This could cause a large increase of the inductor current and lead to a long recovery from a transient, over-current condition, or even to a failure at especially high input voltages. To prevent this, the output of the error amplifier is clamped to a fixed value after two clock cycles if severe output voltage excursion is detected, limiting the maximum duty cycle to:

$$DC_{MAX} = \frac{V_{OUT}}{V_{IN}} + \left(\frac{2.4}{V_{IN}}\right) \quad (7)$$

This is designed to not interfere with normal PWM operation. When FPWM is grounded, the duty cycle clamp is disabled and the maximum duty cycle is 87%.

Gate Driver Section

The adaptive gate control logic translates the internal PWM control signal into the MOSFET gate drive signals, providing necessary amplification, level shifting, and shoot-through protection. It also has functions that optimize the IC performance over a wide range of operating conditions. Since MOSFET switching time can vary dramatically from type to type and with the input voltage, the gate control logic provides adaptive dead time by monitoring the gate-to-source voltages of both upper and lower MOSFETs. The lower MOSFET drive is not turned on until the gate-to-source voltage of the upper MOSFET has decreased to less than approximately 1V. Similarly, the upper MOSFET is not turned on until the gate-to-source voltage of the lower MOSFET has decreased to less than approximately 1V. This allows a wide variety of upper and lower MOSFETs to be used without a concern for simultaneous conduction or shoot-through.

There must be a low-resistance, low-inductance path between the driver pin and the MOSFET gate for the adaptive dead-time circuit to function properly. Any delay along that path subtracts from the delay generated by the adaptive dead-time circuit and shoot-through may occur.

Frequency Loop Compensation

Due to the implemented current-mode control, the modulator has a single-pole response with -1 slope at frequency determined by load:

$$f_{PO} = \frac{1}{2\pi R_O C_O} \quad (8)$$

where R_O is load resistance; C_O is load capacitance.

For this type of modulator, a Type-2 compensation circuit is usually sufficient. To reduce the number of external components and simplify the design, the PWM controller has an internally compensated error amplifier. Figure 14 shows a Type-2 amplifier, its response, and the responses of a current-mode modulator and the converter. The Type-2 amplifier, in addition to the pole at the origin, has a zero-pole pair that causes a flat gain region at frequencies between the zero and the pole.

$$f_Z = \frac{1}{2\pi R_2 C_1} = 6kHz \quad (9)$$

$$f_P = \frac{1}{2\pi\pi_2 C_2} = 600kHz \quad (10)$$

This region is also associated with phase “bump” or reduced phase shift. The amount of phase-shift reduction depends on the width of the region of flat gain and has a maximum value of 90°. To further simplify the converter compensation, the modulator gain is kept independent of the input voltage variation by providing feedforward of V_{IN} to the oscillator ramp. The zero frequency, the amplifier high-frequency gain, and the modulator gain are chosen to satisfy most typical applications. The crossover frequency appears at the point where the modulator attenuation equals the amplifier high-frequency gain. The system designer must specify the output filter capacitors to position the load main pole somewhere within a decade lower than the amplifier zero frequency. With this type of compensation, plenty of phase margin is achieved due to zero-pole pair phase “boost.”

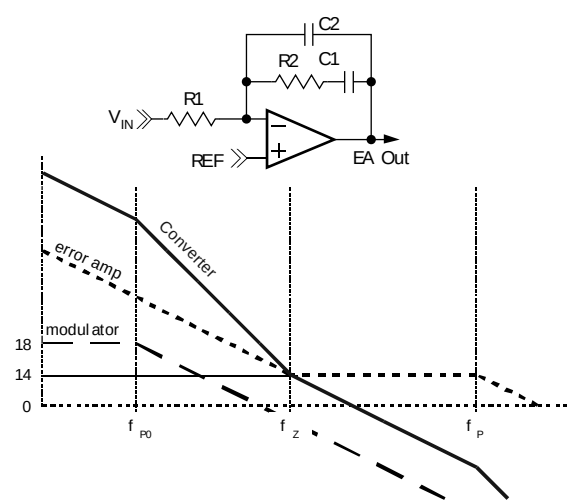


Figure 14. Compensation

Conditional stability may occur only when the main load pole is positioned too much to the left side on the frequency axis due to excessive output filter capacitance. In this case, the ESR zero placed within the 10kHz to 50kHz range gives some additional phase boost. There is an opposite trend in mobile applications to keep the output capacitor as small as possible.

If a larger inductor value or low-ESR values are required by the application, additional phase margin can be achieved by putting a zero at the LC crossover frequency. This can be achieved with a capacitor across the feedback resistor (e.g. R5 from Figure 6), as shown in Figure 15.

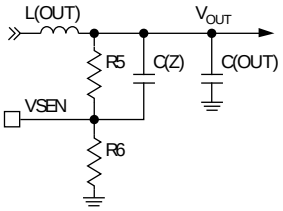


Figure 15. Improving Phase Margin

The optimal value of C(Z) is:

$$C(Z) = \frac{\sqrt{L(OUT)} \times C(OUT)}{R} \quad (11)$$

Protections

The converter output is monitored and protected against extreme overload, short-circuit, over-voltage, and under-voltage conditions.

A sustained overload on an output sets the PGx pin LOW and latches off the regulator on which the fault occurs. Operation can be restored by cycling the V_{CC} voltage or by toggling the EN pin.

If V_{OUT} drops below the under-voltage threshold, the regulator shuts down immediately.

Over-Current Sensing

If the circuit's current limit signal ("ILIM det" in Figure 12) is HIGH at the beginning of a clock cycle, a pulse-skipping circuit is activated and HDRV is inhibited. The circuit continues to pulse skip in this manner for the next eight clock cycles. If at any time from the ninth to the sixteenth clock cycle, the ILIM det is again reached, the over-current protection latch is set, disabling the regulator. If ILIM det does not occur between cycles nine and sixteen, normal operation is restored and the over-current circuit resets itself.

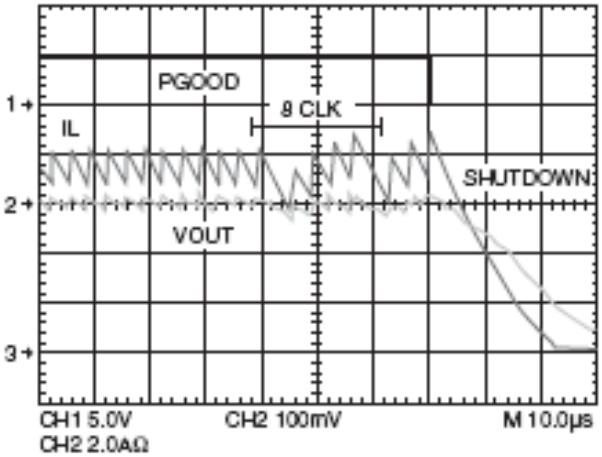


Figure 16. Over-Current Protection Waveforms

Over-Voltage / Under-Voltage Protection

Should the V_{SNS} voltage exceed 120% of V_{REF} (0.9V) due to an upper MOSFET failure or for other reasons, the over-voltage protection comparator forces LDRV HIGH. This action actively pulls down the output voltage and, in the event of the upper MOSFET failure, eventually blows the battery fuse. As soon as the output voltage drops below the threshold, the OVP comparator is disengaged.

This OVP scheme provides a "soft" crowbar function, which accommodates severe load transients and does not invert the output voltage when activated — a common problem for latched OVP schemes.

Similarly, if an output short-circuit or severe load transient causes the output to drop to less than 75% of the regulation set point, the regulator shuts down.

Over-Temperature Protection

The chip incorporates an over-temperature protection circuit that shuts the chip down if a die temperature of about 150°C is reached. Normal operation is restored at die temperature below 125°C with internal power-on reset asserted, resulting in a full soft-start cycle.

Design and Component Selection Guidelines

As an initial step, define operating input voltage range, output voltage, and minimum and maximum load currents for the controller.

Setting the Output Voltage

The internal reference voltage is 0.9V. The output is divided down by a voltage divider to the VSEN pin (for example, R5 and R6 in Figure 5). The output voltage therefore is:

$$\frac{0.9V}{R6} = \frac{V_{OUT} - 0.9V}{R5} \quad (12)$$

To minimize noise pickup on this node, keep the resistor to GND (R6) below 2K; for example, R6 at 1.82KΩ. Then choose R5:

$$R5 = \frac{(1.82K\Omega)(V_{OUT} - 0.9)}{0.9} = 3.24K \quad (13)$$

For DDR applications converting from 3.3V to 2.5V or other applications requiring high duty cycles, the duty cycle clamp must be disabled by tying the converter's FPWM to GND. When converter's FPWM is at GND, the converter's maximum duty cycle is greater than 90%. When using as a DDR converter with 3.3V input, set up the converter for in-phase synchronization by tying the VIN pin to +5V.

Output Inductor Selection

The minimum practical output inductor value keeps inductor current just on the boundary of continuous conduction at some minimum load. The industry standard practice is to choose the minimum current somewhere from 15% to 35% of the nominal current. At light load, the controller can automatically switch to Hysteretic Mode of operation to sustain high efficiency. The following equations help to choose the proper value of the output filter inductor:

$$\Delta I = 2 \times 1_{MIN} = \frac{\Delta V_{OUT}}{ESR} \quad (14)$$

where ΔI is the inductor ripple current and ΔV_{OUT} is the maximum ripple allowed:

$$L = \frac{V_{IN} - V_{OUT}}{f_{SW} \times \Delta I} \times \frac{V_{OUT}}{V_{IN}} \quad (15)$$

for this example, use:

$$V_{IN} = 20, V_{OUT} = 2.5$$
$$\Delta I = 20\% \bullet 6A = 1.2A \quad (16)$$
$$f_{SW} = 300KHz$$

therefore:

$$L \approx 6\mu H \quad (17)$$

Output Capacitor Selection

The output capacitor serves two major functions in a switching power supply. Along with the inductor, it filters the sequence of pulses produced by the switcher and it supplies the load transient currents. The output capacitor requirements are usually dictated by ESR, inductor ripple current (ΔI), and the allowable ripple voltage (ΔV):

$$ESR < \frac{\Delta V}{\Delta I} \quad (18)$$

In addition, the capacitor's ESR must be low enough to allow the converter to stay in regulation during a load step. The ripple voltage due to ESR for the converter in Figure 6 is $120mV_{PP}$. Some additional ripple appears due to the capacitance value itself:

$$\Delta V = \frac{\Delta I}{C_{OUT} \times 8 \times f_{SW}} \quad (19)$$

which is only about 1.5mV, for the converter in Figure 6, and can be ignored.

The capacitor must also be rated to withstand the RMS current, which is approximately 0.3 X (ΔI), or about 400mA for the converter in Figure 6. High-frequency decoupling capacitors should be placed as close to the loads as physically possible.

Input Capacitor Selection

The input capacitor should be selected by its ripple current rating.

Two-Stage Converter Case

In DDR Mode (shown in Figure 5), the V_{TT} power input is powered by the V_{DDQ} output; therefore, all of the input capacitor ripple current is produced by the V_{DDQ} converter. A conservative estimate of the output current required for the 2.5V regulator is:

$$I_{REGI} = I_{VDDQ} + \frac{I_{VTT}}{2} \quad (20)$$

As an example, if the average I_{VDDQ} is 3A and average I_{VTT} is 1A, I_{VDDQ} current is about 3.5A. If average input voltage is 16V, RMS input ripple current is:

$$I_{RMS} = I_{OUT(MAX)} \sqrt{D - D^2} \quad (21)$$

where D is the duty cycle of the PWM1 converter:

$$D < \frac{V_{OUT}}{V_{IN}} = \frac{2.5}{16} \quad (22)$$

therefore:

$$I_{RMS} = 3.5 \sqrt{\frac{2.5}{16} - \left(\frac{2.5}{16}\right)^2} = 1.49A \quad (23)$$

Dual Converter 180° Phased

In dual mode (shown in Figure 6), both converters contribute to the capacitor input ripple current. With each converter operating 180° out of phase, the RMS currents add in the following fashion:

$$I_{RMS} = \sqrt{I_{RMS(1)}^{2} + I_{RMS(2)}^{2}} \text{ or} \quad (24)$$

$$I_{RMS} = \sqrt{(I_1)^2\left(D_1 - D_1^2\right) + (I_2)^2\left(D_2 - D_2^2\right)} \quad (25)$$

which, for the dual 3A converters shown in Figure 6, calculates to:

$$I_{RMS} = 1.4A \quad (26)$$

Power MOSFET Selection

Losses in a MOSFET are the sum of its switching (P_{SW}) and conduction (P_{COND}) losses.

In typical applications, the FAN5236 converter's output voltage is low with respect to its input voltage. Therefore, the lower MOSFET (Q2) is conducting the full load current for most of the cycle. Q2 should therefore be selected to minimize conduction losses, thereby selecting a MOSFET with low $R_{DS(ON)}$.

In contrast, the high-side MOSFET (Q1) has a shorter duty cycle and it's conduction loss has less impact. Q1, however, sees most of the switching losses, so Q1's primary selection criteria should be gate charge.

High-Side Losses

Figure 17 shows a MOSFET's switching interval, with the upper graph being the voltage and current on the drain-to-source and the lower graph detailing V_{GS} vs. time with a constant current charging the gate. The X-axis, therefore, is also representative of gate charge (Q_G). $C_{ISS} = C_{GD} + C_{GS}$ and it controls t1, t2, and t4 timing. C_{GD} receives the current from the gate driver during t3 (as V_{DS} is falling). The gate charge (Q_G) parameters on the lower graph are either specified or can be derived from MOSFET datasheets.

Assuming switching losses are about the same for both the rising edge and falling edge, Q1's switching losses occur during the shaded time when the MOSFET has voltage across it and current through it.

These losses are given by:

$$P_{UPPER} = P_{SW} + P_{COND} \quad (27)$$

$$P_{SW} = \left(\frac{V_{DS} \times I_L}{2} \times 2 \times t_S\right) f_{SW} \quad (28)$$

$$P_{COND} = \frac{V_{OUT}}{V_{IN}} \times I_{OUT}^{2} \times R_{DS(ON)} \quad (29)$$

P_{UPPER} is the upper MOSFET's total losses and P_{SW} and P_{COND} are the switching and conduction losses for a given MOSFET. $R_{DS(ON)}$ is at the maximum junction temperature (T_J). t_S is the switching period (rise or fall time), shown as t2+t3 in Figure 17.

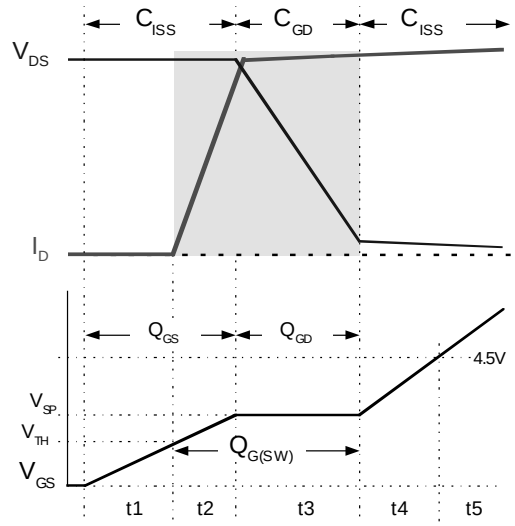


Figure 17. Switching Losses and Q_G

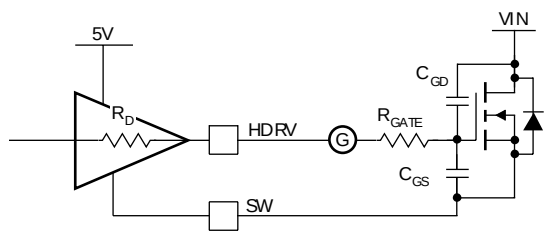


Figure 18. Drive Equivalent Circuit

The driver's impedance and C_{ISS} determine t2, while t3's period is controlled by the driver's impedance and Q_{GD}. Since most of t_S occurs when $V_{GS} = V_{SP}$, use a constant current assumption for the driver to simplify the calculation of t_S:

$$t_S = \frac{Q_{G(SW)}}{I_{DRIVER}} = \frac{Q_{G(SW)}}{\left(\frac{V_{CC} - V_{SP}}{R_{DRIVER} + R_{GATE}}\right)} \quad (30)$$

Most MOSFET vendors specify Q_{GD} and Q_{GS}. $Q_{G(SW)}$ can be determined as:

$$Q_{G(SW)} = Q_{GD} + Q_{GS} - Q_{TH} \quad (31)$$

where Q_{TH} is the gate charge required to get the MOSFET to its threshold (V_{TH}).

For the high-side MOSFET, $V_{DS} = V_{IN}$, which can be as high as 20V in a typical portable application. Care should be taken to include the delivery of the MOSFET's gate power (PGATE) in calculating the power dissipation required for the FAN5236:

$$P_{GATE} = Q_G \times V_{CC} \times f_{SW} \quad (32)$$

where Q_G is the total gate charge to reach V_{CC}.

Low-Side Losses

Q2, however, switches on or off with its parallel Schottky diode conducting; therefore $V_{DS} \approx 0.5V$. Since P_{SW} is proportional to V_{DS}, Q2's switching losses are negligible and Q2 is selected based on $R_{DS(ON)}$ only.

Conduction losses for Q2 are given by:

$$P_{COND} = (1 - D) \times I_{OUT}^{2} \times R_{DS(ON)} \quad (33)$$

where $R_{DS(ON)}$ is the $R_{DS(ON)}$ of the MOSFET at the highest operating junction temperature, and:

$$D = \frac{V_{OUT}}{V_{IN}} \quad (34)$$

is the minimum duty cycle for the converter.

Since $D_{MIN} < 20\%$ for portable computers, $(1-D) \approx 1$ produces a conservative result, further simplifying the calculation.

The maximum power dissipation ($P_{D(MAX)}$) is a function of the maximum allowable die temperature of the low-side MOSFET, the Θ_{JA}, and the maximum allowable ambient temperature rise:

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_{A(MAX)}}{\Theta_{JA}} \quad (35)$$

Θ_{JA} depends primarily on the amount of PCB area that can be devoted to heat sinking *(see ON Semiconductor Application Note AN-1029 — Maximum Power Enhancement Techniques for SO-8 Power MOSFETs)*.

Layout Considerations

Switching converters, even during normal operation, produce short pulses of current that could cause substantial ringing and be a source of EMI if layout constraints are not observed.

There are two sets of critical components in a DC-DC converter. The switching power components process large amounts of energy at high rates and are noise generators. The low-power components responsible for bias and feedback functions are sensitive to noise.

A multi-layer printed circuit board is recommended. Dedicate one solid layer for a ground plane. Dedicate another solid layer as a power plane and break this plane into smaller islands of common voltage levels.

Notice all the nodes that are subjected to high-dV/dt voltage swing; such as SW, HDRV, and LDRV. All surrounding circuitry tends to couple the signals from these nodes through stray capacitance. Do not oversize copper traces connected to these nodes. Do not place traces connected to the feedback components adjacent to these traces. It is not recommended to use high-density interconnect systems, or micro-vias, on these signals. The use of blind or buried vias should be limited to the low-current signals only. The use of normal thermal vias is at the discretion of the designer.

Keep the wiring traces from the IC to the MOSFET gate and source as short as possible and capable of handling peak currents of 2A. Minimize the area within the gate-source path to reduce stray inductance and eliminate parasitic ringing at the gate.

Locate small critical components, like the soft-start capacitor and current sense resistors, as close as possible to the respective pins of the IC.

The FAN5236 utilizes advanced packaging technology with lead pitch of 0.6mm. High-performance analog semiconductors utilizing narrow lead spacing may require special considerations in design and manufacturing. It is critical to maintain proper cleanliness of the area surrounding these devices.

Physical Dimensions

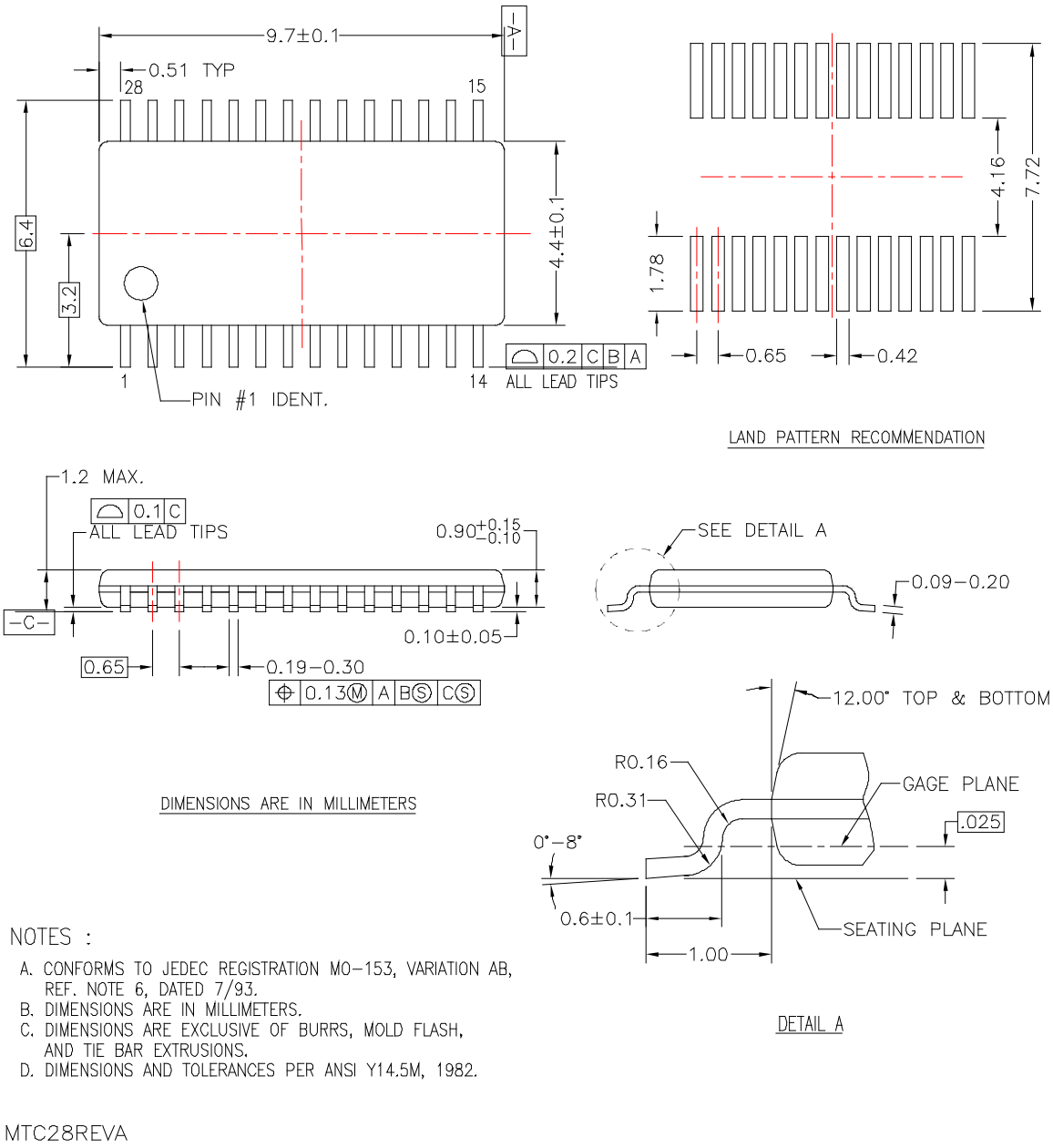


Figure 19. 28-Lead, Thin Shrink Outline Package

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