

2.5 W Power Amplifier 5.6 - 7.1 GHz

Rev. V1

Features

- 17 dB Small Signal Gain
- 48 dBm Third Order Intercept Point (OIP3)
- 2 W P1dB
- Integrated Power Detector
- Lead-Free 6 mm 24-lead QFN Package
- RoHS Compliant and 260°C Reflow Compatible

Description

The XP1039-QJ is a packaged linear power amplifier that operates from 5.6-7.1 GHz. The device provides 17 dB gain and 48 dBm Output Third Order Intercept Point (OIP3). The packaged amplifier comes in an industry standard, fully molded 6 mm QFN package and is comprised of a two stage power amplifier with an integrated, temperature compensated on-chip power detector. The device includes on-chip ESD protection structures and DC by-pass capacitors to ease the implementation and volume assembly of the packaged part.

The device is specifically designed for use in 6 GHz Point-to-Point radio applications.

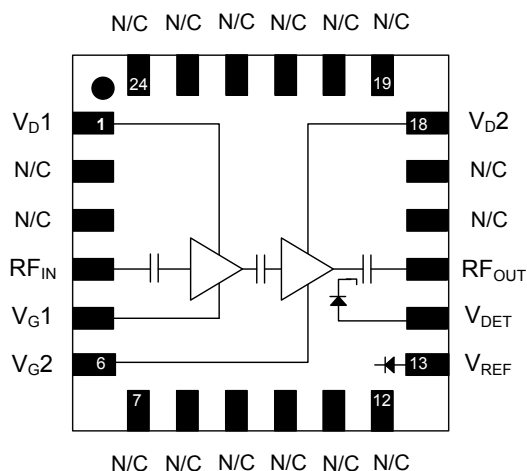
External DC blocks are required. See the reliability note on page 3 for more information.

Ordering Information^{1,2}

Part Number	Package
XP1039-QJ-0G00	bulk quantity
XP1039-QJ-0G0T	tape and reel
XP1039-QJ-EV1	evaluation module

1. Reference Application Note M513 for reel size information.
2. All sample boards include 5 loose parts.

Functional Schematic



Pin Configuration³

Pin No.	Pin Name	Function
1	V _{D1}	Drain 1 Bias
2-3	N/C	No Connection
4	RF _{IN}	RF Input
5	V _{G1}	Gate 1 Bias
6	V _{G2}	Gate 2 Bias
7-12	N/C	No Connection
13	V _{REF}	Power Det. Ref.
14	V _{DET}	Power Detector
15	RF _{OUT}	RF Output
16-17	N/C	No Connection
18	V _{D2}	Drain 2 Bias
19-24	N/C	No Connection
25 ⁴	Pad	Ground

3. It is recommended to connect unused pins to ground.
4. The exposed pad centered on the package bottom must be connected to RF and DC ground.

* Restrictions on Hazardous Substances, European Union Directive 2002/95/EC.

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Electrical Specifications: Freq: 5.9 - 7.1 GHz, $V_{DD} = 7\text{ V}$, $I_{DQ}^5 = 1350\text{ mA}$, $T_A = +25^\circ\text{C}$

Parameter	Units	Min.	Typ.	Max.
Small Signal Gain	dB	15	17	20
Input Return Loss	dB	—	10	—
Output Return Loss	dB	—	8	—
P1dB	dBm	—	33	—
Psat ⁶	dBm	—	34	—
Output IP3, +22 dBm SCL	dBm	43.5	48	—
Delta V_{DET} ($V_{DET} - V_{REF}$) @ 4 dBm P_{IN} , 7.1 GHz	V	—	-1.53	—
Detector Bias Voltage	VDC	—	5.0	—
Gate Bias Voltage ($V_{GG1,2}$)	VDC	—	-0.9	—

5. Adjust V_{GG1} and V_{GG2} between -1.4 and -0.4 V to achieve specified I_{DQ} . V_{GG1} and V_{GG2} should be the same voltage.

6. For reference only. Large signal operation is only recommended under pulsed conditions. Keep output power below P1dB for C.W. operation.

Maximum Operating Ratings^{7,8,9}

Parameter	Absolute Maximum
Input Power	+24 dBm
Drain Supply Voltage	+8 Volts
Junction Temperature ¹⁰	+160°C
Operating Temperature	-40°C to +85°C
Storage Temperature	-65°C to +150°C

7. Exceeding any one or combination of these limits may cause permanent damage to this device.
8. M/A-COM Technology Solutions does not recommend sustained operation near these survivability limits.
9. Operating at nominal conditions with $T_J \leq 160^\circ\text{C}$ will ensure $MTTF > 1 \times 10^6$ hours.
10. Junction Temperature (T_J) = $T_C + \Theta_{JC} * ((V * I) - (P_{OUT} - P_{IN}))$
Typical thermal resistance (Θ_{JC}) = 6.8°C/W
 - a) For $T_C = 25^\circ\text{C}$,
 $T_J = 88^\circ\text{C}$ @ 7 V, 1350 mA, $P_{OUT} = 23\text{ dBm}$, $P_{IN} = 6\text{ dBm}$
 - b) For $T_C = 85^\circ\text{C}$,
 $T_J = 148^\circ\text{C}$ @ 7 V, 1350 mA, $P_{OUT} = 21.5\text{ dBm}$, $P_{IN} = 6\text{ dBm}$

Absolute Maximum Ratings^{11,12}

Parameter	Absolute Max.
Supply Gate Voltage	-2.5 V
Supply Current (I_{D1})	600 mA
Supply Current (I_{D2})	1200 mA
Detector Pin	6 V
Detector Ref Pin	6 V
Continuous Power Dissipation @ 85°C	11.2 W
Junction Temperature	175°C

11. Channel temperature directly affects a device's MTTF. Channel temperature should be kept as low as possible to maximize lifetime.
12. For saturated performance it recommended that the sum of $(2 * V_{DD} + \text{abs}(V_{GG})) < 17$

Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

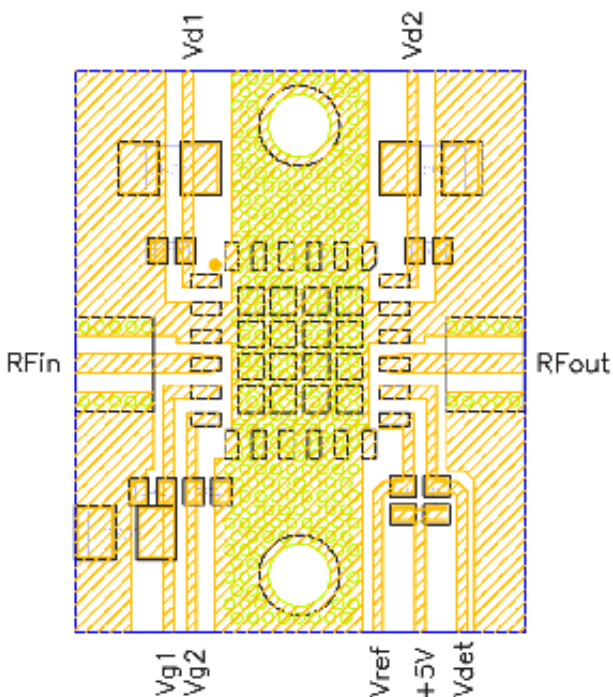
Gallium Arsenide Integrated Circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these Class 1A devices.

Important Reliability Information:

The input and output capacitors on the die may be damaged through handling and assembly processes. External DC blocks are recommended on the RF input and output lines on the PC board. If the output capacitor shorts due to ESD damage, the part will continue to function with slightly degraded performance. IP3 may decrease by approximately 1.5 dB. If the input capacitor shorts due to ESD damage, the part will continue to function with a slight shift in input return loss. Once shorted, the capacitor should remain shorted for the standard product lifetime. The external DC blocks are needed to maintain the bias point on the part.

Even though the ESD rating using the Human Body Model is Class 1A, it is recommended to treat this part as a Class 0 part. The rate of shorted capacitors due to ESD damage can be in the range of 10%. Shorted capacitors on this part are not subject to the warranty because the part continues to operate reliably with only slightly reduced performance.

Recommended Layout



METAL 1
METAL 2
SOLDERMASK TOP – POSITIVE VIEW
VIAS

MATERIAL: RO4350B, 10 mil.
CAPACITORS: 1 μ F (0805), 1000 pF (0402)

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App Note [1] Biasing - As shown in the Pin Designations table, the device is operated by biasing $V_{d1,2}$ at 7.0V. The nominal drain currents are $I_{d1}=450\text{mA}$ and $I_{d2}=900\text{mA}$. This ratio of 1:2 between the first and second stage drain currents should be maintained for best linearity. The typical gate voltages needed are -0.9V. The negative gate voltage must be applied prior to applying the positive drain voltage.

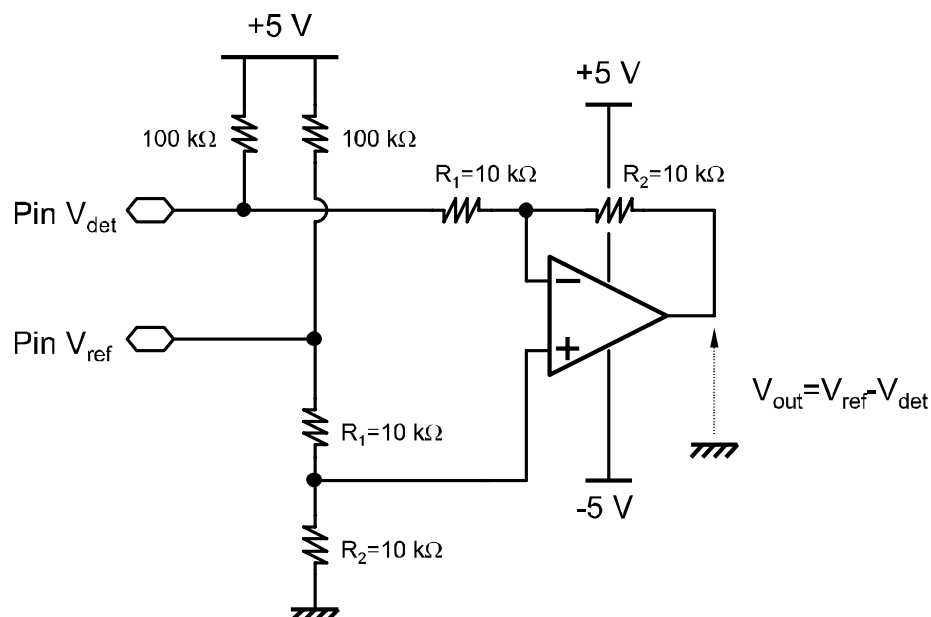
The XP1039-QJ is recommended for linear applications only. Active bias is recommended to keep the currents known and constant, and to maintain the best performance over temperature. Depending on the supply voltage available and the power dissipation constraints, the bias circuit may be a single transistor or a low-power operational amplifier, with a low value resistor in series with the drain supply used to sense the current.

App Note [2] PWB Layout Considerations - It is recommended to provide 100pF decoupling capacitors as close as possible to the pins of the device, with additional larger decoupling capacitors further away. For example, in the Recommended Layout shown below, there are 100pF 0402 capacitors placed very near the device pins, and 1uF 0805 capacitors placed further away (the gate line shown without a 1uF capacitor (pin 6) would have this capacitor further away on the other side of the screw).

Thermal management of the device is essential. It is recommended that measures such as copper-filled vias under the package, and post/screws for top to bottom heat transfer are used (see Recommended Layout shown below). Adequate heat-sinking under the PWB is necessary in maintaining the package base at a safe operating temperature.

App Note [3] Power Detector - As shown in the schematic at right, the power detector is implemented by providing +5V bias and measuring the difference in output voltage with standard op-amp in a differential mode configuration.

Application Schematic

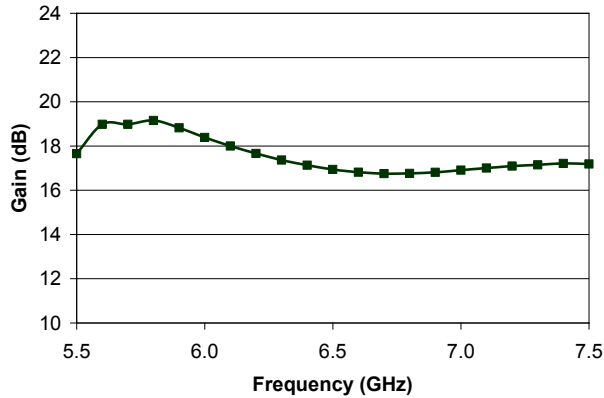


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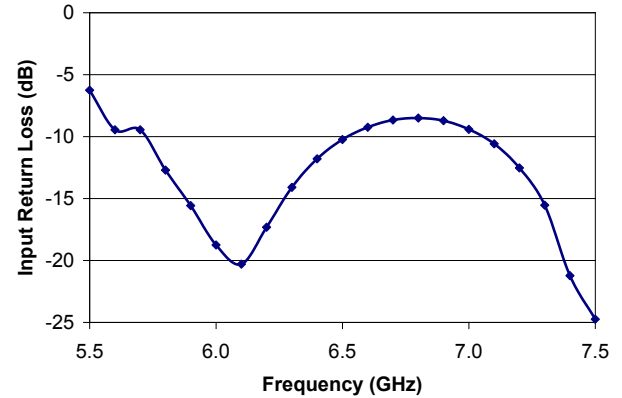
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Typical Performance Curves: $V_{DD} = 7\text{ V}$, $I_{DQ} = 1350\text{ mA}$

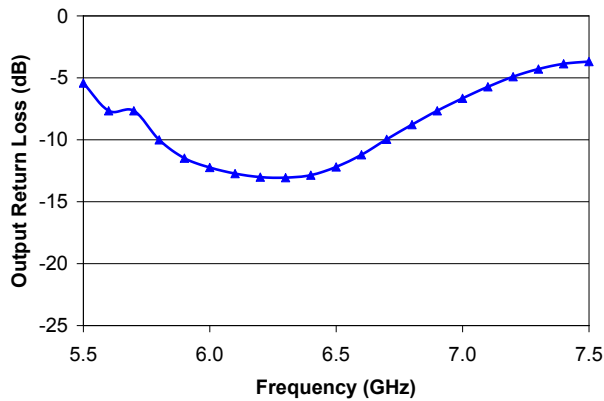
Gain vs. Frequency, +25C



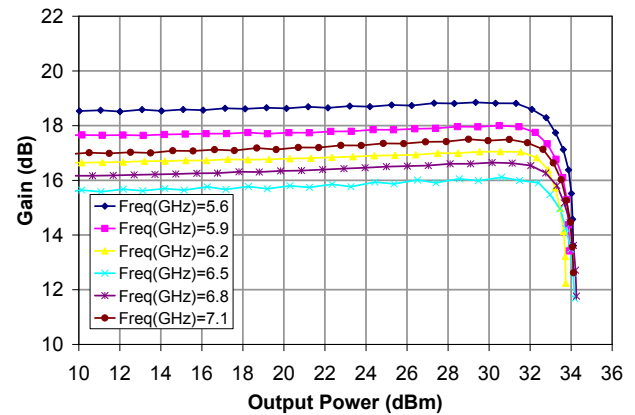
Input Return Loss vs. Frequency, +25C



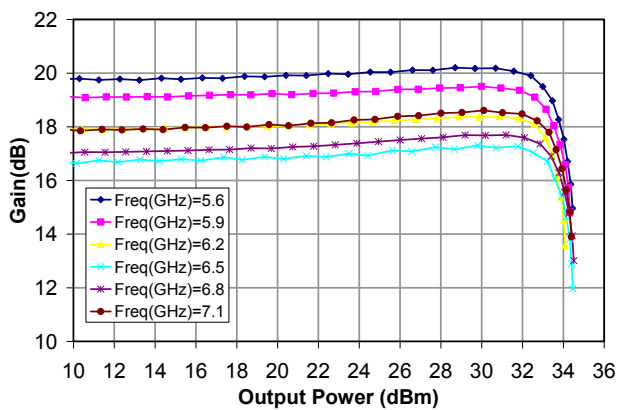
Output Return Loss vs. Frequency, +25C



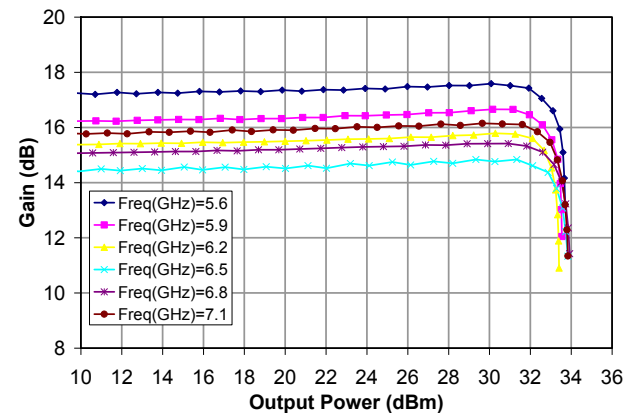
Gain vs. Output Power, +25C



Gain vs. Output Power, -40C



Gain vs. Output Power, +85C

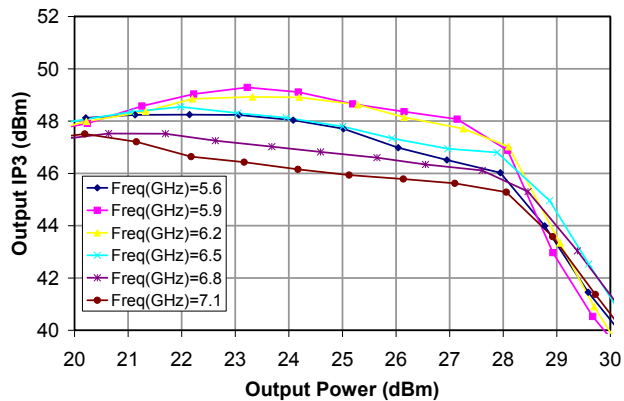


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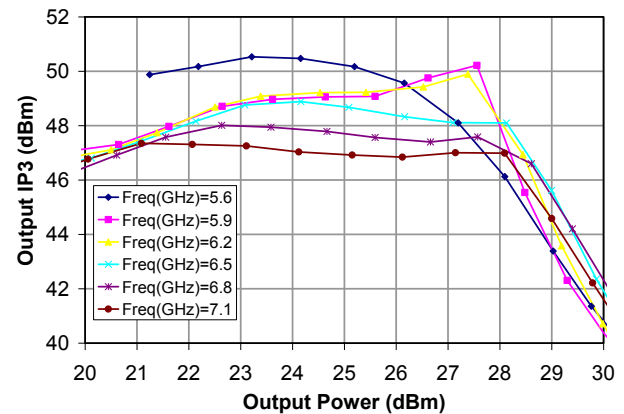
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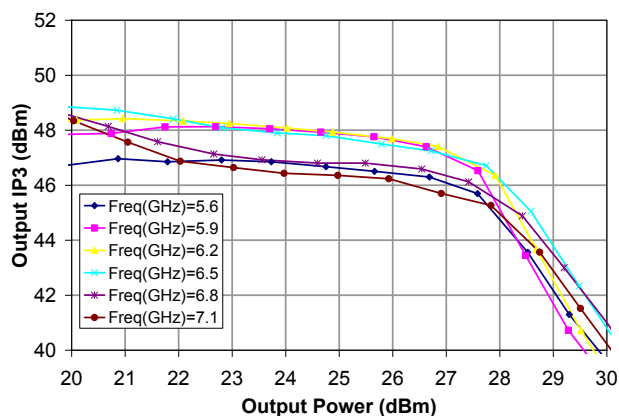
Output IP3 vs. Output Power, +25°C



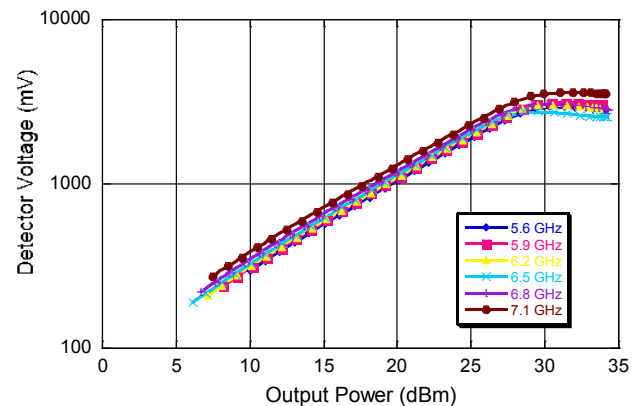
Output IP3 vs. Output Power, -40°C



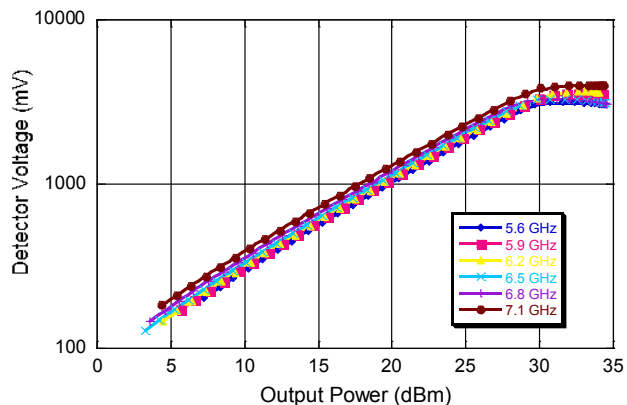
Output IP3 vs. Output Power, +85°C



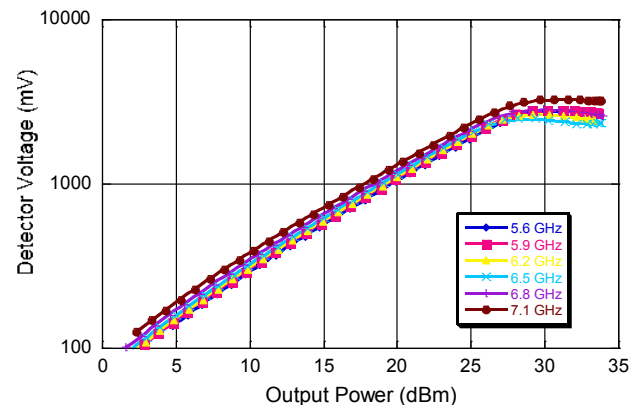
Detector Voltage ($V_{REF} - V_{DET}$) vs. Output Power, +25°C



Detector Voltage ($V_{REF} - V_{DET}$) vs. Output Power, -40°C



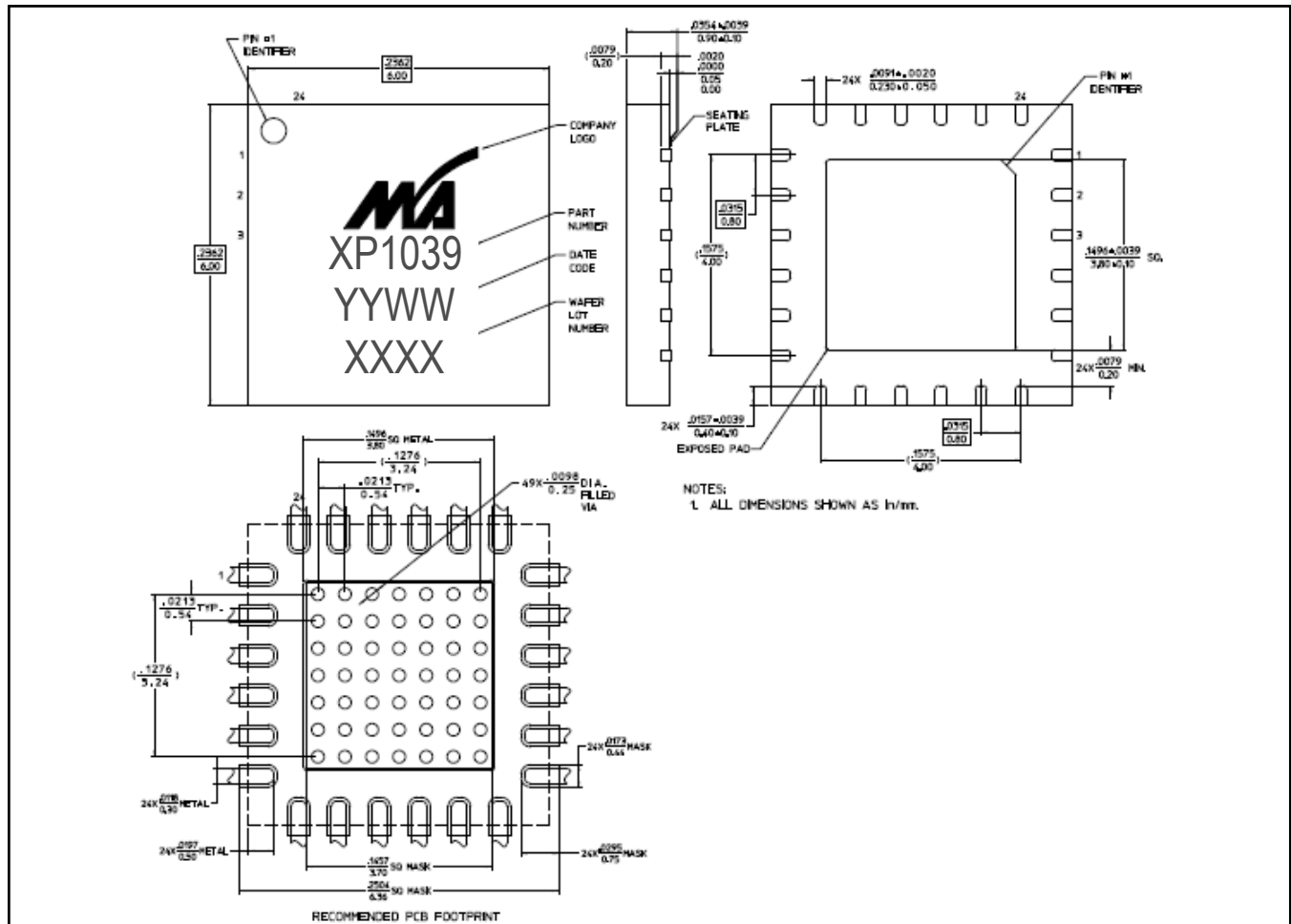
Detector Voltage ($V_{REF} - V_{DET}$) vs. Output Power, +85°C



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Lead-Free 6 mm 24-Lead PQFN[†]



- † Reference Application Note S2083 for lead-free solder reflow recommendations.
Meets JEDEC moisture sensitivity level 3 requirements.
Plating is 100% matte tin over copper.

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