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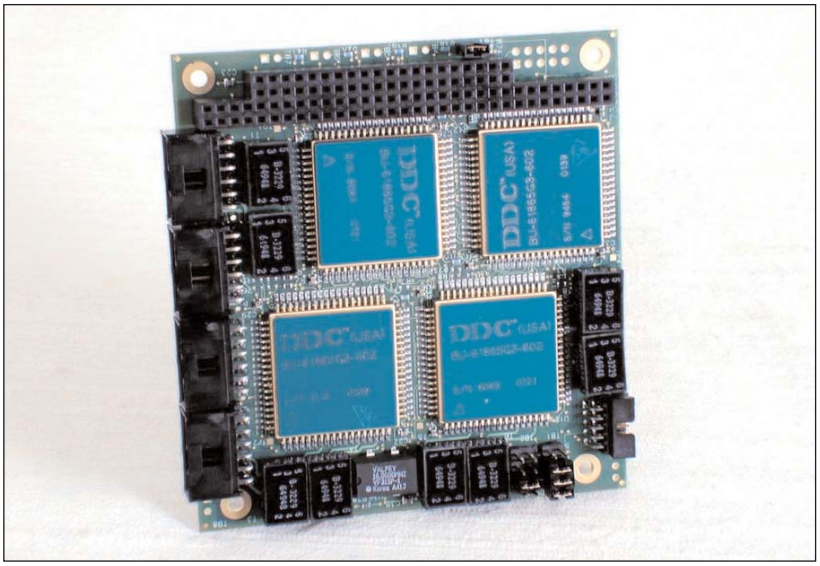
BU-65568CX
MIL-STD-1553 BC/RT/MT PC/104 CARD



DESCRIPTION

DDC's BU-65568 PC/104 card provides a complete COTS solution for interfacing between an embedded PC/104 bus and a MIL-STD-1553 bus. The card's two addressing modes serve to provide compatibility with both Intel and Motorola processor platforms.

The BU-65568 includes one to four channels of DDC's proven industry standard Enhanced Mini-ACE. The card's advanced bus controller architecture provides a high degree of flexibility and autonomy. This includes methods to control message scheduling, the means to minimize host overhead for asynchronous message insertion, facilitate bulk data transfers and double buffering, and support various message retry and bus switching strategies. The BC architecture also provides flexibility for data logging and fault reporting.

The card's remote terminal architecture provides flexibility in meeting all common MIL-STD-1553 protocols. The choice of RT data buffering and interrupt options provides robust support for synchronous and asynchronous messaging, while ensuring data sample consistency and supporting bulk data transfers.

The card includes a true message monitor mode, along with a combined RT/Monitor mode. The monitor provides highly flexible message filtering, along with a robust interrupt architecture to simplify host software.

The BU-65568 card also includes an 8-bit bi-directional I/O port.

The BU-65568 is supported by free software, including a "C" library and drivers for specific operating systems, including VxWorks. The library and drivers comprise a suite of "C" function calls that serves to offload a great deal of low-level tasks from the application programmer. This software supports all of the Enhanced Mini-ACE's advanced architectural features.

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FEATURES

- 16-bit Card per PC/104 Version 2.3
- One to Four Dual Redundant MIL-STD-1553 Channels
- Convection Cooled
- Extended Temperature Range Available
- Enhanced Mini-ACE RT-only or BC/RT/MT Architecture
- 4K or 64K-word RAM per Channel
- Choice of Segmented or Flat Addressing Mode
- Highly Autonomous Bus Controller Architecture
  - Asynchronous Messages
  - Message Timing Control
  - Bulk Data Transfers
  - Data Block Double Buffering
  - Retries and Bus Switching
- RT Buffering Options
  - Single Buffering
  - Double Buffering
  - Subaddress Circular Buffering
  - Global Circular Buffering
- Selective Message Monitor
- Supports PC/104 Interrupts
- Software Support for DOS, Linux, VxWorks®, and Windows NT®

FOR MORE INFORMATION CONTACT:

Technical Support:
1-800-DDC-5757 ext. 7771

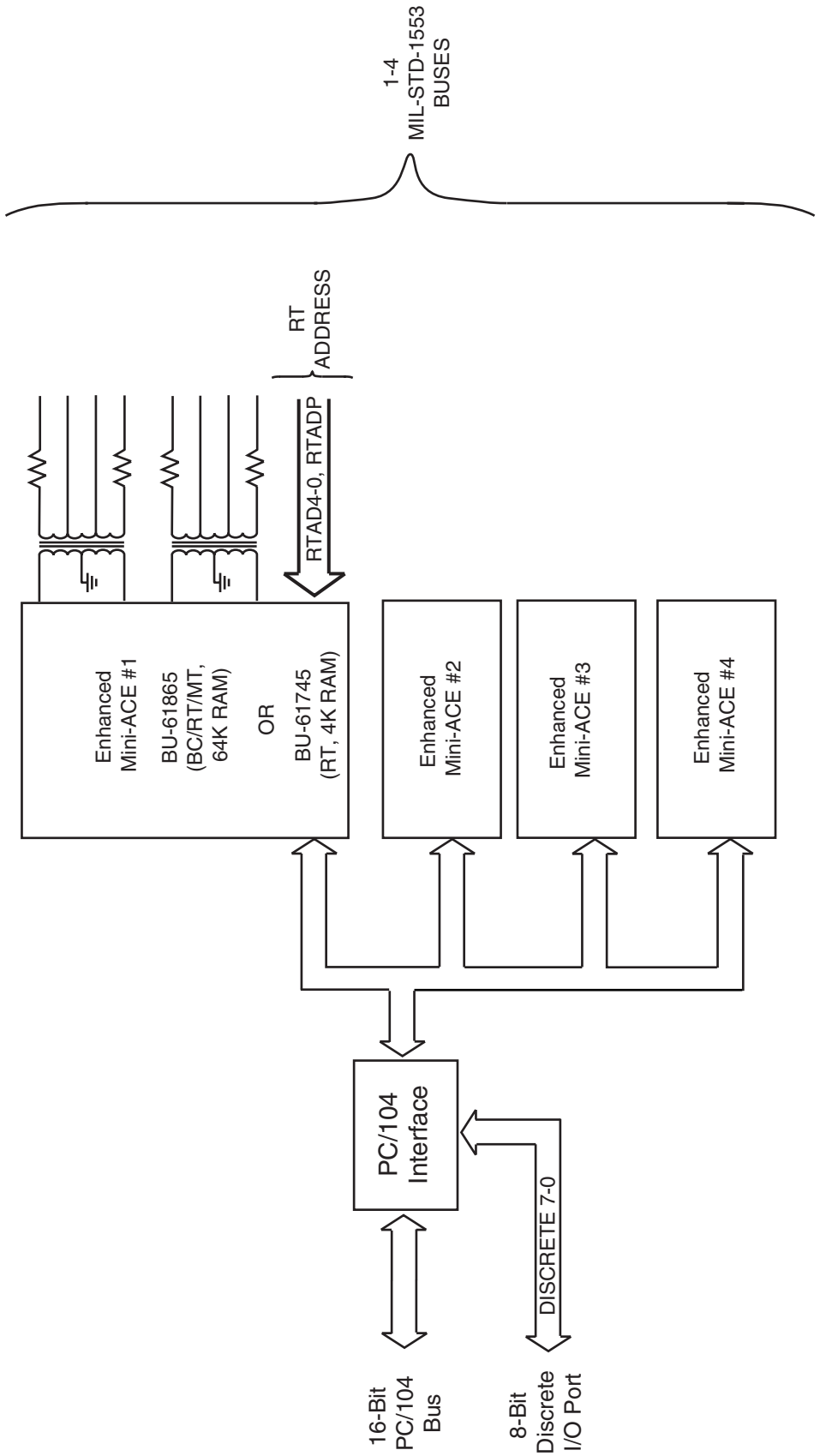


FIGURE 1. BU-65568 BLOCK DIAGRAM

TABLE 1. BU-65568 SPECIFICATIONS

PARAMETER	MIN	TYP	MAX	UNITS
ABSOLUTE MAXIMUM RATINGS				
+5 V Supply Voltage	-0.3		6.0	V
RECEIVER				
Input Impedance, Transformer Coupled (see Notes 1-3)	1.000			kohm
Threshold Voltage, Transformer Coupled	0.200		0.860	Vp-p
Common-Mode Voltage (see Note 4)			10	VPEAK
TRANSMITTER				
Differential Output Voltage				
Transformer Coupled, Across 70 Ohms	18	20	27	Vp-p
Output Offset Voltage				
Transformer Coupled, Across 70 Ohms	-250	150	250	mVPEAK
Rise/Fall Time	100	150	300	ns
POWER SUPPLY REQUIREMENTS				
Voltages/Tolerances				
+ 5 V	4.75	5.0	5.25	V
Current Drain @ + 5.0 V				
BU-65567X1				
• Idle			200	mA
• 25% Transmitter Duty Cycle			310	mA
• 50% Transmitter Duty Cycle			420	mA
• 100% Transmitter Duty Cycle			640	mA
BU-65568X1				
• Idle			220	mA
• 25% Transmitter Duty Cycle			330	mA
• 50% Transmitter Duty Cycle			440	mA
• 100% Transmitter Duty Cycle			660	mA
BU-65567X2				
• Idle			340	mA
• 25% Transmitter Duty Cycle			560	mA
• 50% Transmitter Duty Cycle			880	mA
• 100% Transmitter Duty Cycle			1.22	A
BU-65568X2				
• Idle			380	mA
• 25% Transmitter Duty Cycle			600	mA
• 50% Transmitter Duty Cycle			920	mA
• 100% Transmitter Duty Cycle			1.26	A
BU-65567X3				
• Idle			480	mA
• 25% Transmitter Duty Cycle			810	mA
• 50% Transmitter Duty Cycle			1.14	A
• 100% Transmitter Duty Cycle			1.80	A
BU-65568X3				
• Idle			540	mA
• 25% Transmitter Duty Cycle			870	mA
• 50% Transmitter Duty Cycle			1.2	A
• 100% Transmitter Duty Cycle			1.86	A
BU-65567X4				
• Idle			620	mA
• 25% Transmitter Duty Cycle			1.06	A
• 50% Transmitter Duty Cycle			1.50	A
• 100% Transmitter Duty Cycle			2.38	A
BU-65568X4				
• Idle			700	mA
• 25% Transmitter Duty Cycle			1.14	A
• 50% Transmitter Duty Cycle			1.58	A
• 100% Transmitter Duty Cycle			2.46	A
POWER DISSIPATION				
BU-65567X1				
• Idle			0.84	W
• 25% Transmitter Duty Cycle			1.12	W
• 50% Transmitter Duty Cycle			1.41	W
• 100% Transmitter Duty Cycle			1.98	W

TABLE 1. BU-65568 SPECIFICATIONS (CONT.)

PARAMETER	MIN	TYP	MAX	UNITS
POWER DISSIPATION (CONT)				
BU-65568X1				
• Idle			0.84	W
• 25% Transmitter Duty Cycle			1.12	W
• 50% Transmitter Duty Cycle			1.41	W
• 100% Transmitter Duty Cycle			1.98	W
BU-65567X2				
• Idle			1.53	W
• 25% Transmitter Duty Cycle			2.10	W
• 50% Transmitter Duty Cycle			2.67	W
• 100% Transmitter Duty Cycle			3.81	W
BU-65568X2				
• Idle			1.53	W
• 25% Transmitter Duty Cycle			2.10	W
• 50% Transmitter Duty Cycle			2.67	W
• 100% Transmitter Duty Cycle			3.81	W
BU-65567X3				
• Idle			2.23	W
• 25% Transmitter Duty Cycle			3.08	W
• 50% Transmitter Duty Cycle			3.93	W
• 100% Transmitter Duty Cycle			5.64	W
BU-65568X3				
• Idle			2.23	W
• 25% Transmitter Duty Cycle			3.08	W
• 50% Transmitter Duty Cycle			3.93	W
• 100% Transmitter Duty Cycle			5.64	W
BU-65567X4				
• Idle			2.92	W
• 25% Transmitter Duty Cycle			4.06	W
• 50% Transmitter Duty Cycle			5.20	W
• 100% Transmitter Duty Cycle			7.47	W
BU-65568X4				
• Idle			2.92	W
• 25% Transmitter Duty Cycle			4.06	W
• 50% Transmitter Duty Cycle			5.20	W
• 100% Transmitter Duty Cycle			7.47	W
HOTTEST DIE				
• Idle			0.22	W
• 25% Transmitter Duty Cycle			0.42	W
• 50% Transmitter Duty Cycle			0.62	W
• 100% Transmitter Duty Cycle			1.02	W
1553 MESSAGE TIMING				
Completion of CPU Write (BC Start)-to-Start of Next Message (Non-enhanced BC Mode)		2.5		µs
BC Intermessage Gap - (Note 5)				
Non-Enhanced (Mini-ACE compatible BC mode)		9.5		µs
Enhanced BC mode (Note 6)		10-10.5		µs
BC/RT/MT Response Timeout (Note 7)				
18.5 nominal	17.5	18.5	19.5	µs
22.5 nominal	21.5	22.5	23.5	µs
50.5 nominal	49.5	50.5	51.5	µs
128.0 nominal	127	129.5	131	µs
RT Response Time (mid-parity to mid-sync) (Note 8)	4		7	µs
Transmitter Watchdog Timeout		660.5		µs
THERMAL				
Card Operating Temperature				
BU-65568CX-200	-40		+85	°C
BU-65568CX-300	0		+55	°C
BU-65568CX-900	-55		+85	°C
BU-61745/61865 Thermal Resistance, Junction-to-Case (θJC)			7	°C/W
Operating Junction Temperature	-55		150	°C
Storage Temperature	-65		150	°C

TABLE 1. BU-65568 SPECIFICATIONS (CONT.)				
PARAMETER	**MIN**	**TYP**	**MAX**	**UNITS**
PHYSICAL CHARACTERISTICS				
Size		3.775 x 3.550 x 0.6 (95.9 x 90.2 x 15.2)		in (mm)
Weight BU-65568X4		4.2 (119)		oz (g)

Notes (For TABLE 1):

(1) Specifications are applicable for both unpowered and powered conditions.
(2) Specifications assume a 2 volt rms balanced, differential, sinusoidal input. Applicable frequency range is 75 kHz to 1 MHz.
(3) Minimum impedance is guaranteed over the operating range, but is not tested.
(4) Assumes a common-mode voltage within the frequency range of dc to 2 MHz, applied to pins of the isolation transformer on the stub side (transformer coupled), and referenced to signal.
(5) Typical value for minimum intermessage gap time. Under software control, this may be lengthened to 65,535 ms - message time, in increments of 1 µs. If ENHANCED CPU ACCESS, bit 14 of Configuration Register #6, is set to logic "1", then host accesses during BC Start-of-Message (SOM) and End-of-Message (EOM) transfer sequences could have the effect of lengthening the intermessage gap time. For each host access during an SOM or EOM sequence, the intermessage gap time will be lengthened by 6 clock cycles. Since there are 7 internal transfers during SOM, and 5 during EOM, this could theoretically lengthen the intermessage gap by up to 72 clock cycles; i.e., up to 7.2 ms with a 10 MHz clock, 6.0 µs with a 12 MHz clock, 4.5 µs with a 16 MHz clock, or 3.6 µs at 20 MHz clock.
(6) For Enhanced BC mode, the typical value for intermessage gap time is approximately 10 clock cycles longer than for the non-enhanced BC mode. That is, an addition of 1.0 µs at 10 MHz, 833 ns at 12 MHz, 625 ns at 16 MHz, or 500 ns at 20 MHz.
(7) Software programmable (4 options). Includes RT-to-RT Timeout (measured mid parity transmit Command Word to mid-sync of Transmitting RT Status Word).
(8) Measured from mid-parity crossing of Command Word to mid-sync crossing of RT's Status word.

INTRODUCTION

The BU-65568 is a single- or multi-channel MIL-STD-1553 PC/104 card supporting one to four dual redundant 1553 channels on a convection-cooled or conduction-cooled (consult factory) card. The design of the BU-65568 leverages the full capabilities of DDC's new Enhanced Mini-ACE (EMA). Features include a highly autonomous bus controller, an RT providing a wide variety of buffering options, and a selective message monitor. Each of the installed Enhanced Mini-ACE channels contains 64K words of RAM.

The essentially similar BU-65567 is limited to RT ONLY operation w/AutoBoot option. Each of the installed BU-65567 Enhanced Mini-ACE channels contain 4K words of RAM.

The Conduction-Cooled (Consult Factory) version of the BU-65568 includes thermal vias connected to chassis ground, and a chassis ground plane to provide improved thermal conduction.

Features of the board include:

- Each channel independently programmed for BC, RT, Monitor or RT/Monitor (**BU-65568 Only**)
- Programmable BC operation (**BU-65568 Only**)
- Conduction (Consult Factory) or convection cooled
- Transformer-coupled bus connection (Consult Factory for Direct-Coupled)
- 64 Kbytes of shared static RAM per installed channel (**BU-65568 Only**)

The BU-65568 is supported by free software, including a "C" library, VxWorks and DOS driver. This software supports all of the EMA's advanced architectural features.

ENHANCED MINI-ACE

The BU-65568 PC/104 card incorporates a 16-bit PC/104 interface, along with between one and four of DDC's BU-61865G3 BC/RT/MT or BU-61745G3 RT Enhanced Mini-ACE hybrids. Each Enhanced Mini-ACE comprises a complete, independent interface between the PC/104 bus and a dual redundant MIL-STD-1553 bus. The Enhanced Mini-ACE hybrids provide software compatibility with DDC's older generation ACE and Mini-ACE (Plus) terminals.

The Enhanced Mini-ACE provides complete multiprotocol support of MIL-STD-1553A/B/McAir and STANAG 3838. These hybrids include dual transceiver, along with protocol, host interface, memory management logic, and either 4K or 64K words of RAM. For the BC/RT/MT (64K) version, there is built-in parity checking for this RAM.

The Enhanced Mini-ACE's include a 5V, voltage source transceiver for improved line driving capability, with options for MIL-STD-1760 compliance (20 VP-P minimum transmitter voltage) or McAir compatibility (consult factory).

One of the new salient features of the Enhanced Mini-ACE is its new bus controller architecture. The Enhanced BC's highly autonomous message sequence control engine provides a means for offloading the host processor for implementing multi-frame message scheduling, message retry and bus switching schemes, data double buffering, and asynchronous message insertion. In addition, the Enhanced BC mode includes 8 general purpose flag bits, a general purpose queue, and user-defined interrupts, for the purpose of performing messaging to the host processor.

Another important feature of the Enhanced Mini-ACE is the incorporation of a fully autonomous built-in self-test. This test provides comprehensive testing of the internal protocol logic. A separate test verifies the operation of the Enhanced Mini-ACE's internal RAM. Since the self-tests are fully autonomous, they eliminate the need for the host to write and read stimulus and response vectors.

The Enhanced Mini-ACE RT offers the choice of single, double, and circular buffering for individual subaddresses or a global circular buffering option for multiple (or all) receive subaddresses, a 50% rollover interrupt for circular buffers, an interrupt status

queue for logging up to 32 interrupt events, and an option to automatically initialize to RT mode with the Busy bit set.

TRANSCEIVERS

The transceivers in the Enhanced Mini-ACE series terminals are fully monolithic, requiring only a +5 volt power input. The transmitters are voltage sources, which provide better line driving capability than current sources. This serves to improve performance on long buses with many taps. The BU-65568's transmitters may be trimmed to meet the MIL-STD-1760 requirement of a minimum of 20 volts peak-to-peak, transformer coupled (consult factory).

To provide compatibility to McAir specs, the BU-65568 is also available with an option for sinusoidal transmitters (consult factory).

Besides eliminating the demand for an additional power supply, the use of a +5V-only transceiver entails the use of a step-up, rather than step-down, isolation transformer. This provides the advantage of a higher terminal input impedance than is possible for a 15 volt or 12 volt transmitter. As a result, there is a greater margin for the input impedance test, as mandated by the MIL-STD-1553 RT validation test. This characteristic allows for longer cable lengths between the BU-65568's 1553 I/O connector and the system connector.

The receiver sections of the Enhanced Mini-ACE are fully compliant with MIL-STD-1553B Notice 2 in terms of front end overvoltage protection, threshold, common-mode rejection, and word error rate.

INTERRUPTS

The Enhanced Mini-ACE's may issue interrupt requests over the PC/104 bus. The PC/104 interrupt level is user-programmable from among levels 3, 4, 5, 7, 10, 11, 12, 14, or 15. The interrupt level is user-selectable by means of the base memory address I/O register. The interrupts for all Enhanced Mini-ACE(s) on a card are functionally OR'd together to provide a single interrupt output.

The BU-65568 allows multiple cards to be ganged on the same interrupt level. The interrupt outputs are open collector type signals, which provide 0.5 µs negative-going pulses.

SOFTWARE

The BU-69097 VxWorks driver, which is based on the BU-69090 "C" software library, provides comprehensive support of the BU-65568 card. This driver, which was developed in Microsoft Visual C++ 4.0, comprises a suite of function calls that serves to offload a great deal of low-level tasks from the application programmer.

MEMORY ALLOCATION

For each mode of operation - BC, RT, and Monitor - the library and driver operate under an open/access/close model, in which areas of RAM are autonomously allocated and de-allocated by means of low-level routines. While these functions may be invoked directly by an application, in general their operation is transparent to the application programmer. The library's memory manager module performs autonomous allocation of shared memory for stacks and data blocks. This provides a high degree of flexibility for sizing various data structures.

The memory management functions make use of handles consisting of starting addresses and sizes of memory blocks, along with status information delineating whether particular areas of shared RAM are unused, used, or protected. For each mode there are functions to transfer data between shared RAM data blocks and buffers in host memory. In addition, there are functions to access consolidated data structures providing both message status information, as well as 1553 message words.

MODE-SPECIFIC SOFTWARE

In BC mode, there is comprehensive support of the enhanced bus controller capabilities, allowing the user to leverage function calls and macros invoking the BC instruction set. Some of the functions support higher level tasks such as minor and major frame timing control and asynchronous message insertion. For the enhanced BC, the software also supports the offline development and compilation of BC message scenarios on (for example) a desktop PC. The binary images created from these may then be downloaded to the target processor environment.

In BC mode, the Enhanced Mini-ACE Run Time Library encapsulates all opcodes, data blocks, messages, and frames (major, minor, and asynchronous). This allows the user to create the desired 1553 BC activity, without the overhead of memory management. The library includes a function that creates 2 files which allow the user to view the opcode sequence generated by the library. The first file is a binary file which contains an image of ACE memory, and the second file is a 'C' header file that shows all locations to structures/frames within memory.

In RT mode, there is high level operation for configuring and utilizing the Enhanced Mini-ACE's single-buffer, double-buffer, and circular buffered subaddress memory management schemes. This includes methods for accessing synchronously and asynchronously received message data. There is also a mechanism provided for automatically reading and accessing the most recently received message. In addition, there is high-level support of subaddress illegalization and use of the busy bit, enhanced mode code handling, along with functions allowing for accessing user programmable status and BIT words.

In the message monitor mode, functions are provided for programming the command and data stack sizes, programming of the monitor "filter" table (which addresses/T-R/subaddresses to

monitor), along with high-level tools that decode monitored messages, and transfer status information and message words to host RAM in a consolidated stack data structure.

IMAGE FILES

As a means of reducing both the code size and the level of computational resources for embedded system software, the BU-69090 enables the library routines used to initialize the Enhanced Mini-ACE to be processed in an offline (non-embedded) development environment. By limiting the library's use to the non-flight environment, the user has greater control over the development and validation of the code for his embedded system.

The output of this process is a pure binary image file for the Enhanced Mini-ACE registers and shared RAM, along with header file information. The header file information provides data about the location and size of various data structures, along with source code for the four low-level functions to read and write Enhanced Mini-ACE registers and RAM.

The binary image may then be downloaded into the source of the embedded host program. As a result, to initialize the Enhanced Mini-ACE, all that the executable program needs to do is to write the image file to the Enhanced Mini-ACE registers and shared RAM. The header file information may then be used as a mechanism for determining the location and size of message blocks and other data structures.

I/O-MAPPED REGISTERS, MEMORY-MAPPED REGISTERS, AND MEMORY MAPPING

The BU-65568 contains a number of registers. Two of these are I/O-mapped, while the rest are memory mapped. The I/O base address is jumper-selectable. The card's base memory address is programmable by means of the Enhanced Mini-ACE Base Memory Address Register. This register is also used for selecting the card's interrupt level.

The base address of the card's memory-mapped registers is programmable by means of the Register Base Address Register. The memory mapped registers include all of the registers in the individual Enhanced Mini-ACE's. Note that the Enhanced Mini-ACE register space is 64 registers. As a result, all of the self-test registers are accessible by the PC/104 host. There also are four additional memory-mapped registers for the card: the Card ID Register, Channel/Segment Select Register, Interrupt Status Register, and Discrete I/O Register.

The Enhanced Mini-ACE Base Memory Address Register contains a MEMORY ENABLE bit, while the Register Base Address Register contains a REGISTER ENABLE bit. These bits, which default to logic "0" following power turn-on, must be set to logic "1" by the PC/104 host in order to enable host access to the card's memory and registers. Note that while either or both of these bits are logic "0", the card will continue to operate on the 1553 bus (if previously configured); however the card's registers and/or memory will not be host accessible.

The Card ID Register identifies the number of Enhanced Mini-ACE channels, whether each channel is an RT or a BC/RT/Monitor, and (for a BC/RT/Monitor card) whether the paged or flat addressing mode is used. The Channel/Segment Select Register is used in the paged (segmented) addressing mode for a BC/RT/Monitor card to select the 16 Kword (32 Kbyte) area of shared RAM within a specified Enhanced Mini-ACE that is currently accessible by the PC/104 host. The Interrupt Status Register may be used to determine which Enhanced Mini-ACE channel(s) have issued interrupt requests. The Discrete I/O Register is used to configure and access the BU-65568's discrete I/O port.

For a BU-65567 RT-only version of the card, the one to four BU-61845 Enhanced Mini-ACE(s) are located within the same 16 Kword (32 Kbyte) region of memory address space.

For the BU-65568 BC/RT/MT version of the card, the user may select between either of two different addressing modes. The selection of addressing mode is done by means of a jumper. The two addressing modes are: (1) a 32 Kbyte (16 Kword) paging mode (factory default); and (2) a flat addressing mode, which maps to an area of up to 512 Kbytes (256 Kwords), to accommodate up to four Enhanced Mini-ACE channels, with each channel containing 64K X 16 (128K X 8) of register/RAM address space.

The BU-65568 contains two I/O registers. The I/O base address is selected by means of jumpers. The two I/O registers are used to map the device into the host system.

TABLE 2. GENERAL PURPOSE I/O PORT REGISTER

BIT	DESCRIPTION
15 (MSB)	Direction 7
14	Direction 6
13	Direction 5
12	Direction 4
11	Direction 3
10	Direction 2
9	Direction 1
8	Direction 0
7	Data 7
6	Data 6
5	Data 5
4	Data 4
3	Data 3
2	Data 2
1	Data 1
0 (LSB)	Data 0

GENERAL PURPOSE I/O PORT

The BU-65568 includes an 8-bit discrete I/O port. This port is memory-mapped to the PC/104 host, with a memory word address of 0206h (byte address = 040Ch) relative to the card's base register address.

The upper 8 bits of this register specify the direction of each I/O signal (0 = input; 1 = output). The upper 8 bits are read/writable. The lower 8 bits control or enable reading of the respective I/O signal logic sense. Output bits are host read/writable. Any of bits 7-0 programmed as inputs are read-only. TABLE 2 illustrates the bit mapping for the General Purpose I/O Port Register.

BUS CONTROLLER (BC) ARCHITECTURE

The BC functionality for the Enhanced Mini-ACE includes two separate architectures: (1) the older, non-Enhanced mode, which provides complete compatibility with the previous ACE and Mini-ACE (Plus) generation products; and (2) the newer, Enhanced BC mode. The Enhanced BC mode offers several new powerful architectural features. These include the incorporation of a highly autonomous BC message sequence control engine, which greatly serves to offload the operation of the host CPU.

The Enhanced BC's message sequence control engine provides a high degree of flexibility for implementing major and minor frame scheduling; capabilities for inserting asynchronous messages in the middle of a frame; to separate 1553 message data from control/status data for the purpose of implementing double buffering and performing bulk data transfers; for implementing message retry schemes, including the capability for automatic bus channel switchover for failed messages; and for reporting various conditions to the host processor by means of 4 user-defined interrupts and a general purpose queue.

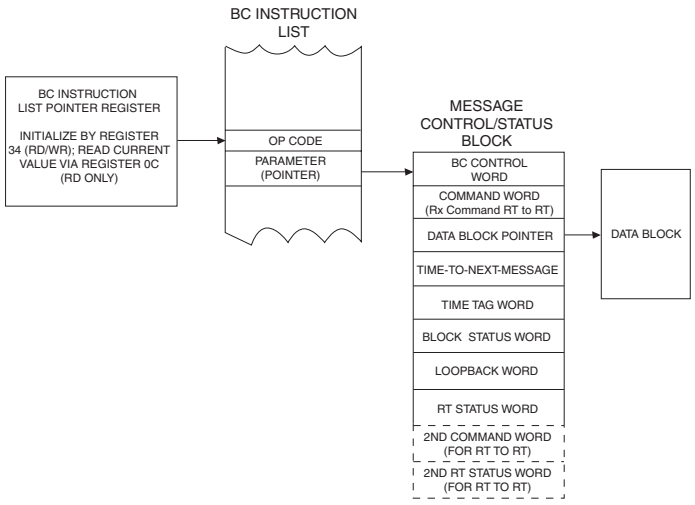


FIGURE 2. BC MESSAGE SEQUENCE CONTROL

In both the non-Enhanced and Enhanced BC modes, the Enhanced Mini-ACE BC implements all MIL-STD-1553B message formats. Message format is programmable on a message-by-message basis by means of the BC Control Word and the T/$\overline{R}$ bit of the Command Word for the respective message. The BC Control Word allows 1553 message format, 1553A/B type RT, bus channel, self-test, and Status Word masking to be specified on an individual message basis. In addition, automatic retries and/or interrupt requests may be enabled or disabled for individual messages. The BC performs all error checking required by MIL-STD-1553B. This includes validation of response time, sync type and sync encoding, Manchester II encoding, parity, bit count, word count, Status Word RT Address field, and various RT-to-RT transfer errors. The Enhanced Mini-ACE BC response timeout value is programmable with choices of 18, 22, 50, and 130 ms. The longer response timeout values allow for operation over long buses and/or use of repeaters.

In its non-Enhanced mode, the Enhanced Mini-ACE may be programmed to process BC frames of up to 512 messages with no processor intervention. In the Enhanced BC mode, there is no explicit limit to the number of messages that may be processed in a frame. In both modes, it is possible to program for either single frame or frame auto-repeat operation. In the auto-repeat mode, the frame repetition rate may be controlled either internally, using a programmable BC frame timer, or from an external trigger input.

ENHANCED BC MODE: MESSAGE SEQUENCE CONTROL

One of the major new architectural features of the Enhanced Mini-ACE series is its advanced capability for BC message sequence control. The Enhanced Mini-ACE supports highly autonomous BC operation, which greatly offloads the operation of the host processor.

The operation of the Enhanced Mini-ACE's message sequence control engine is illustrated in FIGURE 2. The BC message sequence control involves an instruction list pointer register; an instruction list which contains multiple 2-word entries; a message control/status stack, which contains multiple 8-word or 10-word descriptors; and data blocks for individual messages.

The initial value of the instruction list pointer register is initialized by the host processor (via Register 0D), and is incremented by the BC message sequence processor (host readable via Register 03). During operation, the message sequence control processor fetches the operation referenced by the instruction list pointer register from the instruction list.

Note that the pointer parameter referencing the first word of a message's control/status block (the BC Control Word) must contain an address value that is modulo 8. Also, note that if the message is an RT-to-RT transfer, the pointer parameter must contain an address value that is modulo 16.

TABLE 3. ENHANCED MINI-ACE REGISTERS

ADDRESS							REGISTER DESCRIPTION/ACCESSIBILITY
A6	A5	A4	A3	A2	A1	A0	
0	0	0	0	0	0	0/1	Interrupt Mask Register #1 (RD/WR)
0	0	0	0	0	1	0/1	Configuration Register #1 (RD/WR)
0	0	0	0	1	0	0/1	Configuration Register #2 (RD/WR)
0	0	0	0	1	1	0/1	Start/Reset Register
0	0	0	0	1	1	0/1	Non-Enhanced BC or RT Command Stack Pointer/Enhanced BC Instruction List Pointer Register (RD)
0	0	0	1	0	0	0/1	BC Control Word/RT Subaddress Control Word Register (RD/WR)
0	0	0	1	0	1	0/1	Time Tag Register (RD/WR)
0	0	0	1	1	0	0/1	Interrupt Status Register #1(RD)
0	0	0	1	1	1	0/1	Configuration Register #3 (RD/WR)
0	0	1	0	0	0	0/1	Configuration Register #4 (RD/WR)
0	0	1	0	0	1	0/1	Configuration Register #5 (RD/WR)
0	0	1	0	1	0	0/1	RT Monitor Data Stack Address Register (RD/WR)
0	0	1	0	1	1	0/1	BC Frame Time Remaining Register (RD)
0	0	1	1	0	0	0/1	BC Time Remaining to Next Message Register (RD)
0	0	1	1	0	1	0/1	BC Frame Time/Enhanced BC Initial Instruction Pointer/RT Last Command/MT Trigger Word Register (RD/WR)
0	0	1	1	1	0	0/1	RT Status Word Register (RD)
0	0	1	1	1	1	0/1	RT BIT Word Register
0	1	0	0	0	0	0/1	Test Mode Register 0
0	1	0	0	0	1	0/1	Test Mode Register 1
0	1	0	0	1	0	0/1	Test Mode Register 2
0	1	0	0	1	1	0/1	Test Mode Register 3
0	1	0	1	0	0	0/1	Test Mode Register 4
0	1	0	1	0	1	0/1	Test Mode Register 5
0	1	0	1	1	0	0/1	Test Mode Register 6
0	1	0	1	1	1	0/1	Test Mode Register 7
0	1	1	0	0	0	0/1	Configuration Register #6 (RD/WR)
0	1	1	0	0	1	0/1	Configuration Register #7 (RD/WR)
0	0	1	0	0	1	0/1	Reserved
0	1	1	0	1	1	0/1	BC Condition Code Register (RD)
0	1	1	0	1	1	0/1	BC General Purpose Flag Register (WR)
0	1	1	1	0	0	0/1	BIT Test Status Register (RD)
0	1	1	1	0	1	0/1	Interrupt Mask Register #2 (RD/WR)
0	1	1	1	1	0	0/1	Interrupt Status Register #2 (RD)
0	1	1	1	1	1	0/1	BC General Purpose Queue Pointer RT-MT Interrupt Status Queue Pointer Register (RD/WR)
0	1	1	1	1	1	0/1	Test Registers
1	•	•	•	•	•	0/1	
	•	•	•	•	•		
	•	•	•	•	•		
1	1	1	1	1	1	0/1	

OP CODES

The instruction list pointer register references a pair of words in the BC instruction list: an op code word, followed by a parameter word. The format of the op code word, which is illustrated in FIGURE 3, includes a 5-bit op code field and a 5-bit condition code field. The op code identifies the instruction to be executed by the BC message sequence controller.

Most of the operations are conditional, with execution dependent on the contents of the condition code field. Bits 3-0 of the condition code field identifies the particular condition. Bit 4 of the condition code field identifies the logic sense ("1" or "0") of the selected condition code on which the conditional execution is dependent. TABLE 4 lists all the op codes, along with their respective mnemonic, code value, parameter, and description. TABLE 5 defines all the condition codes.

Eight of the condition codes (8 through F) are set or cleared as the result of the most recent message. The other eight are defined as "General Purpose" condition codes GP0 through GP7. There are three mechanisms for programming the values of the General Purpose Condition Code bits: (1) They may be set, cleared, or toggled by the host processor by means of the BC GENERAL PURPOSE FLAG REGISTER; (2) they may be set, cleared, or toggled by the BC message sequence control processor by means of the GP Flag Bits (FLG) instruction; and (3) GP0 and GP1 only (but none of the others) may be set or cleared by means of the BC message sequence control processor's Compare Frame Timer (CFT) or Compare Message Timer (CMT) instructions.

The host processor also has read-only access to the BC condition codes by means of the BC CONDITION CODE REGISTER.

Note that four (4) instructions are unconditional. These are Compare to Frame Timer (CFT), Compare to Message Timer (CMT), GP Flag Bits (FLG), and Execute and Flip (XQF). For these instructions, the Condition Code Field is "don't care". That is, these instructions are always executed regardless of the result of the condition code test. All other instructions are conditional. That is, they will only be executed if the condition code specified by the condition code field in the op code word tests true. If the condition code field tests false, the instruction list pointer will skip down to the next instruction.

As shown in TABLE 4, many of the operations include a single-word parameter. For an XEQ (execute message) operation, the parameter is a pointer to the start of the message's control/status block. For other operations, the parameter may be an address, a time value, an interrupt pattern, a mechanism to set or clear general purpose flag bits, or an immediate value. For several op codes, the parameter is "don't care" (not used).

As described above, some of the op codes will cause the message sequence control processor to execute messages. In this case, the parameter references the first word of a message control/status block. With the exception of RT-to-RT transfer messages, all message status/control blocks are eight words long: a block control word, time-to-next-message parameter, data block pointer, command word, status word, loopback word, block status word, and time tag word.

In the case of an RT-to-RT transfer message, the size of the message control/status block increases to 16 words. However, in this case the last six words are not used; the ninth and tenth words are for the second command word and second status word.

The third word in the message control/status block is a pointer that references the first word of the message's data word block. Note that the data word block stores only data words, which are to be either transmitted or received by the BC. By segregating data words from command words, status words, and other control and "housekeeping" functions this architecture enables the use of convenient, usable data structures, such as circular buffers and double buffers.

Other operations support program flow control; i.e., jump and call capability. The call capability includes maintenance of a call stack that supports a maximum of four (4) entries, and there is also a return instruction. In the case of a call stack overrun or underrun, the BC will issue a CALL STACK POINTER REGISTER ERROR interrupt, if enabled.

Other op codes may be used to delay for a specified time, start a new BC frame, wait for an external trigger to start a new frame, do comparisons based on frame time and time-to-next message, load the time tag or frame time registers, halt, and issue host interrupts. In the case of host interrupts, the message control processor passes a 4-bit user-defined interrupt vector to the host by means of the Enhanced Mini-ACE's Interrupt Status Register.

The purpose of the FLG instruction is to enable the message sequence controller to set, clear, or toggle the value(s) of any or all of the eight general purpose condition flags.

The op code parity bit encompasses all sixteen bits of the op code word. This bit must be programmed for odd parity. If the message sequence control processor fetches an undefined op code word, an op code word with even parity, or bits 9-5 of an op code word do not have a binary pattern of 01010, the message sequence control processor will immediately halt the BC's operation. In addition, if enabled, a BC TRAP OP CODE interrupt will be issued. Also, if enabled, a parity error will result in an OP CODE PARITY ERROR interrupt.

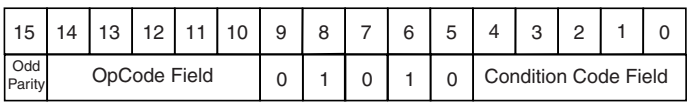


FIGURE 3. BC OP CODE FORMAT

TABLE 4. BC OPERATIONS FOR MESSAGE SEQUENCE CONTROL

INSTRUCTION	MNEMONIC	OP CODE (HEX)	PARAMETER	CONDITIONAL OR UNCONDITIONAL	DESCRIPTION
Execute Message	XEQ	0001	Message Control / Status Block Address	Conditional **(See NOTE)**	Executes the message at the specified Message Control/Status Block Address if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list.
Jump	JMP	0002	Instruction List Address	Conditional	Jump to the OpCode specified in the Instruction List if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list.
Subroutine Call	CAL	0003	Instruction List Address	Conditional	Jump to the OpCode specified by the Instruction List Address and push the Address of the Next OpCode on the Call Stack if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list. Note that the maximum depth of the subroutine call stack is **four**.
Subroutine Return	RTN	0004	Not Used (Don't Care)	Conditional	Return to the OpCode popped off the Call Stack if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list.
Interrupt Request	IRQ	0006	Interrupt Bit Pattern in 4 LS bits	Conditional	Generate an interrupt if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list. The passed parameter (Interrupt Bit Pattern) specifies which of the ENHANCED BC IRQ bit(s) (bits 5-2) will be set in Interrupt Status Register #2. Only the four LSBs of the passed parameter are used. A parameter where the four LSBs are logic "0" will **not** generate an interrupt.
Halt	HLT	0007	Not Used (Don't Care)	Conditional	Stop execution of the Message Sequence Control Program until a new BC Start is issued by the host if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list.
Delay	DLY	0008	Delay Time Value (Resolution = 1µS)	Conditional	Delay the time specified by the Time parameter before executing the next OpCode if the condition flag tests TRUE, otherwise continue execution at the next OpCode without delay. The delay generated will use the Time to Next Message Timer.
Wait Until Frame Timer = 0	WFT	0009	Not Used (Don't Care)	Conditional	Wait until Frame Time counter is equal to Zero before continuing execution of the Message Sequence Control Program if the condition flag tests TRUE, otherwise continue execution at the next OpCode without delay.
Compare to Frame Timer	CFT	000A	Delay Time Value (Resolution = 100µS / LSB)	Unconditional	Compare Time Value to Frame Time Counter. The LT/GP0 and EQ/GP1 flag bits are set or cleared based on the results of the compare. If the value of the CFT's parameter is less than the value of the frame time counter, then the LT/GP0 and NE/$\overline{GP1}$ flags will be set, while the GT-EQ/$\overline{GP0}$ and EQ/GP1 flags will be cleared. If the value of the CFT's parameter is equal to the value of the frame time counter, then the GT-EQ/$\overline{GP0}$ and EQ/GP1 flags will be set, while the LT/GP0 and NE/$\overline{GP1}$ flags will be cleared. If the value of the CFT's parameter is greater than the current value of the frame time counter, then the GT-EQ/$\overline{GP0}$ and NE/$\overline{GP1}$ flags will be set, while the LT/GP0 and EQ/GP1 flags will be cleared.
Compare to Message Timer	CMT	000B	Delay Time Value (Resolution = 1µS / LSB)	Unconditional	Compare Time Value to Message Time Counter. The LT/GP0 and EQ/GP1 flag bits are set or cleared based on the results of the compare. If the value of the CMT's parameter is less than the value of the message time counter, then the LT/GP0 and NE/$\overline{GP1}$ flags will be set, while the GT-EQ/$\overline{GP0}$ and EQ/GP1 flags will be cleared. If the value of the CMT's parameter is equal to the value of the message time counter, then the GT-EQ/$\overline{GP0}$ and EQ/GP1 flags will be set, while the LT/GP0 and NE/$\overline{GP1}$ flags will be cleared. If the value of the CMT's parameter is greater than the current value of the message time counter, then the GT-EQ/$\overline{GP0}$ and NE/$\overline{GP1}$ flags will be set, while the LT/GP0 and EQ/GP1 flags will be cleared.

NOTE: While the XEQ (Execute Message) instruction is conditional, not all condition codes may be used to enable its use. The ALWAYS and NEVER condition codes may be used. The eight general purpose flag bits, GP0 through GP7, may also be used. However, if GP0 through GP7 are used, it is imperative that the host processor not modify the value of the specific general purpose flag bit that enabled a particular message while that message is being processed. Similarly, the LT, GT-EQ, EQ, and NE flags, which the BC only updates by means of the CFT and CMT instructions, may also be used. However, these two flags are dual use. Therefore, if these are used, it is imperative that the host processor not modify the value of the specific flag (GP0 or GP1) that enabled a particular message while that message is being processed. The NORESP, FMT ERR, GD BLK XFER, MASKED STATUS SET, BAD MESSAGE, RETRY0, and RETRY1 condition codes are not available for use with the XEQ instruction and should not be used to enable its execution.

TABLE 4. BC OPERATIONS FOR MESSAGE SEQUENCE CONTROL (CONT.)

INSTRUCTION	MNEMONIC	OP CODE (HEX)	PARAMETER	CONDITIONAL OR UNCONDITIONAL	DESCRIPTION
GP Flag Bits	FLG	000C	Used to set, clear, or toggle GP (General Purpose) Flag bits (See description)	Unconditional	Used to set, toggle, or clear any or all of the eight general purpose flags. The table below illustrates the use of the GP Flag Bits instruction for the case of GP0 (General Purpose Flag 0). Bits 1 and 9 of the parameter byte affect flag GP1, bits 2 and 10 effect GP2, etc., according to the following rules:
Load Time Tag Counter	LTT	000D	Time Value. Resolution (µs/LSB) is defined by bits 9, 8, and 7 of Configuration Register #2.	Conditional	Load Time Tag Counter with Time Value if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list.
Load Frame TimerLoad Frame	LFT	000E	Time Value (resolution = 100 µs/LSB)	Conditional	Load Frame Timer Register with the Time Value parameter if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list.
Start Frame Timer	SFT	000F	Not Used (Don't Care)	Conditional	Start Frame Time Counter with Time Value in Time Frame register if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list.
Push Time Tag Register	PPT	0010	Not Used (Don't Care)	Conditional	Push the value of the Time Tag Register on the General Purpose Queue if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list.
Push Block Status Word	PBS	0011	Not Used (Don't Care)	Conditional	Push the Block Status Word for the most recent message on the General Purpose Queue if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list.
Push Immediate Value	PSI	0012	Immediate Value	Conditional	Push Immediate data on the General Purpose Queue if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list.
Push Indirect	PSM	0013	Memory Address	Conditional	Push the data stored at the specified memory location on the General Purpose Queue if the condition flag tests TRUE, otherwise continue execution at the next OpCode in the instruction list.
Wait for External Trigger	WTG	0014	Not Used (Don't Care)	Conditional	Wait for a logic "0"-to-logic "1" transition on the EXT_TRIG input signal before proceeding to the next OpCode in the instruction list if the condition flag tests TRUE, otherwise continue execution at the next OpCode without delay.
Execute and Flip	XQF	0015	Message Control / Status Block Address	Unconditional	Execute (unconditionally) the message referenced by the Message Control/Status Block Address. Following the processing of this message, if the condition flag tests TRUE, the BC will toggle bit 4 in the Message Control/Status Block Address, and store the new Message Block Address as the updated value of the parameter following the XQF instruction code. As a result, the **next** time that this line in the instruction list is executed, the Message Control/Status Block at the **updated** address (**old address XOR 0010h**), rather than the old address, will be processed. If the condition flag tests FALSE, the value of the Message Control/Status Block Address parameter will not change.

Bit 8	Bit 0	Effect on GP0
0	0	No Change
0	1	Set Flag
1	0	Clear Flag
1	1	Toggle Flag

TABLE 5. BC CONDITION CODES

BIT CODE	NAME (BIT 4 = 0)	INVERSE (BIT 4 = 1)	FUNCTIONAL DESCRIPTION
0	LT/GP0	GT-EQ/ $\overline{\text{GP0}}$	Less than or GP0 flag. This bit is set or cleared based on the results of the compare. If the value of the CMT's parameter is less than the value of the message time counter, then the LT/GP0 and NE/$\overline{\text{GP1}}$ flags will be set, while the GT-EQ/$\overline{\text{GP0}}$ and EQ/GP1 flags will be cleared. If the value of the CMT's parameter is equal to the value of the message time counter, then the GT-EQ/$\overline{\text{GP0}}$ and EQ/GP1 flags will be set, while the LT/GP0 and NE/$\overline{\text{GP1}}$ flags will be cleared. If the value of the CMT's parameter is greater than the current value of the message time counter, then the GT-EQ/$\overline{\text{GP0}}$ and NE/$\overline{\text{GP1}}$ flags will be set , while the LT/GP0 and EQ/GP1 flags will be cleared. Also, General Purpose Flag 1 may also be set or cleared by a FLG operation.
1	EQ/GP1	NE/$\overline{\text{GP1}}$	Equal Flag. This bit is set or cleared after CFT or CMT operation. If the value of the CMT's parameter is equal to the value of the message time counter, then the EQ/GP1 flag will be set and the NE/$\overline{\text{GP1}}$ bit will be cleared. If the value of the CMT's parameter is not equal to the value of the message time counter, then the NE/$\overline{\text{GP1}}$ flag will be set and the EQ/GP1bit will be cleared. Also, General Purpose Flag 1 may also be set or cleared by a FLG operation.
2 3 4 5 6 7	GP2 GP3 GP4 GP5 GP6 GP7	$\overline{\text{GP2}}$ $\overline{\text{GP3}}$ $\overline{\text{GP4}}$ $\overline{\text{GP5}}$ $\overline{\text{GP6}}$ $\overline{\text{GP7}}$	General Purpose Flags may be set, cleared, or toggled by a FLG operation. The host processor can set, clear, or toggle these flags in the same way as the FLG instruction by means of the BC GENERAL PURPOSE FLAG REGISTER.
8	NORESP	$\overline{\text{RESP}}$	NORESP indicates that an RT has either not responded or has responded later than the BC No Response Timeout time. The Enhanced Mini-ACE's No Response Timeout Time is defined per MIL-STD-1553B as the time from the mid-bit crossing of the parity bit of the last word transmitted by the BC to the mid-sync crossing of the RT Status Word. The value of the No Response Timeout value is programmable from among the nominal values 18.5, 22.5, 50.5, and 130 µs (±1 µs) by means of bits 10 and 9 of Configuration Register #5.
9	FMT ERR	$\overline{\text{FMT ERR}}$	FMT ERR indicates that the received portion of the most recent message contained one or more violations of the 1553 message validation criteria (sync, encoding, parity, bit count, word count, etc.), or the RT's status word received from a responding RT contained an incorrect RT address field.
A	GD BLK XFER	$\overline{\text{GD BLK XFER}}$	For the most recent message, GD BLK XFER will be set to logic "1" following completion of a valid (error-free) RT-to-BC transfer, RT-to-RT transfer, or transmit mode code with data message. This bit is set to logic "0" following an invalid message. GOOD DATA BLOCK TRANSFER is **always** logic "0" following a BC-to-RT transfer, a mode code with data, or a mode code without data. The Loop Test has **no effect** on GOOD DATA BLOCK TRANSFER. GOOD DATA BLOCK TRANSFER may be used to determine if the transmitting portion of an RT-to-RT transfer was error free.
B	MASKED STATUS BIT	$\overline{\text{MASKED STATUS BIT}}$	Indicates that one or both of the following conditions have occurred for the most recent message: (1) If one (or more) of the Status Mask bits (14 through 9) in the BC Control Word is logic "0" **and** the corresponding bit(s) is (are) set (logic "1") in the received RT Status Word. In the case of the RESERVED BITS MASK (bit 9) set to logic "0," any or all of the 3 Reserved Status Word bits being set will result in a MASKED STATUS SET condition; and/or (2) If BROADCAST MASK ENABLED/XOR (bit 11 of Configuration Register #4) is logic "1" **and** the MASK BROADCAST bit of the message's BC Control Word is logic "0" and the BROADCAST COMMAND RECEIVED bit in the received RT Status Word is logic "1".
C	BAD MESSAGE	GOOD MESSAGE	BAD MESSAGE indicates either a format error, loop test fail, or no response error for the most recent message. Note that a "Status Set" condition has **no effect** on the "BAD MESSAGE/GOOD MESSAGE" condition code.
D E	RETRY0 RETRY1	$\overline{\text{RETRY0}}$ $\overline{\text{RETRY1}}$	These two bits reflect the retry status of the most recent message. The number of times that the message was retried is delineated by these two bits as shown below: RETRY COUNT 1 (bit 14) / RETRY COUNT 0 (bit 13) / Number of Message Retries 0 / 0 / 0 0 / 1 / 1 1 / 0 / N/A 1 / 1 / 2
F	ALWAYS	NEVER	The ALWAYS flag should be set (bit 4 = 0) to designate an instruction as unconditional. The NEVER bit (bit 4 = 1) can be used to implement a NOP or “skip” instruction.

The Enhanced Mini-ACE BC message sequence control capability enables a high degree of offloading of the host processor. This includes using the various timing functions to enable autonomous structuring of major and minor frames. In addition, by implementing conditional jumps and subroutine calls, the message sequence control processor greatly simplifies the insertion of asynchronous, or "out-of-band" messages.

EXECUTE AND FLIP OPERATION

The Enhanced Mini-ACE BC's XQF, or "Execute and Flip" operation, provides some unique capabilities. Following execution of this unconditional instruction, if the condition code tests TRUE, the BC will modify the value of the current XQF instruction's pointer parameter by toggling bit 4 in the pointer. That is, if the selected condition flag tests true, the value of the parameter will be updated to the value = old address XOR 0010h. As a result, the next time that this line in the instruction list is executed, the Message Control/Status Block at the updated address (old address XOR 0010h), rather than the one at the old address, will be processed. The operation of the XQF instruction is illustrated in FIGURE 4.

There are multiple ways of utilizing the "execute and flip" functionality. One is to facilitate the implementation of a double buffering data scheme for individual messages. This allows the message sequence control processor to "ping-pong" between a pair of data buffers for a particular message. By so doing, the host processor can access one of the two Data Word blocks, while the BC reads or writes the alternate Data Word block.

A second application of the "execute and flip" capability is in association with message retries. This allows the BC to not only switch buses when retrying a failed message, but to automatically switch buses permanently for all future times that the same message is to be processed. This not only provides a high degree of autonomy from the host CPU, but saves BC bandwidth, by eliminating future attempts to process messages on an RT's failed channel.

GENERAL PURPOSE QUEUE

The Enhanced Mini-ACE BC allows for the creation of a general purpose queue. This data structure provides a means for the message sequence processor to convey information to the BC host. The BC op code repertoire provides mechanisms to push various items on this queue. These include the contents of the Time Tag Register, the Block Status Word for the most recent message, an immediate data value, or the contents of a specified memory address.

FIGURE 5 illustrates the operation of the BC General Purpose Queue. Note that the BC General Purpose Queue Pointer Register will always point to the next address location (modulo 64); that is, the location following the last location written by the BC message sequence control engine.

If enabled, a BC GENERAL PURPOSE QUEUE ROLLOVER interrupt will be issued when the value of the queue pointer address rolls over at a 64-word boundary.

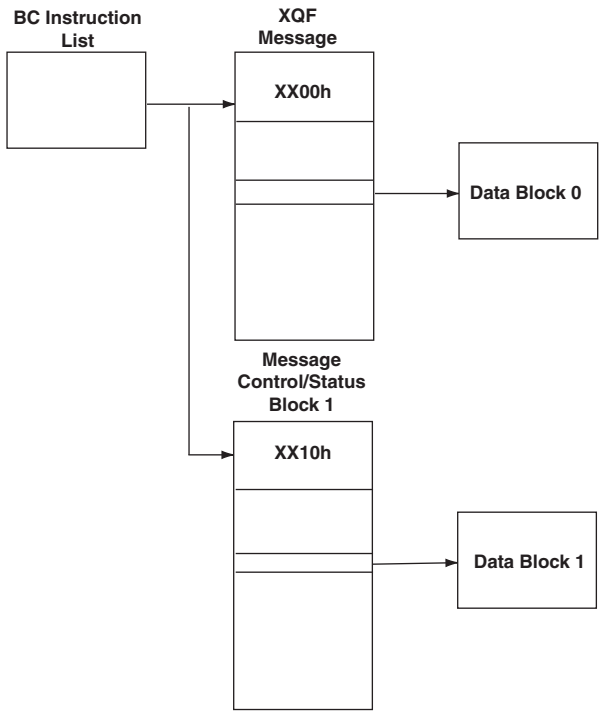


FIGURE 4. EXECUTE AND FLIP (XQF) OPERATION

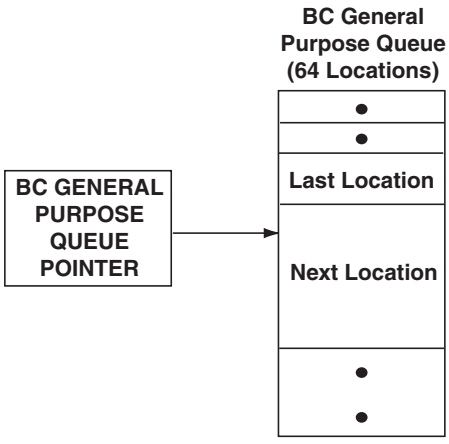


FIGURE 5. BC GENERAL PURPOSE QUEUE

REMOTE TERMINAL (RT) ARCHITECTURE

The Enhanced Mini-ACE RT architecture provides multiprotocol support, with full compliance to all of the commonly used data bus standards, including MIL-STD-1553A, MIL-STD-1553B, Notice 2, STANAG 3838, General Dynamics 16PP303, and McAir A3818, A5232, and A5690. For the Enhanced Mini-ACE RT mode, there is programmable flexibility enabling the RT to be configured to fulfill any set of system requirements. This includes the capability to meet the MIL-STD-1553A response time requirement of 2 to 5 ms, and multiple options for mode code subaddresses, mode codes, RT status word, and RT BIT word.

The Enhanced Mini-ACE RT protocol design implements all of the MIL-STD-1553B message formats and dual redundant mode codes. The design has passed validation testing for MIL-STD-1553B compliance. The Enhanced Mini-ACE RT performs comprehensive error checking, word and format validation, and checks for various RT-to-RT transfer errors. One of the main features of the Enhanced Mini-ACE RT is its choice of memory management options. These include single buffering by subaddress, double buffering for individual receive subaddresses, circular buffering by individual subaddresses, and global circular buffering for multiple (or all) subaddresses.

Other features of the Enhanced Mini-ACE RT include a set of interrupt conditions, an interrupt status queue with filtering based on valid and/or invalid messages, internal command illegalization, programmable busy by subaddress, multiple options on time tagging, and an "auto-boot" feature which allows the RT to initialize as an online RT with the busy bit set following power turn-on.

RT MEMORY MANAGEMENT

The Enhanced Mini-ACE provides a variety of RT memory management capabilities. As with the ACE and Mini-ACE, the choice of memory management scheme is fully programmable on a transmit/receive/broadcast subaddress basis.

In compliance with MIL-STD-1553B Notice 2, received data from broadcast messages may be optionally separated from non-broadcast received data. For each transmit, receive or broadcast subaddress, either a single-message data block, a double buffered configuration (two alternating Data Word blocks), or a variable-sized (128 to 8192 words) subaddress circular buffer may be allocated for data storage. The memory management scheme for individual subaddresses is designated by means of the subaddress control word.

For received data, there is also a global circular buffer mode. In this configuration, the data words received from multiple (or all) subaddresses are stored in a common circular buffer structure. Like the subaddress circular buffer, the size of the global circular buffer is programmable, with a range of 128 to 8192 data words.

The double buffering feature provides a means for the host processor to easily access the most recent, complete received block of valid Data Words for any given subaddress. In addition to helping ensure data sample consistency, the circular buffer options provide a means of greatly reducing host processor overhead for multi-message bulk data transfer applications.

End-of-message interrupts may be enabled either globally (following all messages), following error messages, on a transmit/receive/broadcast subaddress or mode code basis, or

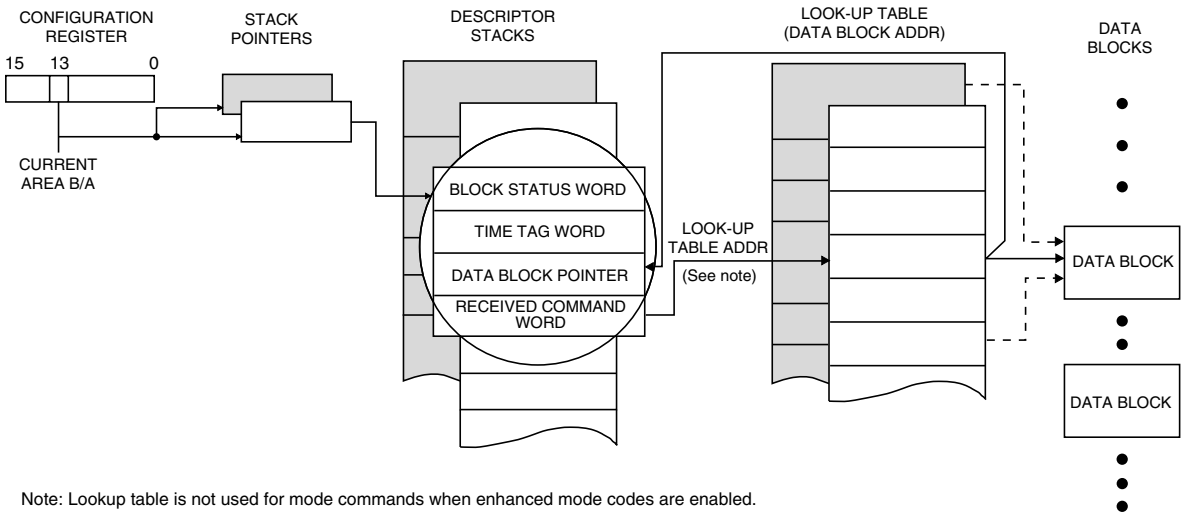


FIGURE 6. RT SINGLE-BUFFERED MODE

when a circular buffer reaches its midpoint (50% boundary) or lower (100%) boundary. A pair of interrupt status registers allow the host processor to determine the cause of all interrupts by means of a single read operation.

SINGLE-BUFFERED MODE

The operation of the single buffered RT mode is illustrated in FIGURE 6. In the single-buffered mode the respective lookup table entry must be written by the host processor. Received data words are written to, or transmitted data words are read from the data word block with starting address referenced by the lookup table pointer. In the single-buffered mode, the current lookup table pointer is not updated by the Enhanced Mini-ACE memory management logic. Therefore, if a subsequent message is received for the same subaddress, the same Data Word block will be overwritten or overread.

SUBADDRESS DOUBLE-BUFFERING MODE

The Enhanced Mini-ACE provides a double-buffering mechanism for received data that may be selected on an individual subaddress basis for any and all receive (and/or broadcast) subaddresses. This is illustrated in FIGURE 7. It should be noted that the Subaddress Double Buffering mode is applicable for receive data only, not for transmit data. Double buffering of transmit messages may be easily implemented by software techniques.

The purpose of the subaddress double buffering-mode is to provide data sample consistency to the host processor. This is accomplished by allocating two 32-word data word blocks for each individual receive (and/or broadcast receive) subaddress. At any given time, one of the blocks will be designated as the "active" 1553 block while the other will be considered as "inactive". The data words for the next receive command to that subaddress will be stored in the active block. Following receipt of a valid message, the Enhanced Mini-ACE will automatically switch the active and inactive blocks for that subaddress. As a result, the latest, valid, complete data block is always accessible to the host processor.

CIRCULAR BUFFER MODE

The operation of the Enhanced Mini-ACE's circular buffer RT memory management mode is illustrated in FIGURE 8. As in the single buffered and double-buffered modes, the individual lookup table entries are initially loaded by the host processor. At the start of each message, the lookup table entry is stored in the third position of the respective message block descriptor in the descriptor stack area of RAM. Receive or transmit data words are transferred to (from) the circular buffer, starting at the location referenced by the lookup table pointer.

In general, the location after the last data word written or read (modulo the circular buffer size) during the message is written to the respective lookup table location during the end-of-message sequence. By so doing, data for the next message for the respective transmit, receive(/broadcast), or broadcast subaddress will be accessed from the next lower contiguous block of locations in the circular buffer.

For the case of a receive (or broadcast receive) message with a data word error, there is an option such that the lookup table pointer will only be updated following receipt of a valid message. That is, the pointer will not be updated following receipt of a message with an error in a data word. This allows failed messages in a bulk data transfer to be retried without disrupting the circular buffer data structure, and without intervention by the RT's host processor.

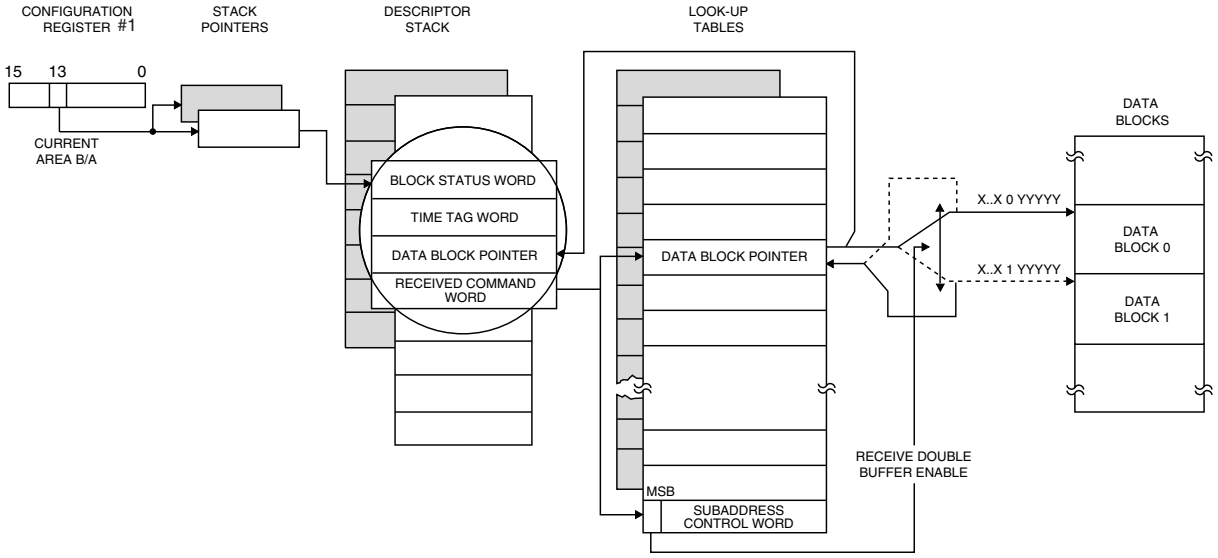


FIGURE 7. RT DOUBLE-BUFFERED MODE

GLOBAL CIRCULAR BUFFER

Beyond the programmable choice of single buffer mode, double buffer mode, or circular buffer mode, programmable on an individual subaddress basis, the Enhanced Mini-ACE RT architecture provides an additional option, a variable sized global circular buffer. The Enhanced Mini-ACE RT allows for a mix of single buffered, double buffered, and individually circular buffered subaddresses, along with the use of the global double buffer for any arbitrary group of receive(/broadcast) or broadcast subaddresses.

In the global circular buffer mode, the data for multiple receive subaddresses is stored in the same circular buffer data structure. The size of the global circular buffer may be programmed for 128, 256, 512, 1024, 2048, 4096, or 8192 words, by means of Configuration Register #6. Individual subaddresses may be mapped to the global circular buffer by means of their respective subaddress control words.

The pointer to the Global Circular Buffer is stored in location 0101 (for Area A), or location 0105 (for Area B).

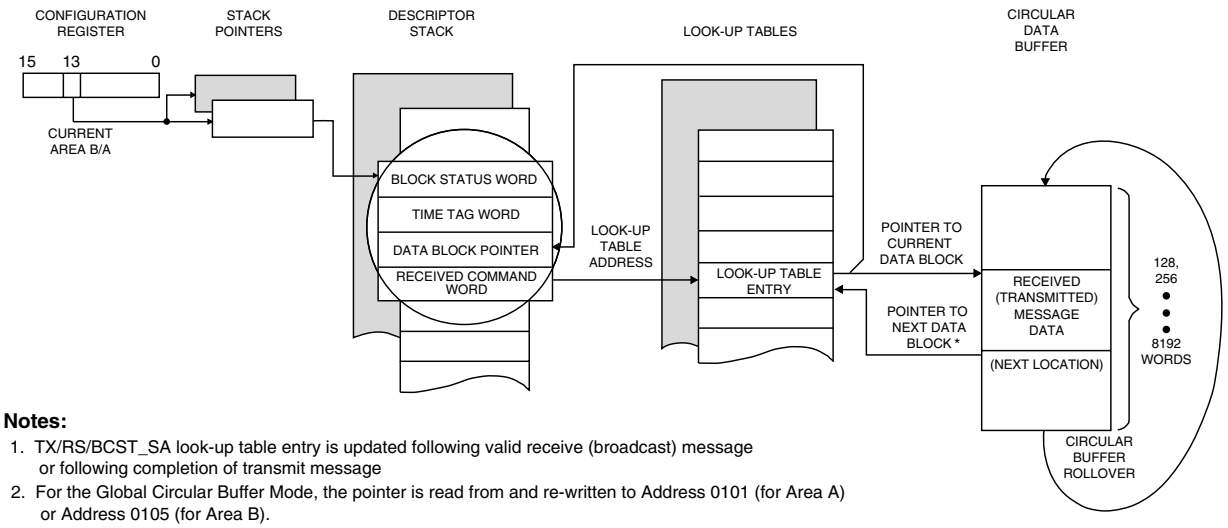
The global circular buffer option provides a highly efficient method for storing received message data. It allows for frequently used subaddresses to be mapped to individual data blocks, while also providing a method for asynchronously received messages to infrequently used subaddresses to be logged to a common area. Alternatively, the global circular buffer provides an efficient means for storing the received data words for all subaddresses. Under this method, all received data words are stored chronologically, regardless of subaddress.

RT DESCRIPTOR STACK

The descriptor stack provides a chronology of all messages processed by the Enhanced Mini-ACE RT. Reference FIGURE 6, FIGURE 7, and FIGURE 8. Similar to BC mode, there is a four-word block descriptor in the Stack for each message processed. The four entries to each block descriptor are the Block Status Word, Time Tag Word, the pointer to the start of the message's data block, and the 16-bit received Command Word.

The RT Block Status Word includes indications of whether a particular message is ongoing or has been completed, what bus channel it was received on, indications of illegal commands, and flags denoting various message error conditions. For the double buffering, subaddress circular buffering, and global circular buffering modes, the data block pointer may be used for locating the data blocks for specific messages. Note that for mode code commands, there is an option to store the transmitted or received data word as the third word of the descriptor, in place of the data block pointer.

The Time Tag Word provides a 16-bit indication of relative time for individual messages. The resolution of the Enhanced Mini-ACE's time tag is programmable from among 2, 4, 8, 16, 32, or 64 µs/LSB. There is also a provision for using an external clock input for the time tag (consult factory). If enabled, there is a time tag rollover interrupt, which is issued when the value of the time tag rolls over from FFFF(hex) to 0. Other time tag options include the capabilities to clear the time tag register following receipt of a Synchronize (without data) mode command and/or to set the time tag following receipt of a Synchronize (with data) mode command. For the latter, there is an added option to filter the "set" capability based on the LSB of the received data word being equal to logic "0".



Notes:

1. TX/RS/BCST_SA look-up table entry is updated following valid receive (broadcast) message or following completion of transmit message
2. For the Global Circular Buffer Mode, the pointer is read from and re-written to Address 0101 (for Area A) or Address 0105 (for Area B).

FIGURE 8. RT CIRCULAR-BUFFERED MODE

RT INTERRUPTS

The Enhanced Mini-ACE offers a great deal of flexibility in terms of RT interrupt processing. By means of the Enhanced Mini-ACE's two Interrupt Mask Registers, the RT may be programmed to issue interrupt requests for the following events/conditions: End-of-(every)Message, Message Error, Selected (transmit or receive) Subaddress, 100% Circular Buffer Rollover, 50% Circular Buffer Rollover, 100% Descriptor Stack Rollover, 50% Descriptor Stack Rollover, Selected Mode Code, Transmitter Timeout, Illegal Command, and Interrupt Status Queue Rollover.

INTERRUPT FOR 50% ROLLOVERS OF STACKS, CIRCULAR BUFFERS

The Enhanced Mini-ACE RT and Monitor are capable of issuing host interrupts when a subaddress circular buffer pointer or stack pointer crosses its mid-point boundary. For RT circular buffers, this is applicable for both transmit and receive subaddresses. Reference FIGURE 9. There are four interrupt mask and interrupt status register bits associated with the 50% rollover function: (1) RT circular buffer; (2) RT command (descriptor) stack; (3) Monitor command (descriptor) stack; and (4) Monitor data stack.

The 50% rollover interrupt is beneficial for performing bulk data transfers. For example, when using circular buffering for a particular receive subaddress, the 50% rollover interrupt will inform the host processor when the circular buffer is half full. At that time, the host may proceed to read the received data words in the upper half of the buffer, while the Enhanced Mini-ACE RT writes received data words to the lower half of the circular buffer. Later, when the RT issues a 100% circular buffer rollover interrupt, the host can proceed to read the received data from the lower half of the buffer, while the Enhanced Mini-ACE RT continues to write received data words to the upper half of the buffer.

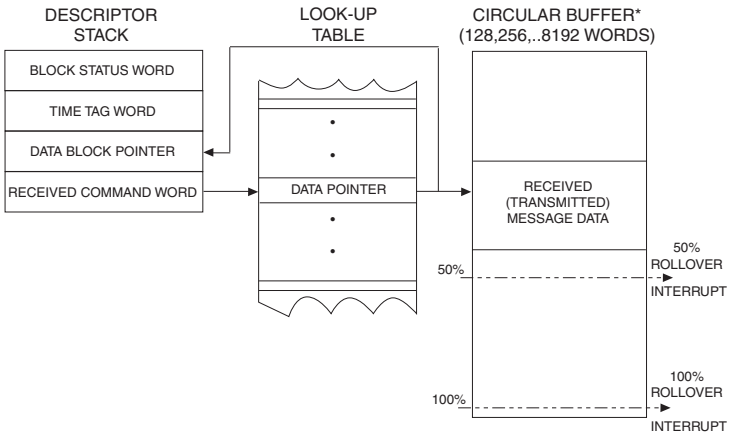
INTERRUPT STATUS QUEUE

The Enhanced Mini-ACE RT, Monitor, and combined RT/Monitor modes include the capability for generating an interrupt status queue. As illustrated in FIGURE 10, this provides a chronological history of interrupt generating events and conditions. In addition to the Interrupt Mask Register, the Interrupt Status Queue provides additional filtering capability such that only valid messages and/or only invalid messages may result in the creation of an entry to the Interrupt Status Queue. The pointer to the Interrupt Status Queue is stored in the INTERRUPT VECTOR QUEUE POINTER REGISTER (register address 1F). This register must be initialized by the host, and is subsequently incremented by the RT message processor. The interrupt status queue is 64 words deep, providing the capability to store entries for up to 32 messages.

The queue rolls over at addresses of modulo 64. The events that result in queue entries include both message-related and non-message related events. Note that the Interrupt Vector Queue Pointer Register will always point to the next location (modulo 64) following the last vector/pointer pair written by the Enhanced Mini-ACE RT, Monitor, or RT/Monitor.

Each event that causes an interrupt results in a two-word entry to be written to the queue. The first word of the entry is the interrupt vector. The vector indicates which interrupt event(s)/condition(s) caused the interrupt.

The interrupt events are classified into two categories: message interrupt events and non-message interrupt events. Message-based interrupt events include End-of-Message, Selected mode code, Format error, Subaddress control word interrupt, RT Circular buffer Rollover, Handshake failure, RT Command stack



Note: This figure is for an RT Subaddress Circular Buffer. The 50% and 100% Rollover Interrupts are also applicable to the RT Global Circular Buffer, RT Command Stack, Monitor Stack and Monitor Data Stack.

FIGURE 9. 50% AND 100% ROLLOVER INTERRUPTS

rollover, transmitter timeout, and RT Circular buffer 50% rollover. Non-message interrupt events/conditions include Time tag rollover, RT address parity error, MT data stack rollover, MT command stack rollover, RAM parity error, RT Command stack 50% rollover, MT data stack 50% rollover, MT command stack 50% rollover, and BIT completed.

Bit 0 of the interrupt vector (interrupt status) word indicates whether the entry is for a message interrupt event (if bit 0 is logic "1") or a non-message interrupt event (if bit 0 is logic "0"). It is not possible for one entry on the queue to indicate both a message interrupt and a non-message interrupt.

As illustrated in FIGURE 10, for a message interrupt event, the parameter word is a pointer. The pointer will reference the first word of the RT or MT command stack descriptor (i.e., the Block Status Word).

For a RAM Parity Error non-message interrupt, the parameter will be the RAM address where the parity check failed. For the RT address Parity Error and Protocol Self-test Complete non-message interrupts, the parameter is not used; it will have a value of 0000. For a Time Tag Rollover non-message interrupt, the parameter will be a pointer to the descriptor stack.

If enabled, an INTERRUPT STATUS QUEUE ROLLOVER interrupt will be issued when the value of the queue pointer address rolls over at a 64-word address boundary.

RT COMMAND ILLEGALIZATION

The Enhanced Mini-ACE provides an internal mechanism for RT Command Word illegalizing. By means of a 256-word area in shared RAM, the host processor may designate that any message be illegalized, based on the command word T/R bit, subaddress, and word count/mode code fields. The Enhanced Mini-ACE illegalization scheme provides the maximum in flexibility, allowing any subset of the 4096 possible combinations of broadcast/own address, T/$\overline{R}$ bit, subaddress, and word count/mode code to be illegalized.

BUSY BIT

The Enhanced Mini-ACE RT provides two different methods for setting the Busy status word bit: (1) globally, by means of Configuration Register #1; or (2) on a T/R-bit/subaddress basis, by means of a RAM lookup table. If the host CPU asserts the BUSY bit low in Configuration Register #1, the Enhanced Mini-ACE RT will respond to all non-broadcast commands with the Busy bit set in its RT Status Word.

Alternatively, there is a Busy lookup table in the Enhanced Mini-ACE shared RAM. By means of this table it is possible for the host processor to set the busy bit for any selectable subset of the 64 combinations of T/R bit and subaddress, and for transmit broadcast mode commands. If the busy bit is set for a transmit command, the Enhanced Mini-ACE RT will respond with the busy bit set in the status word, but will not transmit any data words. If the busy bit is set for a receive command, the RT will also respond with the busy status bit set. There are two programmable options regarding the reception of data words for a non-mode code receive command for which the RT is busy: (1) to transfer the received data words to shared RAM; or (2) to not transfer the data words to shared RAM.

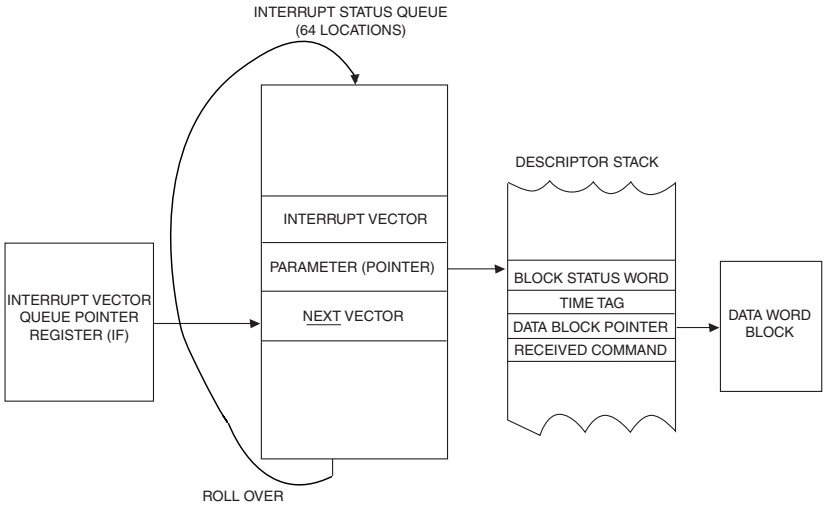


FIGURE 10. RT (AND MONITOR) INTERRUPT STATUS QUEUE (SHOWN FOR MESSAGE INTERRUPT EVENT)

TABLE 6. RT BIT WORD	
BIT	**DESCRIPTION**
15 (MSB)	Transmitter Timeout
14	Loop Test Failure B
13	Loop Test Failure A
12	Handshake Failure
11	Transmitter Shutdown B
10	Transmitter Shutdown A
9	Terminal Flag Inhibited
8	Bit Test Fail
7	High Word Count
6	Low Word Count
5	Incorrect Sync Received
4	Parity/Manchester Error Received
3	RT-RT Gap/Sync/Address Error
2	RT-RT No Response Error
1	Command Word Contents Error
0 (LSB)	Data 0

RT ADDRESS

The design of the BU-65568 supports two options for specifying the RT addresses for the individual Enhanced Mini-ACE's: (1) by means of the RT ADDRESS (and PARITY) inputs, that are brought out to the card's J4 connector, and latched externally; or (2) using the fully software programmable option by the PC/104 host, by means of an internal register. In both configurations, the RT address is readable by the host processor.

RT BUILT-IN TEST (BIT) WORD

The bit map for the Enhanced Mini-ACE's internal RT Built-in-Test (BIT) Word is indicated in TABLE 6.

RT AUTO-BOOT

The BU-65567 RT-only version of the card includes a user jumper option for RT AUTO-BOOT. If this option is exercised, the BU-61745 will initialize to RT mode with the busy status word bit set. AUTO-BOOT is selectable on an individual per-channel basis.

If this option is not exercised, the BU-61745 will initialize to Idle mode. In Idle mode, the BU-61745 is not an online RT; that is, it will not receive messages from the BC or respond on the 1553 bus. In this instance, it will require processor intervention (as a minimum, writing to Configuration Register #1) in order to put the BU-61745 online as an RT.

OTHER RT FEATURES

The Enhanced Mini-ACE includes options for the Terminal flag status word bit to be set either under software control and/or automatically following a failure of the loopback self-test. Other software programmable RT options include software programmable RT status and RT BIT words, automatic clearing of the Service Request bit following receipt of a Transmit vector word mode command, options regarding Data Word transfers for the Busy and Message error (illegal) Status word bits, and options for the handling of 1553A and reserved mode codes.

MONITOR ARCHITECTURE

The Enhanced Mini-ACE includes three monitor modes:

1) A Word Monitor mode

2) A selective message monitor mode

3) A combined RT/message monitor mode

For new applications, it is recommended that the selective message monitor mode be used, rather than the word monitor mode. Besides providing monitor filtering based on RT address, T/R bit, and subaddress, the message monitor eliminates the need to determine the start and end of messages by software.

WORD MONITOR MODE

In the Word Monitor Terminal mode, the Enhanced Mini-ACE monitors both 1553 buses. After the software initialization and Monitor Start sequences, the Enhanced Mini-ACE stores all Command, Status, and Data Words received from both buses. For each word received from either bus, a pair of words is stored to the Enhanced Mini-ACE's shared RAM. The first word is the word received from the 1553 bus. The second word is the Monitor Identification (ID), or "Tag" word. The ID word contains information relating to bus channel, word validity, and inter-word time gaps. The data and ID words are stored in a circular buffer in the shared RAM address space.

SELECTIVE MESSAGE MONITOR MODE

The Enhanced Mini-ACE Selective Message Monitor provides monitoring of 1553 messages with filtering based on RT address, T/R bit, and subaddress with no host processor intervention. By autonomously distinguishing between 1553 command and status words, the Message Monitor determines when messages begin and end, and stores the messages into RAM, based on a programmable filter (RT address, T/R bit, and subaddress).

The selective monitor may be configured as just a monitor, or as a combined RT/Monitor. In the combined RT/Monitor mode, the Enhanced Mini-ACE functions as an RT for one RT address (including broadcast messages), and as a selective message monitor for the other 30 RT addresses. The Enhanced Mini-ACE Message Monitor contains two stacks, a command stack and a data stack, that are independent from the BC/RT command stack. The pointers for these stacks are located at fixed locations in the RAM.

MONITOR SELECTION FUNCTION

Following receipt of a valid command word in Selective Monitor mode, the Enhanced Mini-ACE will reference the selective monitor lookup table to determine if this particular command is enabled. The address for this location is determined by means of an offset based on the RT Address, T/$\overline{R}$ bit, and Subaddress bit 4 of the current command word, and concatenating it to the monitor lookup table base address of 0500-0501 (hex). The bit location within this word is determined by subaddress bits 3-0 of the current command word.

If the specified bit in the lookup table is logic "0", the command is not enabled, and the Enhanced Mini-ACE will ignore this command. If this bit is logic "1", the command is enabled and the Enhanced Mini-ACE will create an entry in the monitor command descriptor stack (based on the monitor command stack pointer), and store the data and status words associated with the command into sequential locations in the monitor data stack. In addition, for an RT-to-RT transfer in which the receive command is selected, the second command word (the transmit command) is stored in the monitor data stack.

SELECTIVE MESSAGE MONITOR MEMORY ORGANIZATION

FIGURE 11 illustrates the Selective Message Monitor operation. Upon receipt of a valid Command Word, the Enhanced Mini-ACE will reference the Selective Monitor Lookup Table to determine if the current command is enabled. If the current command is disabled, the Enhanced Mini-ACE monitor will ignore (and not store) the current message. If the command is enabled, the monitor will create an entry in the Monitor Command Stack at the address location referenced by the Monitor Command Stack Pointer, and an entry in the monitor data stack starting at the location referenced by the monitor data stack pointer.

The format of the information in the data stack depends on the format of the message that was processed. For example, for a BC-to-RT transfer (receive command) the monitor will store the command word in the monitor command descriptor stack, with the data words and the receiving RT's status word stored in the monitor command stack.

The size of the monitor command stack is programmable, with choices of 256, 1K, 4K, or 16K words. The monitor data stack size is programmable with choices of 512, 1K, 2K, 4K, 8K, 16K, 32K or 64K words.

MONITOR INTERRUPTS

Selective monitor interrupts may be issued for End-of-message and for conditions relating to the monitor command stack pointer and monitor data stack pointer. The latter, which are shown in FIGURE 9, include Command Stack 50% Rollover, Command Stack 100% Rollover, Data Stack 50% Rollover, and Data Stack 100% Rollover.

The 50% rollover interrupts may be used to inform the host processor when the command stack or data stack is half full. At that time, the host may proceed to read the received messages in the upper half of the respective stack, while the Enhanced Mini-ACE monitor writes messages to the lower half of the stack. Later, when the monitor issues a 100% stack rollover interrupt, the host can proceed to read the received data from the lower half of the stack, while the Enhanced Mini-ACE monitor continues to write received data words to the upper half of the stack.

INTERRUPT STATUS QUEUE

Like the Enhanced Mini-ACE RT, the Selective Monitor mode includes the capability for generating an interrupt status queue. As illustrated in FIGURE 10, this provides a chronological history of interrupt generating events. Besides the two Interrupt Mask Registers, the Interrupt Status Queue provides additional filtering capability, such that only valid messages and/or only invalid messages may result in entries to the Interrupt Status Queue. The interrupt status queue is 64 words deep, providing the capability to store entries for up to 32 monitored messages.

TIME TAG

The Enhanced Mini-ACE includes an internal read/writable Time Tag Register. This register is a CPU read/writable 16-bit counter with a programmable resolution of either 2, 4, 8, 16, 32, or 64 µs per LSB. Another option allows software controlled incrementing of the Time Tag Register. This supports self-test for the Time Tag Register. For each message processed, the value of the Time Tag Register is loaded into the second location of the respective descriptor stack entry ("TIME TAG WORD") for both the BC and RT mode.

The functionality involving the Time Tag Register that's compatible with ACE/Mini-ACE (Plus) includes: the capability to issue an interrupt request and set a bit in the Interrupt Status Register when the Time Tag Register rolls over FFFF to 0000; for RT mode, the capability to automatically clear the Time Tag Register following reception of a Synchronize (without data) mode command, or to load the Time Tag Register following a Synchronize (with data) mode command.

Additional time tag features supported by the Enhanced Mini-ACE include the capability for the BC to transmit the contents of the Time Tag Register as the data word for a Synchronize (with data) mode command; the capability for the RT to "filter" the data word for the Synchronize with data mode command, by only loading the Time Tag Register if the LSB of the received data word is "0"; an instruction enabling the BC Message Sequence Control engine to autonomously load the Time Tag Register; and an instruction enabling the BC Message Sequence Control engine to write the value of the Time Tag Register to the General Purpose Queue.

INTERRUPTS

The Enhanced Mini-ACE series components provide many programmable options for interrupt generation and handling. Individual interrupts are enabled by the two Interrupt Mask Registers (#1 or #2). The host processor may easily determine the cause of the interrupt by using the Interrupt Status Register (#1 or #2). The two Interrupt Status Registers (#1 and #2) provide the current state of the interrupt conditions. The Interrupt Status Registers may be updated in two ways. In the one interrupt handling mode, a particular bit in the Interrupt Status Register (#1 or #2) will be updated only if the event occurs and the corresponding bit in the Interrupt Mask Register (#1 or #2) is enabled. In the Enhanced interrupt handling mode, a particular bit in the Interrupt Status Register (#1 or #2) will be updated if the condition exists regardless of the contents of the corresponding Interrupt Mask Register bit. In any case, the respective Interrupt Mask Register (#1 or #2) bit enables an interrupt for a particular condition.

The Enhanced Mini-ACE supports all the interrupt events from ACE/Mini-ACE (Plus), including RAM Parity Error, Transmitter Timeout, BC/RT Command Stack Rollover, MT Command Stack and Data Stack Rollover, Handshake Error, BC Retry, RT Address Parity Error, Time Tag Rollover, RT Circular Buffer Rollover, BC Message, RT Subaddress, BC End-of-Frame, Format Error, BC Status Set, RT Mode Code, MT Trigger, and End-of-Message.

In the Enhanced Mini-ACE's Enhanced BC mode, there are four user-defined interrupt bits. The BC Message Sequence Control Engine includes an instruction enabling it to issue these interrupts at any time.

For RT and Monitor modes, the Enhanced Mini-ACE architecture includes an Interrupt Status Queue. This provides a mechanism for logging messages that result in interrupt requests. Entries to the Interrupt Status Queue may be filtered such that only valid and/or invalid messages result in entries on the queue.

The Enhanced Mini-ACE incorporates additional interrupt conditions beyond ACE/Mini-ACE (Plus), based on the addition of Interrupt Mask Register #2 and Interrupt Status Register #2. This is accomplished by chaining of the two Interrupt Status Registers (#1 and #2) using one of the bits in Interrupt Status Register #2 to indicate an interrupt has occurred in Interrupt Status Register #1. Additional interrupts include "Self Test Completed", masking bits for the Advanced BC Control Interrupts, 50% Rollover interrupts for RT Command Stack, RT Circular Buffers, MT Command Stack, and MT Data Stack; BC Op Code Parity Error, (RT) Illegal Command, (BC) General Purpose Queue or (RT/MT) Interrupt Status Queue Rollover, Call Stack Pointer Register Error, BC Trap Op Code, and four User-Defined interrupts for the Enhanced BC mode.

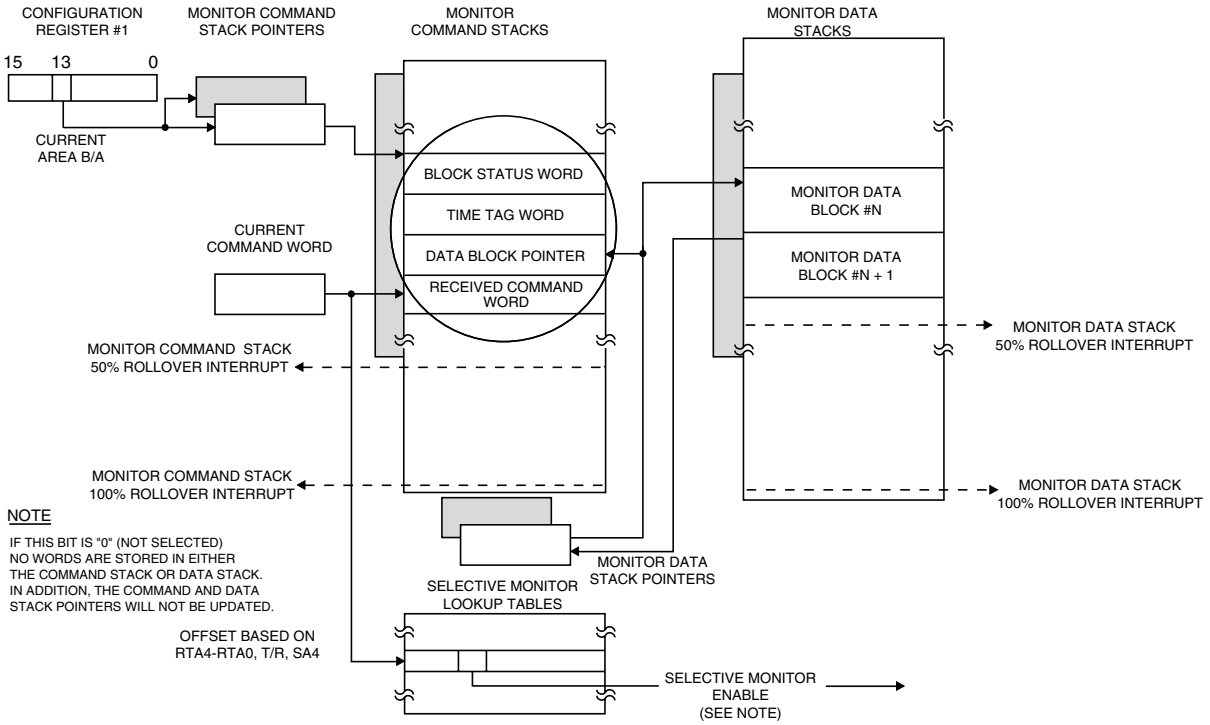


FIGURE 11. SELECTIVE MESSAGE MONITOR MEMORY MANAGEMENT

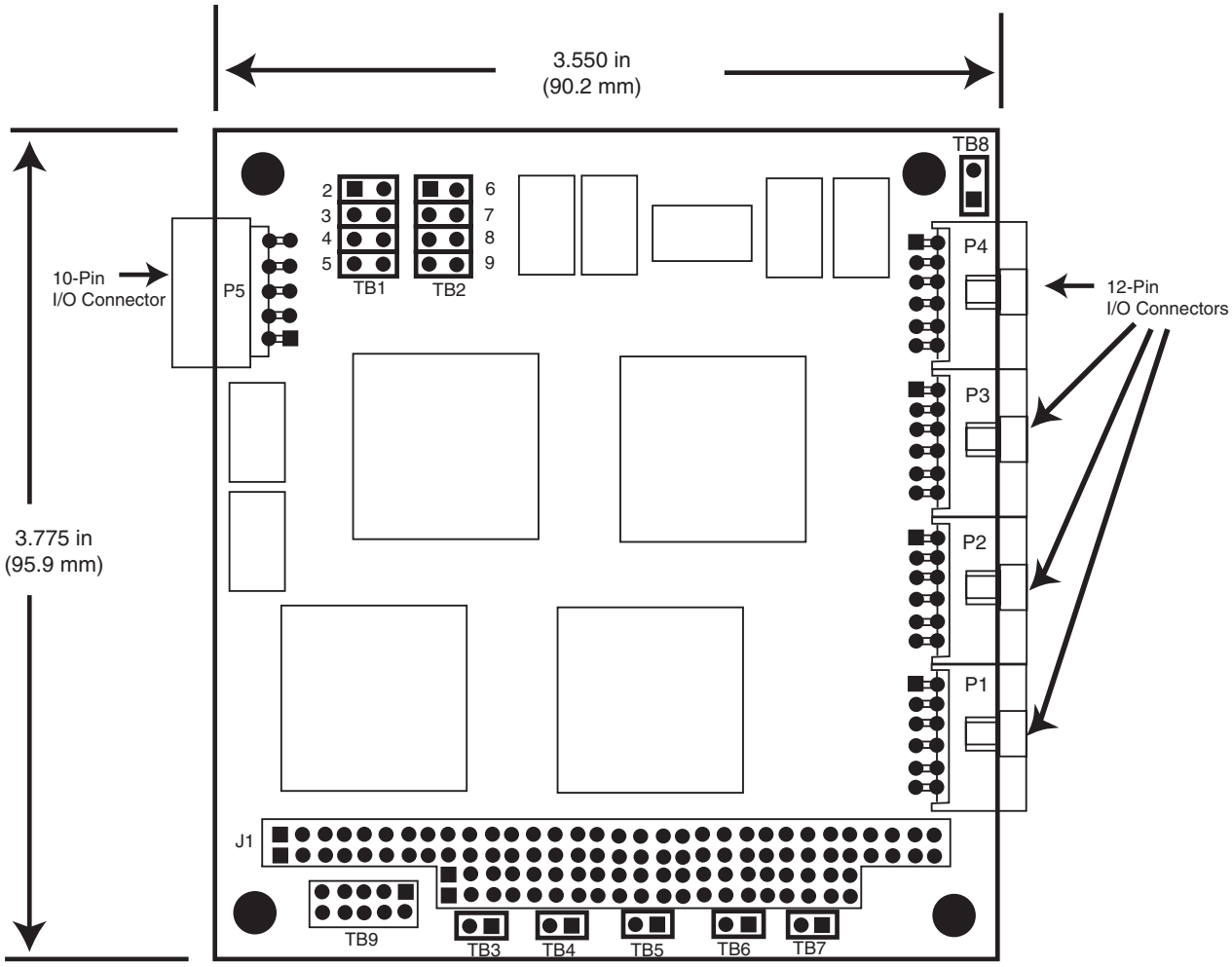
TABLE 7. I/O CONNECTOR P1 CHANNEL 1 PINOUTS	
PIN	FUNCTION
1	BUS1B+
2	BUS1B -
3	BUS1A+
4	BUS1A -
5	Ground
6	BUS1-EXT-TRIG
7	BIA1-RTADP
8	BIA1-RTAD0
9	BIA1-RTAD1
10	BIA1-RTAD2
11	BIA1-RTAD3
12	BIA1-RTAD4

TABLE 8. I/O CONNECTOR P2 CHANNEL 2 PINOUTS	
PIN	FUNCTION
1	BUS2B+
2	BUS2B -
3	BUS2A+
4	BUS2A -
5	Ground
6	BUS2-EXT-TRIG
7	BIA2-RTADP
8	BIA2-RTAD0
9	BIA2-RTAD1
10	BIA2-RTAD2
11	BIA2-RTAD3
12	BIA2-RTAD4

TABLE 9. I/O CONNECTOR P3 CHANNEL 3 PINOUTS	
PIN	FUNCTION
1	BUS3B+
2	BUS3B -
3	BUS3A+
4	BUS3A -
5	Ground
6	BUS3-EXT-TRIG
7	BIA3-RTADP
8	BIA3-RTAD0
9	BIA3-RTAD1
10	BIA3-RTAD2
11	BIA3-RTAD3
12	BIA3-RTAD4

TABLE 10. I/O CONNECTOR P4 CHANNEL 4 PINOUTS	
PIN	FUNCTION
1	BUS4B+
2	BUS4B -
3	BUS4A+
4	BUS4A -
5	Ground
6	BUS4-EXT-TRIG
7	BIA4-RTADP
8	BIA4-RTAD0
9	BIA4-RTAD1
10	BIA4-RTAD2
11	BIA4-RTAD3
12	BIA4-RTAD4

TABLE 11. I/O CONNECTOR P5 DISCRETE PINOUTS	
PIN	FUNCTION
1	DIO0
2	DIO1
3	DIO2
4	DIO3
5	Ground
6	Ground
7	DIO4
8	DIO5
9	DIO6
10	DIO7



Note: Standoffs are in contact with the cards Thermal Plane. The Thermal Plane may optionally be grounded via TB8.

FIGURE 12. BU-65568 OUTLINE DRAWING

ORDERING INFORMATION

BU-65568 C X-X00X

(blank) = No Conformal Coating
N = Conformal Coating

Operating Temperature Range:
3 = 0 to +55°C (BU-65567/8CX-300)
2 = -40 to +85°C (BU-65567/8CX-200)
9 = -55 to +85°C (BU-65567/8CX-900)

Number Of Channels
1 = One Dual Redundant 1553 Channel
2 = Two Dual Redundant 1553 Channels
3 = Three Dual Redundant 1553 Channels
4 = Four Dual Redundant 1553 Channels

Card Type
C = PC/104

Base Product
BU-65567 = MIL-STD-1553 RT-only PC/104 card, with 4K X 17 RAM per channel. Contact Factory for availability.
BU-65568 = MIL-STD-1553 BC/RT/MT PC/104 card, with 64K X 17 RAM per channel.

Note: 1) The above products contain tin-lead solder.

STANDARD DDC PROCESSING FOR DISCRETE MODULES/PC BOARD ASSEMBLIES		
TEST	**METHOD(S)**	**CONDITION(S)**
INSPECTION / WORKMANSHIP	IPC-A-610	Class 3
ELECTRICAL TEST	DDC ATP	—

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Ireland - Tel: +353-21-341065, Fax: +353-21-341568
France - Tel: +33-(0)1-41-16-3424, Fax: +33-(0)1-41-16-3425
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