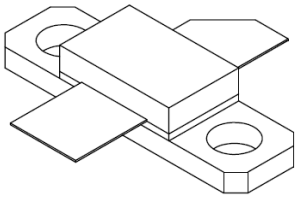
0912LD20

20 Watts, 28 Volts
Pulsed Avionics 960 to 1215 MHz
LDMOS FET

GENERAL DESCRIPTION

The 0912LD20 is a COMMON SOURCE N-Channel enhancement mode lateral MOSFET capable of providing $20W_{pk}$ of RF power from 960 to 1215 MHz. The device is nitride passivated and utilizes gold metallization to ensure highest MTTF. The transistor includes input and output prematch for broadband capability. Low thermal resistance package reduces junction temperature, extends life.

CASE OUTLINE
55QT
(Common Source)



ABSOLUTE MAXIMUM RATINGS

Power Dissipation

Device Dissipation @25°C (P_d)	60 W

Voltage and Current

Drain-Source (V_{DSS})	35V
Gate-Source (V_{GS}, V_{DS}=0)	20V

Temperatures

Storage Temperature	-40 to +150°C
Operating Case Temperature	+100°C

ELECTRICAL CHARACTERISTICS @ 25°C

SYMBOL	CHARACTERISTICS	TEST CONDITIONS	MIN	TYP	MAX	UNITS
BV_{dss}	Drain-Source Breakdown	V_{gs} = 0V, I_d = 1mA	65			V
I_{dss}	Drain-Source Leakage Current	V_{ds} = 28V, V_{gs}= 0V			50	µA
I_{gss}	Gate-Source Leakage Current	V_{gs} = 10V, V_{ds} = 0V			1	µA
$V_{gs(th)}$	Gate Threshold Voltage	V_{ds} = 10V, I_d = 3mA	3		5	V
$V_{ds(on)}$	Drain-Source On Voltage	V_{gs} = 10V, I_d = 250mA			0.23	V
g_{FS}	Forward Transconductance	V_{ds} = 10V, I_d = 125mA		590		mA/V
θ_{JC}[1]	Thermal Resistance			0.3		ºC/W

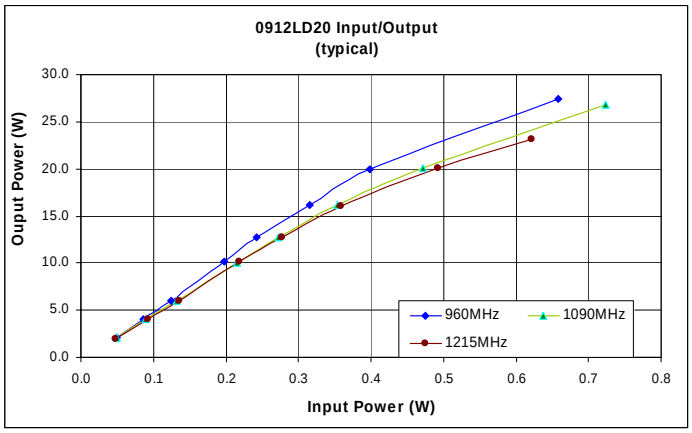
FUNCTIONAL CHARACTERISTICS @ 25°C, Vds = 28V, I_{dq} = 80mA

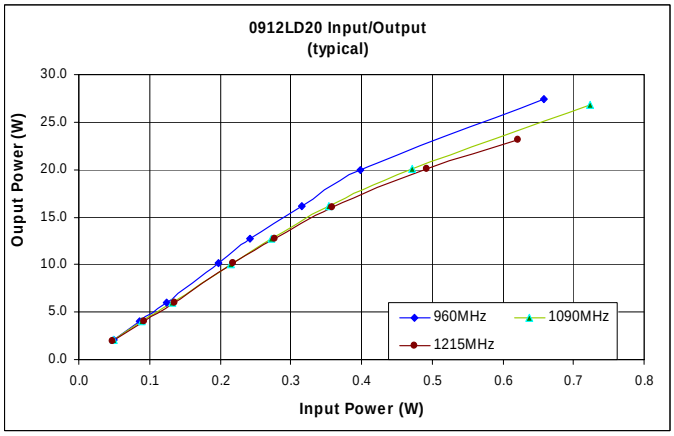
G_{PS}	Common Source Power Gain	Pulse width = 32µs, LTDC=2%	14	15		dB
Pd	Pulse Droop	F=960/1215 MHz, P_{out} = 20W			0.5	dB
η_d	Drain Efficiency	F = 960 MHz, P_{out} = 20W	40	42		%
ψ	Load Mismatch	F = 1090 MHz, P_{out} = 20W			5:1	

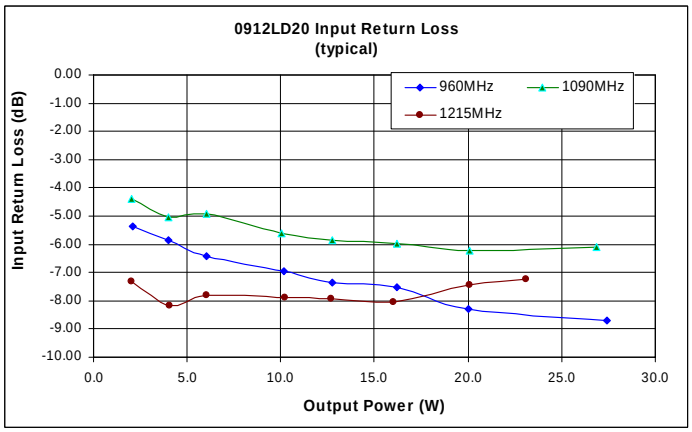
NOTES: 1. At rated output power and pulse conditions
2. Pulse Format 1: 32µs, 2% Long Term Duty Factor

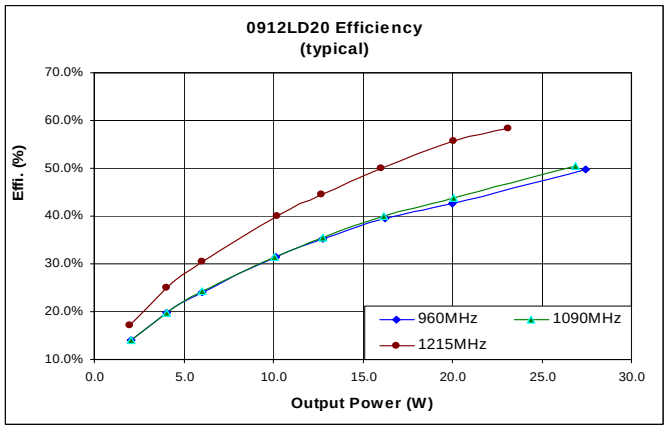
Rev. A - May 2008

PW = 32us, DC=2%: Typical Data









Mode-S Pulse Format Typical Data

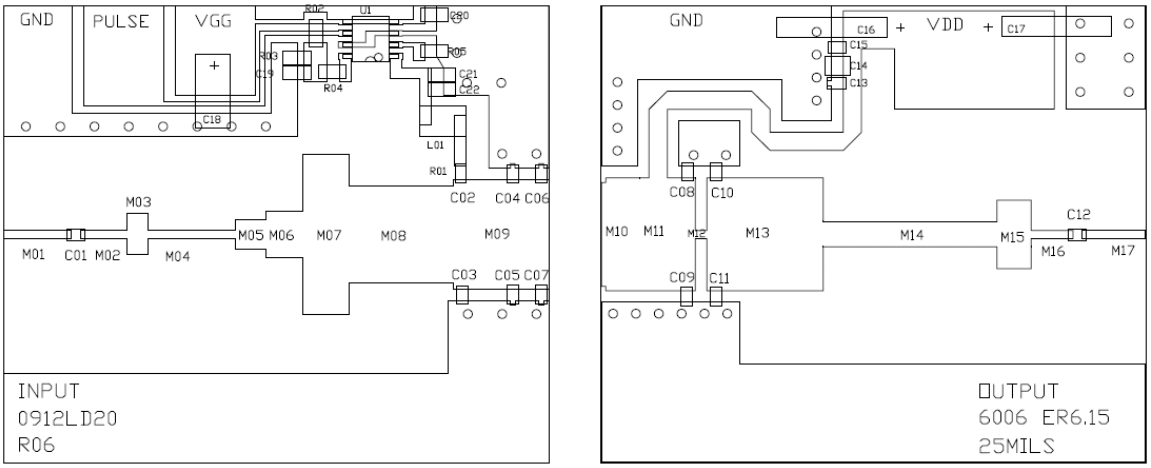
Freq = 1090 MHz (Performance optimized at 1090 MHz)

VDD = 28V, Idq = 80mA, Class-AB Bias

Mode-S Pulse Burst: 0.5uS ON/0.5 uS OFF, 128 pulses, repeated every 3.2 mS (LDTC = 2%)

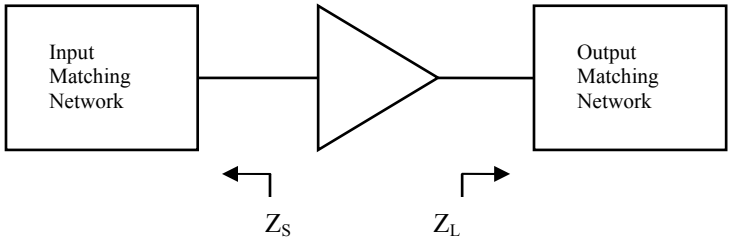
Pulse #	Pout		Gp	Pin		R.L(Input)	Droop
	dBm	W	dB	dBm	W	dB	(dB)
1	43.0	20.0	16.90	26.10	0.41	-12.60	-0.1
64	42.9	19.4	16.77	26.10	0.41		
128	42.9	19.5	16.80	26.10	0.41		

0912LD20 Test Circuit Layout



0912LD20 Test Circuit Component Designations and Values

Part	Description	Part	Description
C01, C12, C13, C22	43pF Chip Capacitor (ATC 100A)	C18	22uF, 63V Electrolytic Capacitor
C03, C10, C11	3.3pF Chip Capacitor (ATC 100A)	C17	47uF 63V Electrolytic Capacitor
C04, C05	2.4pF Chip Capacitor (ATC 100A)	C16	470uF, 63V Electrolytic Capacitor
C06, C07	9.1pF Chip Capacitor (ATC 100A)	C19, C20	1uF Chip Capacitor
C08, C09	7.5pF Chip Capacitor (ATC 100A)	C14, C21	1000pF Chip Capacitor
C05	4.7pF Chip Capacitor (ATC 100A)	C15	1nF Chip Capacitor
C16	3.0pF Chip Capacitor (ATC 100A)	C02, C03,	0.7pF Chip Capacitor (ATC 100B)
R01, R04	15Ω, 1/4W Chip Resistor	L01	6 Turns, 24 AWG, IDIA 0.092″
R02, R03	200, 1/4W Chip Resistor	R05	82.5Ω, 1/4W Chip Resistor
PCB	Rogers 6006, ε_r=6.15, 25mils, 1oz	M01	36 x 295 mils (W x L)
M02	36 x 200 mils (W x L)	M03	180 x 90 mils (W x L)
M04	36 x 387 mils (W x L)	M05	130 x 130 mils (W x L)
M06	200 x 165 mils (W x L)	M07	700 x 200 mils (W x L)
M08	420 x 429 mils (W x L)	M09	480 x 415 mils (W x L)
M10	454 x 18 mils (W x L)	M11	494 x 392 mils (W x L)
M12	36 x 50 mils (W x L)	M13	494 x 510 mils (W x L)
M14	110 x 760 mils (W x L)	M15	300 x 150 mils (W x L)
M16	36 x 183 mils (W x L)	M17	36 x 278 mils (W x L)
U1	ADG419, Analog Device		

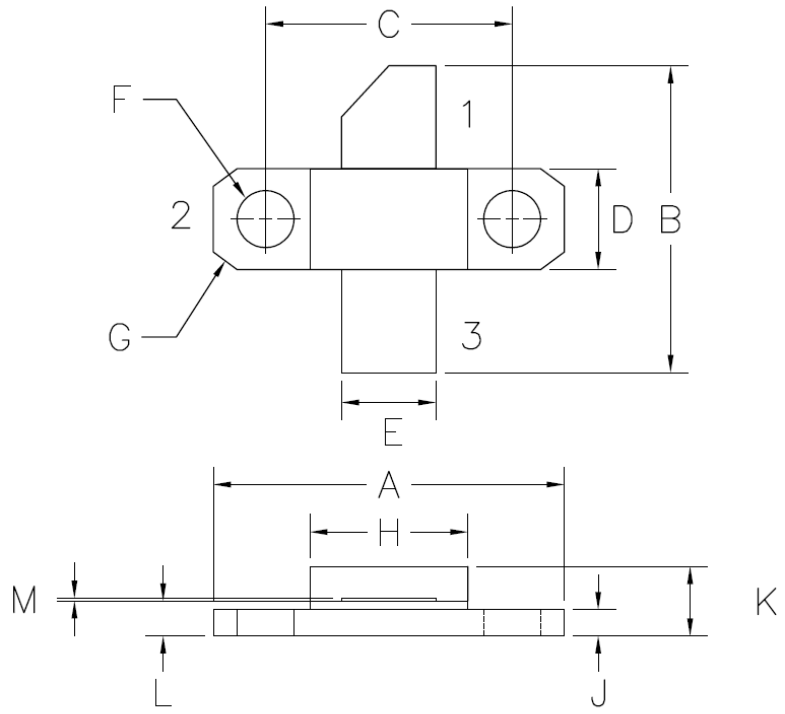


Typical Impedance Values

Frequency (MHz)	$Z_S(\Omega)$	$Z_L(\Omega)$
960	1.61 - j0.35	6.30 - j0.49
1090	2.26 + j0.40	4.98 - j0.82
1215	3.68 + j0.90	4.85 + j0.23

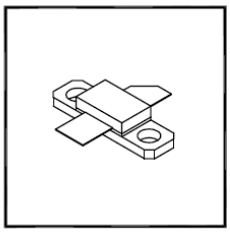
* V_{DS} = 28V, I_{DQ} = 80mA, P_{out} = 20W
* Pulse Format: 32µs, 2% Long Term Duty Factor

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED



DIM	MILLIMETER	±TOL	INCHES	±TOL
A	25.40	1.3	.800	.050
B	17.78	.13	.700	.005
C	14.27	.13	.562	.005
D	5.84	.13	.230	.005
E	5.46	.13	.215	.005
F	3.30 Dia	.13	.130 Dia	.005
G	45°	5°	45°	5°
H	9.14	.13	.360	.005
J	1.52	.13	.060	.005
K	3.51	.13	.138	.005
L	2.03	.13	.080	.005
M	0.10	.02	.004	.001

STYLE 1:
PIN 1 = DRAIN
2 = SOURCE
3 = GATE



Microsemi	CAGE 0PJR2	DWG NO. 55QT	REV A
		SCALE 3/1	SHEET