

RTL020P02

- 1) Low on-resistance. (80mΩ at 2.5V)
- 2) High power package.
- 3) High speed switching.
- 4) Low voltage drive. (2.5V)

DC-DC converter

Silicon P-channel
MOS FET

Type	Package	Taping
	Code	TR
	Basic ordering unit (pieces)	3000
RTL020P02		○

TUMT6

The drawing shows the top and side views of a TUMT6 package. The top view is a square with a side length of 2.0 ± 0.1 . It features a central square pad with a side length of 0.3 ± 0.1 and a square pad at each corner with a side length of 0.05 . The distance between the centers of the corner pads is 0.65 . The side view shows a package with a maximum height of 0.85 MAX and a maximum width of 0.2 MAX . The bottom of the package is flat, with a thickness of 0.17 ± 0.05 . The package is labeled with (1) through (6) corresponding to the legend.

(1) Drain
(2) Drain
(3) Gate
(4) Source
(5) Drain
(6) Drain

Each lead has same dimensions

Abbreviated symbol : WU

(1) Drain
(2) Drain
(3) Gate
(4) Source
(5) Drain
(6) Drain

*1 ESD PROTECTION DIODE
*2 BODY DIODE

Transistors

●Absolute maximum ratings (Ta=25°C)

Parameter	Symbol	Limits	Unit
Drain-source voltage	V _{DSS}	−20	V
Gate-source voltage	V _{GSS}	±12	V
Drain current	Continuous	I _D	A
	Pulsed	I _{DP}	A *1
Source current (Body diode)	Continuous	I _S	A *1
	Pulsed	I _{SP}	A
Total power dissipation	P _D	1	W *2
Channel temperature	T _{ch}	150	°C
Range of Storage temperature	T _{stg}	−55 to +150	°C

*1 P_W≤10μs, Duty cycle≤1%

*2 Mounted on a ceramic board

●Electrical characteristics (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I _{GSS}	−	−	±10	μA	V _{GS} =±12V, V _{DS} =0V
Drain-source breakdown voltage	V _{(BR) DSS}	−20	−	−	V	I _D = −1mA, V _{GS} =0V
Zero gate voltage drain current	I _{DSS}	−	−	−1	μA	V _{DS} = −20V, V _{GS} =0V
Gate threshold voltage	V _{GS(th)}	−0.7	−	−2.0	V	V _{DS} = −10V, I _D = −1mA
Static drain-source on-state resistance	R _{DS(on)} *	−	100	135	mΩ	I _D = −2A, V _{GS} = −4.5V
		−	110	150	mΩ	I _D = −2A, V _{GS} = −4V
		−	180	250	mΩ	I _D = −1A, V _{GS} = −2.5V
Forward transfer admittance	Y _{fs} *	1.2	−	−	S	V _{DS} = −10V, I _D = −1A
Input capacitance	C _{iss}	−	430	−	pF	V _{DS} = −10V
Output capacitance	C _{oss}	−	80	−	pF	V _{GS} =0V
Reverse transfer capacitance	C _{rss}	−	55	−	pF	f=1MHz
Turn-on delay time	t _{d(on)} *	−	11	−	ns	I _D = −1A
Rise time	t _r *	−	13	−	ns	V _{DD} ≐ −15V V _{GS} = −4.5V
Turn-off delay time	t _{d(off)} *	−	38	−	ns	R _L =15Ω
Fall time	t _f *	−	12	−	ns	R _{GS} =10Ω
Total gate charge	Q _g	−	4.9	−	nC	V _{DD} ≐ −15V R _L ≐7.5Ω
Gate-source charge	Q _{gs}	−	1.2	−	nC	V _{GS} = −4.5V R _{GS} =10Ω
Gate-drain charge	Q _{gd}	−	1.3	−	nC	I _D = −2A

*Pulsed

Body diode characteristics (source-drain characteristics)

Forward voltage	V _{SD}	−	−	−1.2	V	I _S = −0.8A, V _{GS} =0V
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Transistors

●Electrical characteristic curves

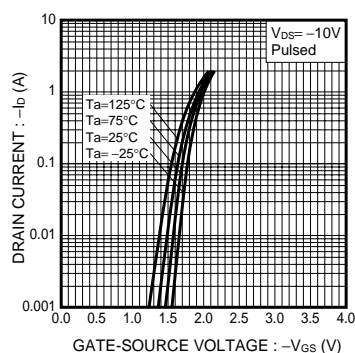


Fig.1 Typical Transfer Characteristics

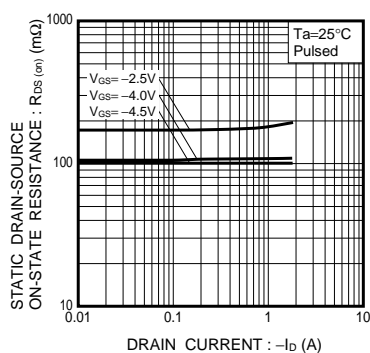


Fig.2 Static Drain-Source On-State Resistance vs. Drain Current

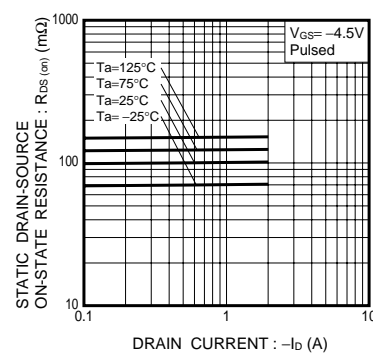


Fig.3 Static Drain-Source On-State Resistance vs. Drain Current

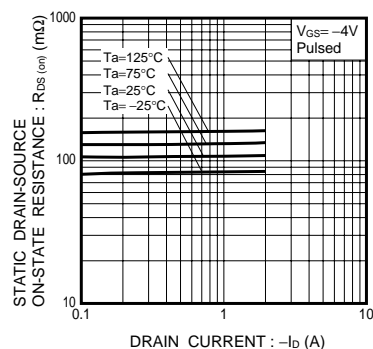


Fig.4 Static Drain-Source On-State Resistance vs. Drain Current

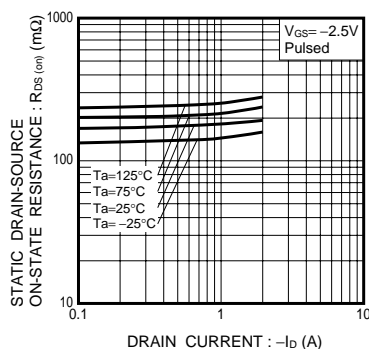


Fig.5 Static Drain-Source On-State Resistance vs. Drain Current

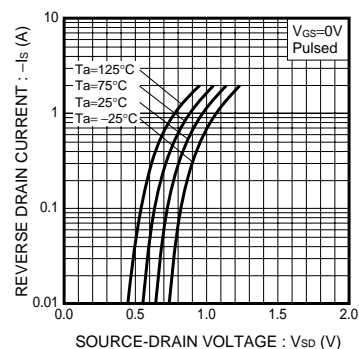


Fig.6 Reverse Drain Current vs. Source-Drain Voltage

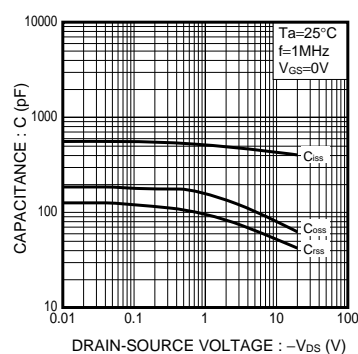


Fig.7 Typical Capacitance vs. Drain-Source Voltage

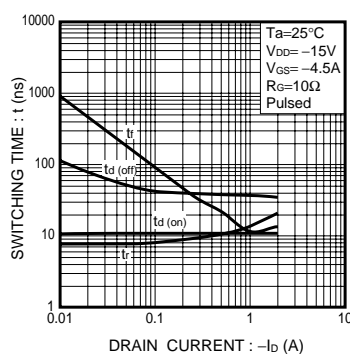


Fig.8 Switching Characteristics

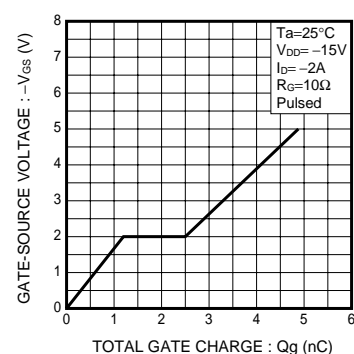


Fig.9 Dynamic Input Characteristics

Transistors

●Measurement circuits

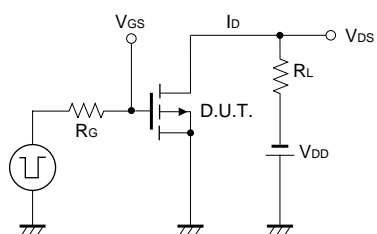


Fig.10 Switching Time Measurement Circuit

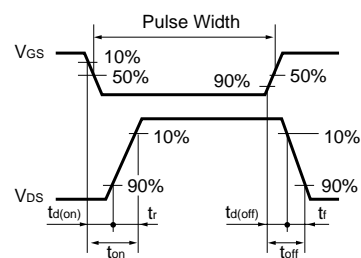


Fig.11 Switching Waveforms

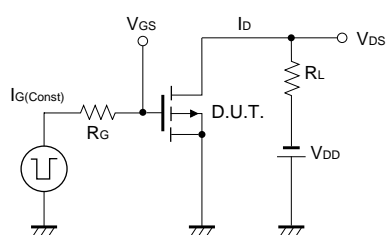


Fig.12 Gate Charge Measurement Circuit

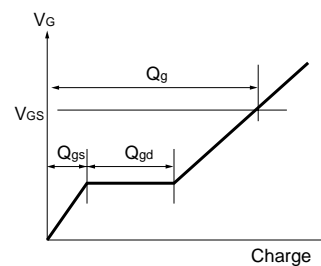


Fig.13 Gate Charge Waveforms

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