Spartan Family of One-Time Programmable Configuration PROMs (XC17S00)

DS030 (v1.8) October 10, 2001

Product Specification

Introduction

The Spartan™ family of PROMs provides an easy-to-use, cost-effective method for storing Spartan device configuration bitstreams.

When the Spartan device is in Master Serial mode, it generates a configuration clock that drives the Spartan PROM. A short access time after the rising clock edge, data appears on the PROM DATA output pin that is connected to the Spartan device D_{IN} pin. The Spartan device generates the appropriate number of clock pulses to complete the configuration. Once configured, it disables the PROM. When a Spartan device is in Slave Serial mode, the PROM and the Spartan device must both be clocked by an incoming signal.

For device programming, either the Xilinx Alliance or the Foundation series development systems compiles the Spartan device design file into a standard HEX format which is then transferred to most commercial PROM programmers.

Spartan PROM Features

- Configuration one-time programmable (OTP) read-only memory designed to store configuration bitstreams for Spartan, Spartan-XL, and Spartan-II FPGA devices
- Simple interface to the Spartan device requires only one user I/O pin
- Programmable reset polarity (active High or active Low)
- Low-power CMOS floating gate process
- Available in 5V and 3.3V versions
- Available in compact plastic 8-pin DIP, 8-pin VOIC, or 20-pin SOIC packages.
- Programming support by leading programmer manufacturers.
- Design support using the Xilinx Alliance and Foundation series software packages.
- Guaranteed 20 year life data retention

Spartan FPGA	Configuration Bits	Compatible Spartan PROM
XCS05	53,984	XC17S05
XCS05XL	54,544	XC17S05XL
XCS10	95,008	XC17S10
XCS10XL	95,752	XC17S10XL
XCS20	178,144	XC17S20
XCS20XL	179,160	XC17S20XL
XCS30	247,968	XC17S30
XCS30XL	249,168	XC17S30XL
XCS40	329,312	XC17S40
XCS40XL	330,696	XC17S40XL
XC2S50	559,232	XC17S50XL
XC2S100	781,248	XC17S100XL
XC2S150	1,040,128	XC17S150XL

Pin Description

Table 1: **Spartan PROM Pinouts**

Pin Name	8-pin PDIP and VOIC	20-pin SOIC	Pin Description
DATA	1	1	Data output, High-Z state when either $\overline{CE}$ or $\overline{OE}$ are inactive. During programming, the DATA pin is I/O. Note that $\overline{OE}$ can be programmed to be either active High or active Low.
CLK	2	3	Each rising edge on the CLK input increments the internal address counter, if both $\overline{CE}$ and $\overline{OE}$ are active.
RESET/$\overline{OE}$ (OE/$\overline{RESET}$)	3	8	When High, this input holds the address counter reset and puts the DATA output in a high-impedance state. The polarity of this input pin is programmable as either RESET/$\overline{OE}$ or OE/$\overline{RESET}$. To avoid confusion, this document describes the pin as RESET/$\overline{OE}$, although the opposite polarity is possible on all devices. When RESET is active, the address counter is held at zero, and the DATA output is in a high-impedance state. The polarity of this input is programmable. The default is active High RESET, but the preferred option is active Low $\overline{RESET}$, because it can be driven by the FPGAs $\overline{INIT}$ pin. The polarity of this pin is controlled in the programmer interface. This input pin is easily inverted using the Xilinx HW-130 programmer software. Third-party programmers have different methods to invert this pin.
CE	4	10	When High, this pin disables the internal address counter, puts the DATA output in a high-impedance state, and forces the device into low-I_{CC} standby mode.
GND	5	11	GND is the ground connection.
V_{CC}	7, 8	18, 20	The V_{CC} pins are to be connected to the positive voltage supply.

Notes:
1. Pins not listed in the table are reserved and ***must*** not be externally connected.

Controlling PROMs

Connecting the Spartan device with the PROM:

- The DATA output of the PROM drives the D_{IN} input of the lead Spartan device.
- The Master Spartan device CCLK output drives the CLK input of the PROM.
- The $\overline{RESET}$/OE input of the PROM is driven by the $\overline{INIT}$ output of the Spartan device. This connection assures that the PROM address counter is reset before the start of any (re)configuration, even when a reconfiguration is initiated by a V_{CC} glitch. Other methods—such as driving $\overline{RESET}$/OE from $\overline{LDC}$ or system reset—assume that the PROM internal power-on-reset is always in step with the FPGAs internal power-on-reset, which may not be a safe assumption.
- The $\overline{CE}$ input of the PROM is driven by the DONE output of the Spartan device, provided that DONE is not permanently grounded. Otherwise, $\overline{LDC}$ can be used to drive $\overline{CE}$, but must then be unconditionally High during user operation. $\overline{CE}$ can also be permanently tied Low, but this keeps the DATA output active and causes an unnecessary supply current of 10 mA maximum.

FPGA Master Serial Mode Summary

The I/O and logic functions of the Configurable Logic Block (CLB) and their associated interconnections are established by a configuration program. The program is loaded either automatically upon power up, or on command, depending on the state of the Spartan device MODE pin. In Master Serial mode, the Spartan device automatically loads the configuration program from an external memory. The Spartan PROM has been designed for compatibility with the Master Serial mode.

Upon power-up or reconfiguration, the Spartan device enters the Master Serial mode when the MODE pin is Low. Data is read from the PROM sequentially on a single data line. Synchronization is provided by the rising edge of the temporary signal CCLK, which is generated during configuration.

Master Serial mode provides a simple configuration interface (Figure 1). Only a serial data line and two control lines are required to configure the Spartan device. Data from the PROM is read sequentially, accessed via the internal address and bit counters which are incremented on every valid rising edge of CCLK.

If the user-programmable, dual-function D_{IN} pin on the Spartan device is used only for configuration, it must still be held at a defined level during normal operation. The Spartan family takes care of this automatically with an on-chip default pull-up resistor.

Programming the FPGA With Counters Unchanged Upon Completion

When multiple-configurations for a single Spartan device are stored in a PROM, the $\overline{OE}$ pin should be tied Low. Upon power-up, the internal address counters are reset and configuration begins with the first program stored in memory. Since the $\overline{OE}$ pin is held Low, the address counters are left unchanged after configuration is complete. Therefore, to reprogram the FPGA with another program, the DONE line is pulled Low and configuration begins at the last value of the address counters.

This method fails if a user applies $\overline{RESET}$ during the Spartan device configuration process. The Spartan device aborts the configuration and then restarts a new configuration, as intended, but the PROM does not reset its address counter, since it never saw a High level on its $\overline{OE}$ input. The new configuration, therefore, reads the remaining data in the PROM and interprets it as preamble, length count etc. Since the Spartan device is the Master, it issues the necessary number of CCLK pulses, up to 16 million (2^{24}) and DONE goes High. However, the Spartan device configuration will be completely wrong, with potential contentions inside the Spartan device and on its output pins. This method must, therefore, never be used when there is any chance of external reset during configuration.

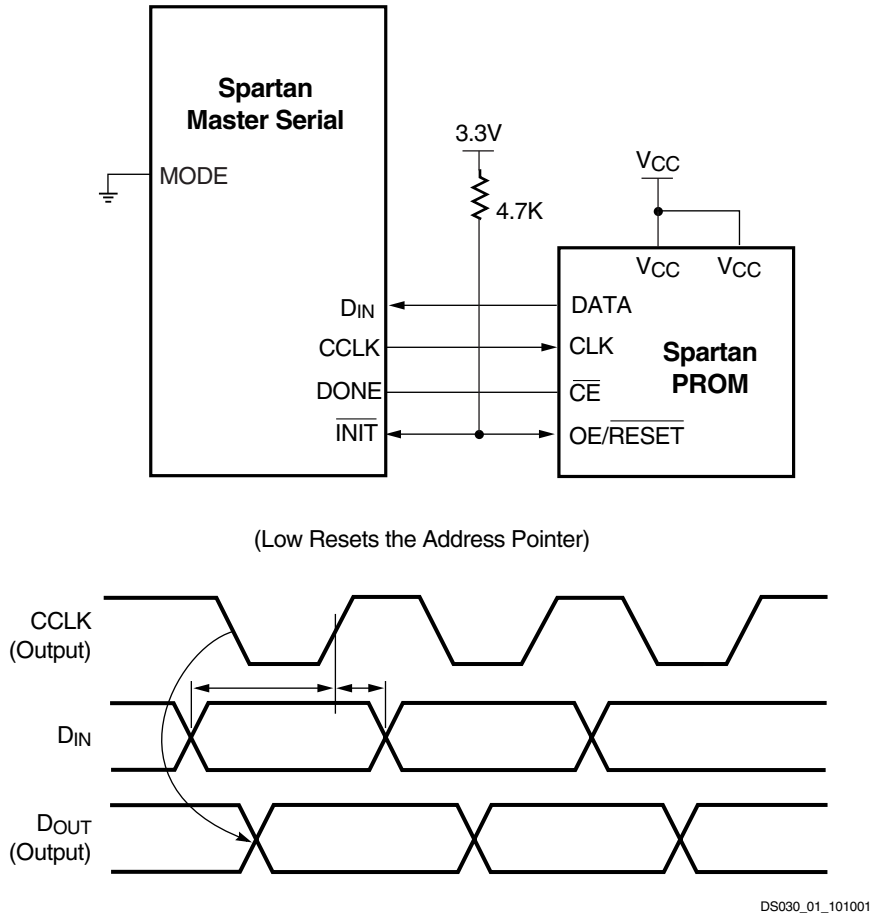


Figure 1: **Master Serial Mode.** The one-time-programmable Spartan PROM supports automatic loading of configuration programs. An early DONE inhibits the PROM data output one CCLK cycle before the Spartan FPGA I/Os become active.

Standby Mode

The PROM enters a low-power standby mode whenever $\overline{CE}$ is asserted High. The output remains in a high-impedance state regardless of the state of the $\overline{OE}$ input.

Programming the Spartan Family PROMs

The devices can be programmed on programmers supplied by Xilinx or qualified third-party vendors. The user must ensure that the appropriate programming algorithm and the latest version of the programmer software are used. The wrong choice can permanently damage the device.

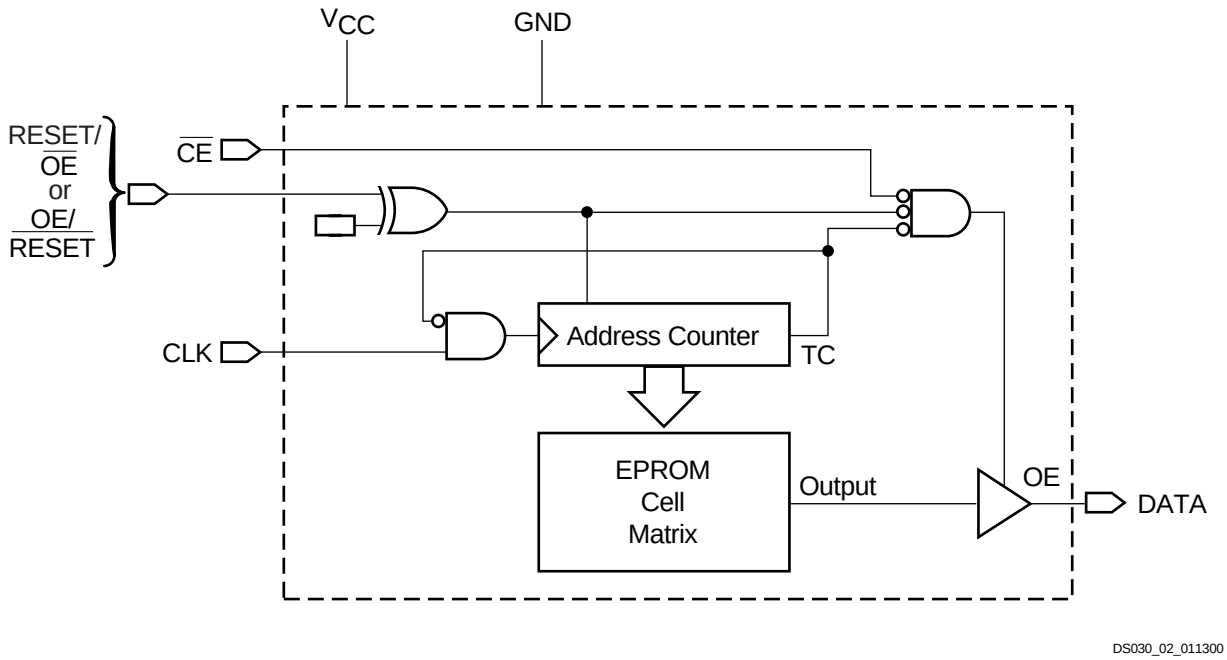


Figure 2: **Simplified Block Diagram (does not show programming circuit)**

Important: Always tie the two V_{CC} pins together in your application.

Table 2: **Truth Table for XC17S00 Control Inputs**

Control Inputs		Internal Address(2)	Outputs	
RESET(1)	CE		DATA	I_{CC}
Inactive	Low	If address ≤ TC: increment If address > TC: don't change	Active High-Z	Active Reduced
Active	Low	Held reset	High-Z	Active
Inactive	High	Not changing	High-Z	Standby
Active	High	Held reset	High-Z	Standby

Notes:
1. The XC17S00 RESET input has programmable polarity
2. TC = Terminal Count = highest address value. TC + 1 = address 0.

XC17S05, XC17S10, XC17S20, XC17S30, XC17S40

Absolute Maximum Ratings(1)

Symbol	Description	Value	Units
V_{CC}	Supply voltage relative to GND	–0.5 to +7.0	V
V_{IN}	Input voltage relative to GND	–0.5 to V_{CC} +0.5	V
V_{TS}	Voltage applied to High-Z output	–0.5 to V_{CC} +0.5	V
T_{STG}	Storage temperature (ambient)	–65 to +150	°C
T_{SOL}	Maximum soldering temperature (10s @ 1/16 in.)	+260	°C

Notes:
1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

Operating Conditions(1)

Symbol	Description	Conditions	Min	Max	Units
V_{CC}	Commercial	Supply voltage relative to GND (T_A = 0°C to +70°C)	4.75	5.25	V
	Industrial	Supply voltage relative to GND (T_A = –40°C to +85°C)	4.50	5.50	V

Notes:
1. During normal read operation both V_{CC} pins must be connected together.

DC Characteristics Over Operating Condition

Symbol	Description		Min	Max	Units
V_{IH}	High-level input voltage		2.0	V_{CC}	V
V_{IL}	Low-level input voltage		0	0.8	V
V_{OH}	High-level output voltage (I_{OH} = –4 mA)	Commercial	3.86	-	V
V_{OL}	Low-level output voltage (I_{OL} = +4 mA)		-	0.32	V
V_{OH}	High-level output voltage (I_{OH} = –4 mA)	Industrial	3.76	-	V
V_{OL}	Low-level output voltage (I_{OL} = +4 mA)		-	0.37	V
I_{CCA}	Supply current, active mode (at maximum frequency)		-	10	mA
I_{CCS}	Supply current, standby mode	XC17S05, XC17S10, XC17S20, XC17S30	-	50	µA
		XC17S40	-	100	µA
I_L	Input or output leakage current		–10	10	µA
C_{IN}	Input Capacitance (V_{IN} = GND, f = 1.0 MHz)		-	10	pF
C_{OUT}	Output Capacitance (V_{IN} = GND, f = 1.0 MHz)		-	10	pF

XC17S05XL, XC17S10XL, XC17S20XL, XC17S30XL, XC17S40XL, XC17S50XL, XC17S100XL, XC17S150XL

Absolute Maximum Ratings(1)

Symbol	Description	Value	Units
V_{CC}	Supply voltage relative to GND	–0.5 to +4.0	V
V_{IN}	Input voltage with respect to GND	–0.5 to V_{CC} +0.5	V
V_{TS}	Voltage applied to High-Z output	–0.5 to V_{CC} +0.5	V
T_{STG}	Storage temperature (ambient)	–65 to +150	°C
T_{SOL}	Maximum soldering temperature (10s @ 1/16 in.)	+260	°C

Notes:
1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

Operating Conditions(1)

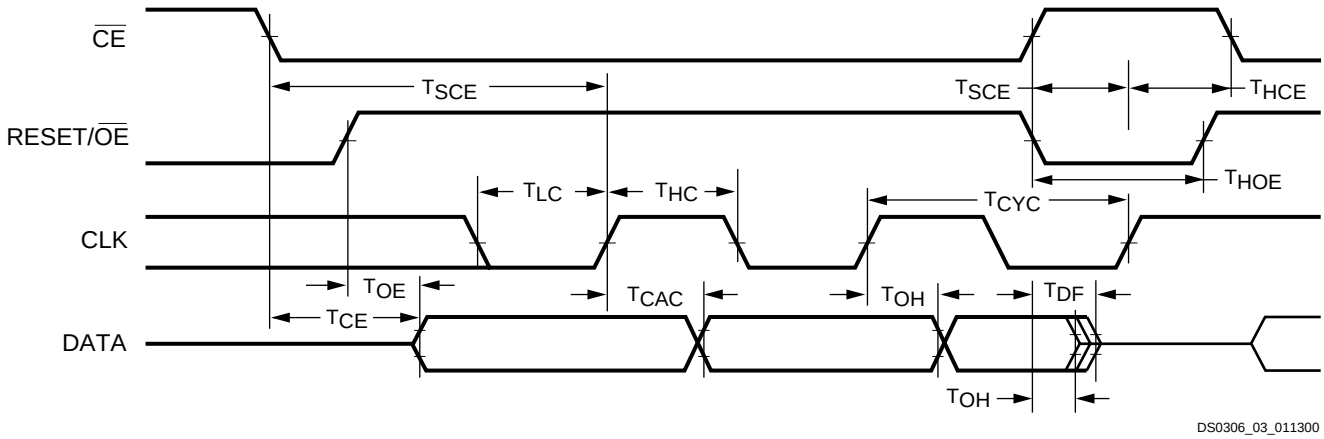
Symbol	Description		Min	Max	Units
V_{CC}	Commercial	Supply voltage relative to GND (T_A = 0°C to +70°C)	3.0	3.6	V
	Industrial	Supply voltage relative to GND (T_A = –40°C to +85°C)	3.0	3.6	V

Notes:
1. During normal read operation both V_{CC} pins must be connected together.

DC Characteristics Over Operating Condition

Symbol	Description	Min	Max	Units
V_{IH}	High-level input voltage	2.0	V_{CC}	V
V_{IL}	Low-level input voltage	0	0.8	V
V_{OH}	High-level output voltage (I_{OH} = –3 mA)	2.4	-	V
V_{OL}	Low-level output voltage (I_{OL} = +3 mA)	-	0.4	V
I_{CCA}	Supply current, active mode (at maximum frequency)	-	5	mA
I_{CCS}	Supply current, standby mode	-	50	µA
I_L	Input or output leakage current	–10	10	µA
C_{IN}	Input Capacitance (V_{IN} = GND, f = 1.0 MHz)	-	10	pF
C_{OUT}	Output Capacitance (V_{IN} = GND, f = 1.0 MHz)	-	10	pF

AC Characteristics Over Operating Condition(1)



Symbol	Description	Min	Max	Units
T_{OE}	RESET/$\overline{OE}$ to Data Delay	-	45	ns
T_{CE}	$\overline{CE}$ to Data Delay	-	60	ns
T_{CAC}	CLK to Data Delay	-	80	ns
T_{OH}	Data Hold From $\overline{CE}$, RESET/$\overline{OE}$, or CLK(2)	0	-	ns
T_{DF}	$\overline{CE}$ or RESET/$\overline{OE}$ to Data Float Delay(2,3)	-	50	ns
T_{CYC}	Clock Periods	100	-	ns
T_{LC}	CLK Low Time(2)	50	-	ns
T_{HC}	CLK High Time(2)	50	-	ns
T_{SCE}	$\overline{CE}$ Setup Time to CLK (to guarantee proper counting)	25	-	ns
T_{HCE}	$\overline{CE}$ Hold Time to CLK (to guarantee proper counting)	0	-	ns
T_{HOE}	RESET/$\overline{OE}$ Hold Time (guarantees counters are reset)	25	-	ns

Notes:
1. AC test load = 50 pF
2. Guaranteed by design, not tested.
3. Float delays are measured with 5 pF AC loads. Transition is measured at ±200 mV from steady state active levels.
4. All AC parameters are measured with V_{IL} = 0.0V and V_{IH} = 3.0V.

Ordering Information

XC17S20XL VO8 C

Device Number

XC17S05
XC17S05XL
XC17S10
XC17S10XL
XC17S20
XC17S20XL
XC17S30
XC17S30XL
XC17S40
XC17S40XL
XC17S50XL
XC17S100XL
XC17S150XL

Package Type

PD8 = 8-pin Plastic DIP
VO8 = 8-pin Plastic Small-Outline Thin Package
SO20 = 20-pin Plastic Small-Outline Package

Operating Range/Processing

C = Commercial (T_A = 0°C to +70°C)
I = Industrial (T_A = –40°C to +85°C)

Spartan 5V Valid Ordering Combinations (XC17S00)

XC17S05PD8C	XC17S10PD8C	XC17S20PD8C	XC17S30PD8C	XC17S40PD8C
XC17S05VO8C	XC17S10VO8C	XC17S20VO8C	XC17S30VO8C	XC17S40SO20C
XC17S05PD8I	XC17S10PD8I	XC17S20PD8I	XC17S30PD8I	XC17S40PD8I
XC17S05VO8I	XC17S10VO8I	XC17S20VO8I	XC17S30VO8I	XC17S40SO20I

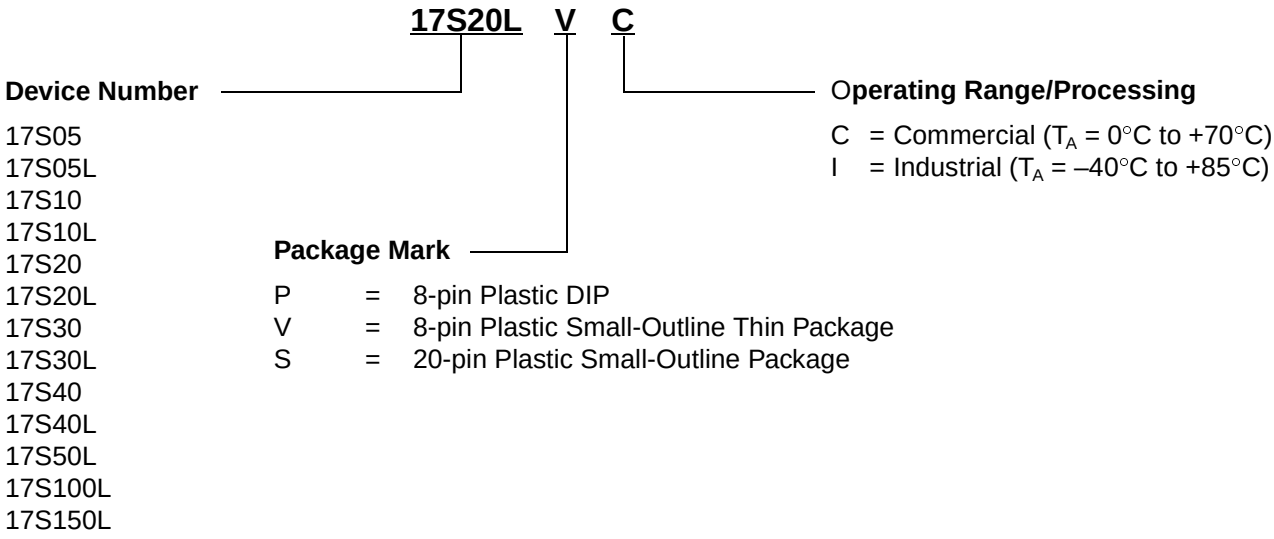
Spartan 3.3V Valid Ordering Combinations (XC17S00XL)

XC17S05XLPD8C	XC17S100XLPD8C	XC17S20XLPD8C	XC17S40XLPD8C
XC17S05XLVO8C	XC17S100XLSO20C	XC17S20XLVO8C	XC17S40XLSO20C
XC17S05XLPD8I	XC17S100XLPD8I	XC17S20XLPD8I	XC17S40XLPD8I
XC17S05XLVO8I	XC17S100XLSO20I	XC17S20XLVO8I	XC17S40XLSO20I
XC17S10XLPD8C	XC17S150XLPD8C	XC17S30XLPD8C	XC17S50XLPD8C
XC17S10XLVO8C	XC17S150XLSO20C	XC17S30XLVO8C	XC17S50XLSO20C
XC17S10XLPD8I	XC17S150XLPD8I	XC17S30XLPD8I	XC17S50XLPD8I
XC17S10XLVO8I	XC17S150XLSO20I	XC17S30XLVO8I	XC17S50XLSO20I

Marking Information

Due to the small size of the PROM package, the complete ordering part number cannot be marked on the package. The XC

prefix is deleted and the package code is simplified. Device marking is as follows.



Note: When marking the device number on the XL parts, an L is used in place of an XL.

Revision History

The following table shows the revision history for this document.

Date	Revision	Revision
07/14/98	1.1	Cosmetic edits for pages 1, 2, and 3.
09/08/98	1.2	Clarified the SPARTAN FPGA and PROM interface by removing references to $\overline{CEO}$ pin. Removed the ESD notation in Absolute Maximum table since it is now included in Xilinx's Reliability Monitor Report.
01/20/00	1.3	Added additional Spartan-XL parts, changed SPROM to PROM.
02/18/00	1.4	Changed device ordering numbers, added 4.7K resistor to OE/$\overline{RESET}$ in Figure 1.
04/04/00	1.5	Added XC17S200XL PROM for Spartan XC2S200.
08/06/00	1.6	Updated format.
04/07/01	1.7	Added to features: "Guaranteed 20 year life data retention."
10/10/01	1.8	Added a note to Table 1. Changed V_{PP} to V_{CC} on Figure 1.