SN54ABT16501, SN74ABT16501
18-BIT UNIVERSAL BUS TRANSCEIVERS
WITH 3-STATE OUTPUTS

- **Members of the Texas Instruments _Widebus_™ Family**

- **State-of-the-Art _EPIC_-II_B_™ BiCMOS Design Significantly Reduces Power Dissipation**

- **_UBT_™ (Universal Bus Transceiver) Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, or Clocked Mode**

- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**

- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**

- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 5 V, T_A = 25°C**

- **Flow-Through Architecture Optimizes PCB Layout**

- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings**

SN54ABT16501 . . . WD PACKAGE
SN74ABT16501 . . . DGG OR DL PACKAGE
(TOP VIEW)

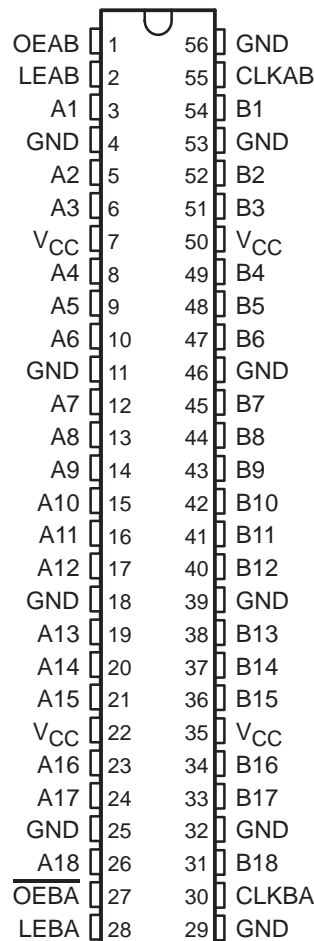|			
OEAB	1	56	GND
LEAB	2	55	CLKAB
A1	3	54	B1
GND	4	53	GND
A2	5	52	B2
A3	6	51	B3
V_{CC}	7	50	V_{CC}
A4	8	49	B4
A5	9	48	B5
A6	10	47	B6
GND	11	46	GND
A7	12	45	B7
A8	13	44	B8
A9	14	43	B9
A10	15	42	B10
A11	16	41	B11
A12	17	40	B12
GND	18	39	GND
A13	19	38	B13
A14	20	37	B14
A15	21	36	B15
V_{CC}	22	35	V_{CC}
A16	23	34	B16
A17	24	33	B17
GND	25	32	GND
A18	26	31	B18
$\overline{OEBA}$	27	30	CLKBA
LEBA	28	29	GND

description

These 18-bit universal bus transceivers consist of storage elements that can operate either as D-type latches or D-type flip-flops to allow data flow in transparent or clocked modes.

Data flow in each direction is controlled by output-enable (OEAB and $\overline{OEBA}$), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if CLKAB is held at a high or low logic level. If LEAB is low, the A data is stored in the latch/flip-flop on the low-to-high transition of CLKAB. When OEAB is high, the outputs are active. When OEAB is low, the outputs are in the high-impedance state.

Data flow for B to A is similar to that of A to B but uses $\overline{OEBA}$, LEBA, and CLKBA. The output enables are complementary (OEAB is active high and $\overline{OEBA}$ is active low).

To ensure the high-impedance state during power up or power down, OE should be tied to GND through a pulldown resistor and $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sourcing/current-sinking capability of the driver.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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description (continued)

The SN54ABT16501 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT16501 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE†

INPUTS				OUTPUT
OEAB	LEAB	CLKAB	A	B
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	↑	L	L
H	L	↑	H	H
H	L	H	X	B_0‡
H	L	L	X	B_0§

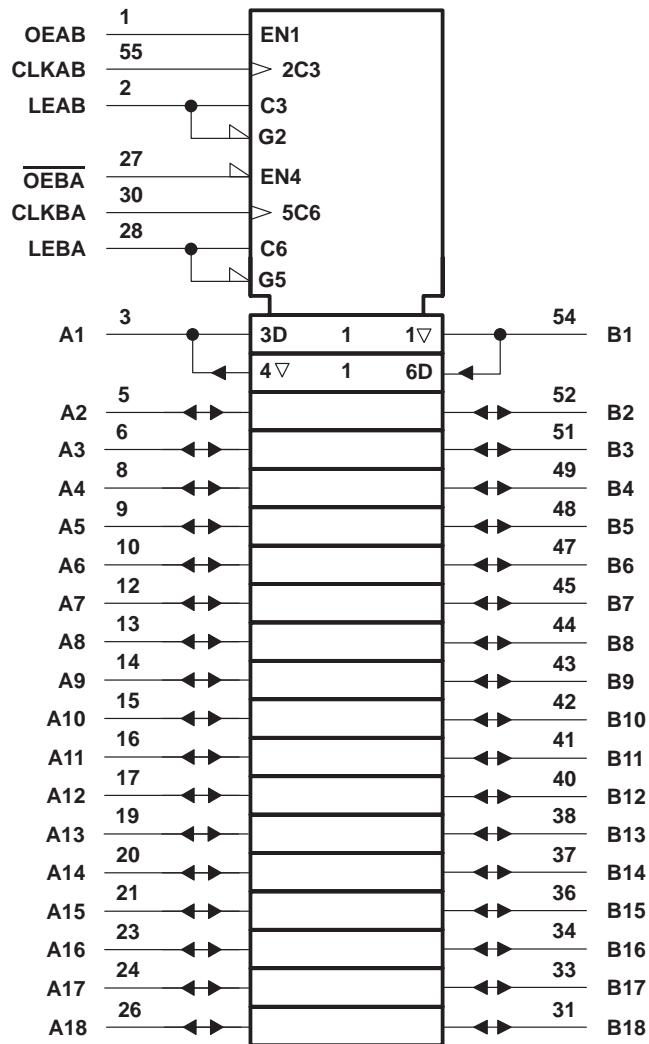† A-to-B data flow is shown: B-to-A flow is similar but uses OEBA, LEBA, and CLKBA.

‡ Output level before the indicated steady-state input conditions were established, provided that CLKAB was high before LEAB went low

§ Output level before the indicated steady-state input conditions were established

logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)

To 17 Other Channels
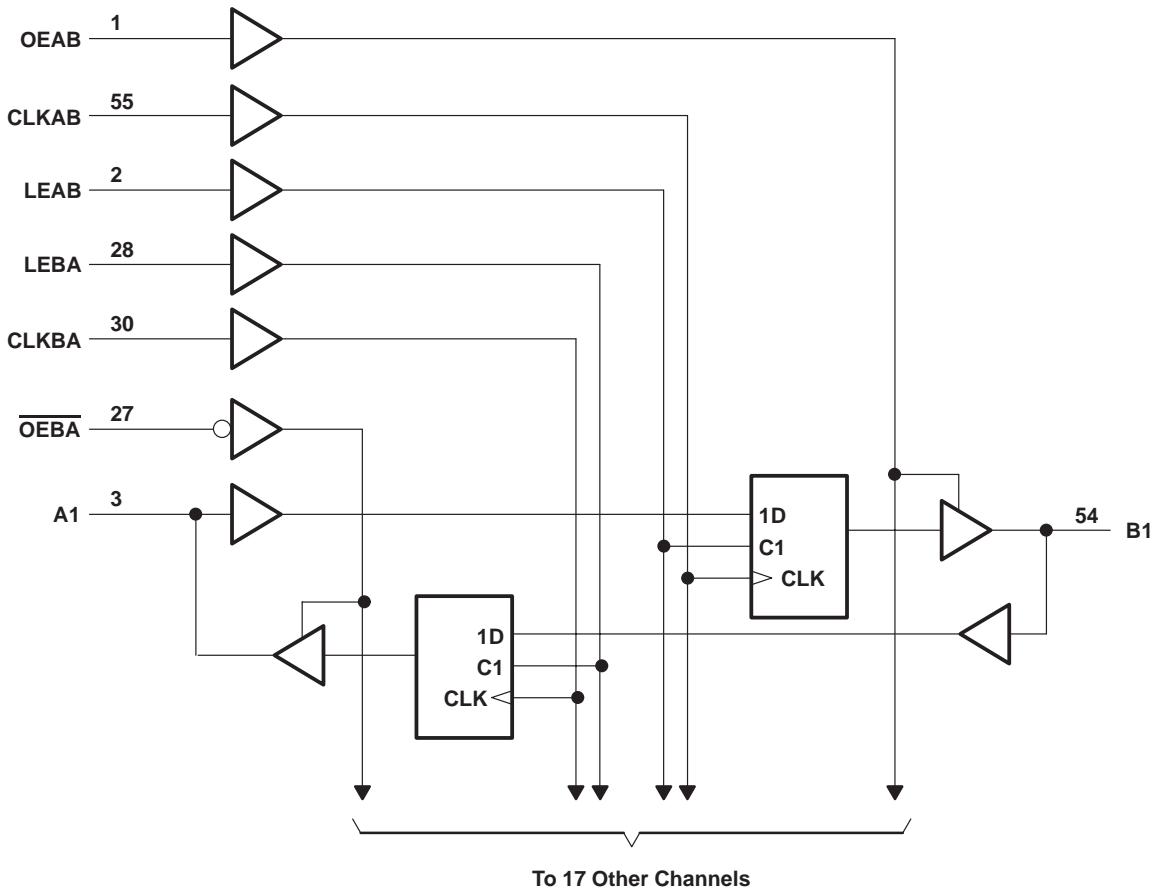
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} .... –0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1) .... –0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, V_O .... –0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT16501 .... 96 mA
                                             SN74ABT16501 .... 128 mA
Input clamp current, I_{IK} (V_I < 0) .... –18 mA
Output clamp current, I_{OK} (V_O < 0) .... –50 mA
Package thermal impedance, θ_{JA} (see Note 2): DGG package .... 81°C/W
                                            DL package .... 74°C/W
Storage temperature range, T_{stg} .... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
       2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51.

recommended operating conditions (see Note 3)

			SN54ABT16501		SN74ABT16501		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t / \Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 3: Unused pins (input or I/O) must be held high or low to prevent them from floating.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		$T_A = 25°C$ MIN	$T_A = 25°C$ TYP†	$T_A = 25°C$ MAX	SN54ABT16501 MIN	SN54ABT16501 MAX	SN74ABT16501 MIN	SN74ABT16501 MAX	UNIT
V_{IK}		$V_{CC} = 4.5$ V,	$I_I = -18$ mA			−1.2		−1.2		−1.2	V
V_{OH}		$V_{CC} = 4.5$ V,	$I_{OH} = -3$ mA	2.5			2.5		2.5		V
		$V_{CC} = 5$ V,	$I_{OH} = -3$ mA	3			3		3		
		$V_{CC} = 4.5$ V	$I_{OH} = -24$ mA	2			2				
			$I_{OH} = -32$ mA	2*					2		
V_{OL}		$V_{CC} = 4.5$ V	$I_{OL} = 48$ mA			0.55		0.55			V
			$I_{OL} = 64$ mA			0.55*				0.55	
V_{hys}					100						mV
I_I	Control inputs	$V_{CC} = 5.5$ V,	$V_I = V_{CC}$ or GND			±1		±1		±1	µA
	A or B ports					±100		±100		±100	
I_{OZH}‡		$V_{CC} = 5.5$ V,	$V_O = 2.7$ V			50		50		50	µA
I_{OZL}‡		$V_{CC} = 5.5$ V,	$V_O = 0.5$ V			−50		−50		−50	µA
I_{off}		$V_{CC} = 0$,	V_I or $V_O \leq 4.5$ V			±100				±100	µA
I_{CEX}		$V_{CC} = 5.5$ V, $V_O = 5.5$ V				50		50		50	µA
I_O§		$V_{CC} = 5.5$ V,	$V_O = 2.5$ V	−50	−100	−180	−50	−180	−50	−180	mA
I_{CC}	A or B ports	$V_{CC} = 5.5$ V, $I_O = 0$, $V_I = V_{CC}$ or GND	Outputs high			3		5		3	mA
			Outputs low			76		76		76	
			Outputs disabled			3.3		5.3		3.3	
ΔI_{CC}¶	Control inputs	$V_{CC} = 5.5$ V, One input at 3.4 V, Other inputs at V_{CC} or GND				5		6		5	mA
	A or B ports					1.5		1.5		1.5	
C_i	Control inputs	$V_I = 2.5$ V or 0.5 V			4						pF
C_{io}	A or B ports	$V_O = 2.5$ V or 0.5 V			8						pF

* On products compliant to MIL-PRF-38535, this parameter does not apply.
† All typical values are at $V_{CC} = 5$ V.
‡ The parameters I_{OZH} and I_{OZL} include the input leakage current.
§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

				SN54ABT16501 MIN	SN54ABT16501 MAX	SN74ABT16501 MIN	SN74ABT16501 MAX	UNIT
f_{clock}	Clock frequency, CLKAB or CLKBA			0	105	0	105	MHz
t_w#	Pulse duration	LEAB or LEBA high		3.3		3.3		ns
		CLKAB or CLKBA high or low		4.7		4.7		
t_{su}	Setup time	A before CLKAB↑ or B before CLKBA↑		4		3.5		ns
		A before LEAB↓ or B before LEBA↓	CLK high	4		4		
			CLK low	1.5		1.5		
t_h	Hold time	A after CLKAB↑ or B after CLKBA↑		1		1		ns
		A after LEAB↓ or B after LEBA↓		2.5		2.5		

This parameter is specified by design, but not production tested.

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT16501		SN74ABT16501		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}	CLKAB or CLKBA		105	160		105		105		MHz
t_{PLH}	A or B	B or A	1	2.6	3.4	1	3.9	1	3.7	ns
t_{PHL}			1	2.6	3.4	1	4.1	1	4	
t_{PLH}	LEAB or LEBA	B or A	1.3	3.3	4.3	1.3	5.4	1.3	5.1	ns
t_{PHL}			1.4	3.1	4.1	1.4	4.6	1.4	4.4	
t_{PLH}	CLKAB or CLKBA	B or A	1.5	3.5	4.5	1.5	5.3	1.5	5	ns
t_{PHL}			1.3	3.1	4.1	1.3	4.6	1.3	4.4	
t_{PZH}	OEAB or $\overline{OEBA}$	B or A	1	3	4	1	4.8	1	4.7	ns
t_{PZL}			2.6	4.9	5.9	2.6	6.6	2.6	6.5	
t_{PHZ}	OEAB or $\overline{OEBA}$	B or A	1.6	3.9	4.9	1.6	5.9	1.6	5.8	ns
t_{PLZ}			1.1	3.4	4.4	1.1	5.1	1.1	4.9	

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PARAMETER MEASUREMENT INFORMATION

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

LOAD CIRCUIT

From Output Under Test — C_L = 50 pF (see Note A) — 500 Ω — 500 Ω — S1 — 7 V, Open, GND
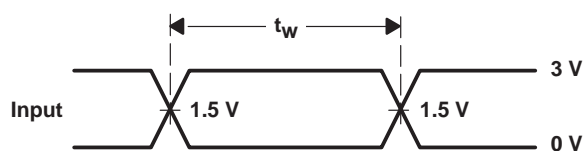
VOLTAGE WAVEFORMS
PULSE DURATION

t_w — Input — 1.5 V — 1.5 V — 3 V / 0 V
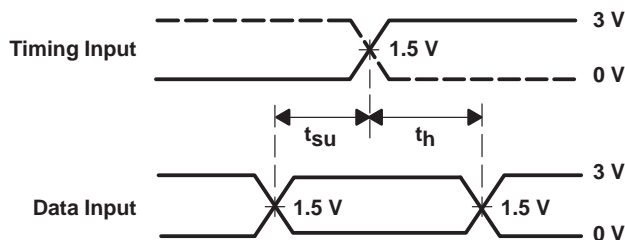
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES

Timing Input — 1.5 V — 3 V / 0 V
t_{su} — t_h
Data Input — 1.5 V — 1.5 V — 3 V / 0 V

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS

Input — 1.5 V — 1.5 V — 3 V / 0 V
t_{PLH} — t_{PHL}
Output — 1.5 V — 1.5 V — V_{OH} / V_{OL}
t_{PHL} — t_{PLH}
Output — 1.5 V — 1.5 V — V_{OH} / V_{OL}
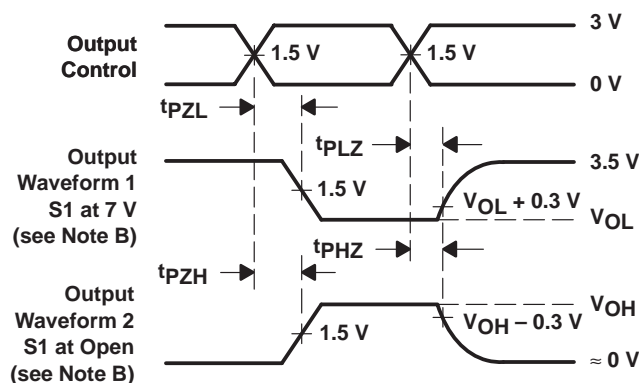
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

Output Control — 1.5 V — 1.5 V — 3 V / 0 V
t_{PZL} — t_{PLZ}
Output Waveform 1 S1 at 7 V (see Note B) — 1.5 V — 3.5 V, V_{OL} + 0.3 V, V_{OL}
t_{PZH} — t_{PHZ}
Output Waveform 2 S1 at Open (see Note B) — 1.5 V — V_{OH}, V_{OH} − 0.3 V, ≈ 0 V

NOTES: A. C_L includes probe and jig capacitance.
   B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
      Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
   C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
   D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74ABT16501DGGR	Active	Production	TSSOP (DGG) | 56	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT16501
SN74ABT16501DGGR.B	Active	Production	TSSOP (DGG) | 56	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT16501
SN74ABT16501DL	Active	Production	SSOP (DL) | 56	20 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT16501
SN74ABT16501DL.B	Active	Production	SSOP (DL) | 56	20 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT16501
SN74ABT16501DLR	Active	Production	SSOP (DL) | 56	1000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT16501
SN74ABT16501DLR.B	Active	Production	SSOP (DL) | 56	1000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT16501
SN74ABT16501DLRG4	Active	Production	SSOP (DL) | 56	1000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT16501
SN74ABT16501DLRG4.B	Active	Production	SSOP (DL) | 56	1000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT16501

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ABT16501DGGR	TSSOP	DGG	56	2000	330.0	24.4	8.9	14.7	1.4	12.0	24.0	Q1
SN74ABT16501DLR	SSOP	DL	56	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1
SN74ABT16501DLRG4	SSOP	DL	56	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1

PACKAGE MATERIALS INFORMATION

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ABT16501DGGR	TSSOP	DGG	56	2000	356.0	356.0	45.0
SN74ABT16501DLR	SSOP	DL	56	1000	356.0	356.0	53.0
SN74ABT16501DLRG4	SSOP	DL	56	1000	356.0	356.0	53.0

PACKAGE MATERIALS INFORMATION

TUBE

T - Tube height

L - Tube length

W - Tube width

B - Alignment groove width

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74ABT16501DL	DL	SSOP	56	20	473.7	14.24	5110	7.87
SN74ABT16501DL.B	DL	SSOP	56	20	473.7	14.24	5110	7.87

DL (R−PDSO−G56) PLASTIC SMALL−OUTLINE PACKAGE

0.025 (0,635)

0.0135 (0,343)
0.008 (0,203)

⊕ 0.005 (0,13) Ⓜ

56   29

0.420 (10,67)
0.395 (10,03)

0.299 (7,59)
0.291 (7,39)

0.010 (0,25)
0.005 (0,13)

Gage Plane

0.010 (0,25)

0°−8°

0.040 (1,02)
0.020 (0,51)

1   28

0.730 (18,54)
0.720 (18,29)

0.110 (2,79) MAX

0.008 (0,20) MIN

Seating Plane

△ 0.004 (0,10)

4040048−4/F 05/13
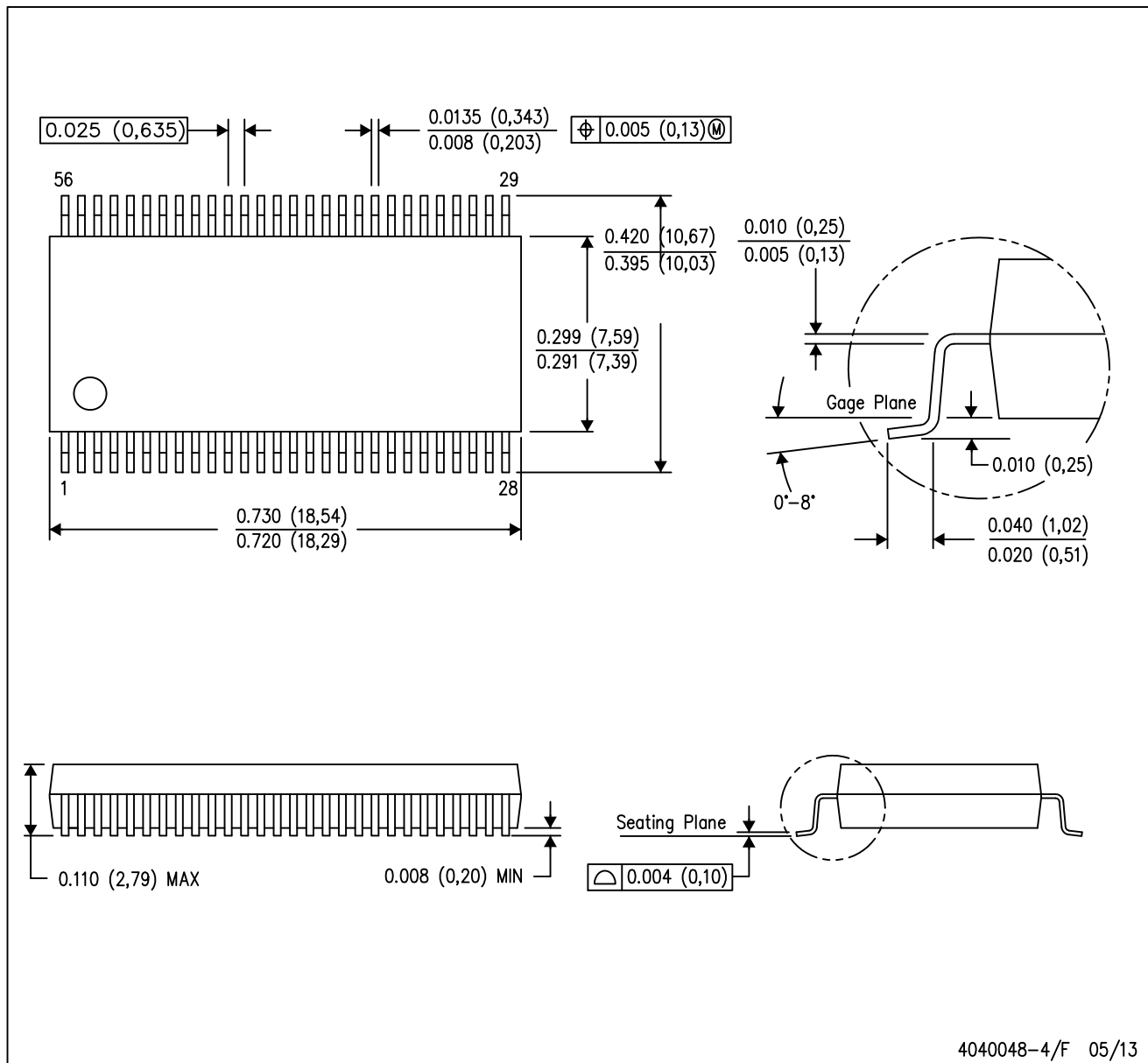
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MO−118

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8.3
7.9 TYP

A

PIN 1 ID
AREA

1

54X 0.5

56

14.1
13.9
NOTE 3

2X
13.5

28

29

B

6.2
6.0

56X 0.27
0.17

⊕ 0.08 Ⓜ C AⓈ BⓈ

C

SEATING PLANE

△ 0.1 C

1.2 MAX

(0.15) TYP

SEE DETAIL A

0.25

GAGE PLANE

0° - 8°

0.75
0.50

0.15
0.05

DETAIL A
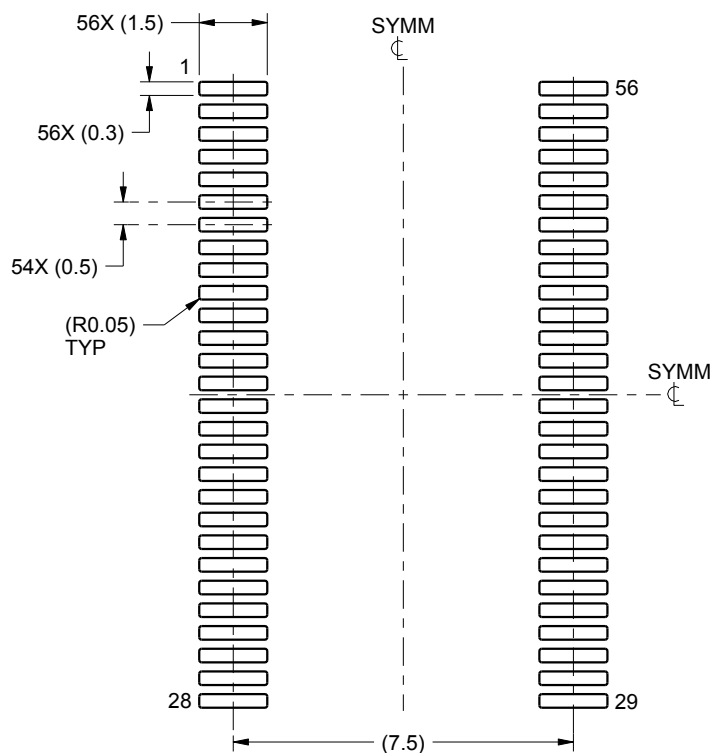TYPICAL
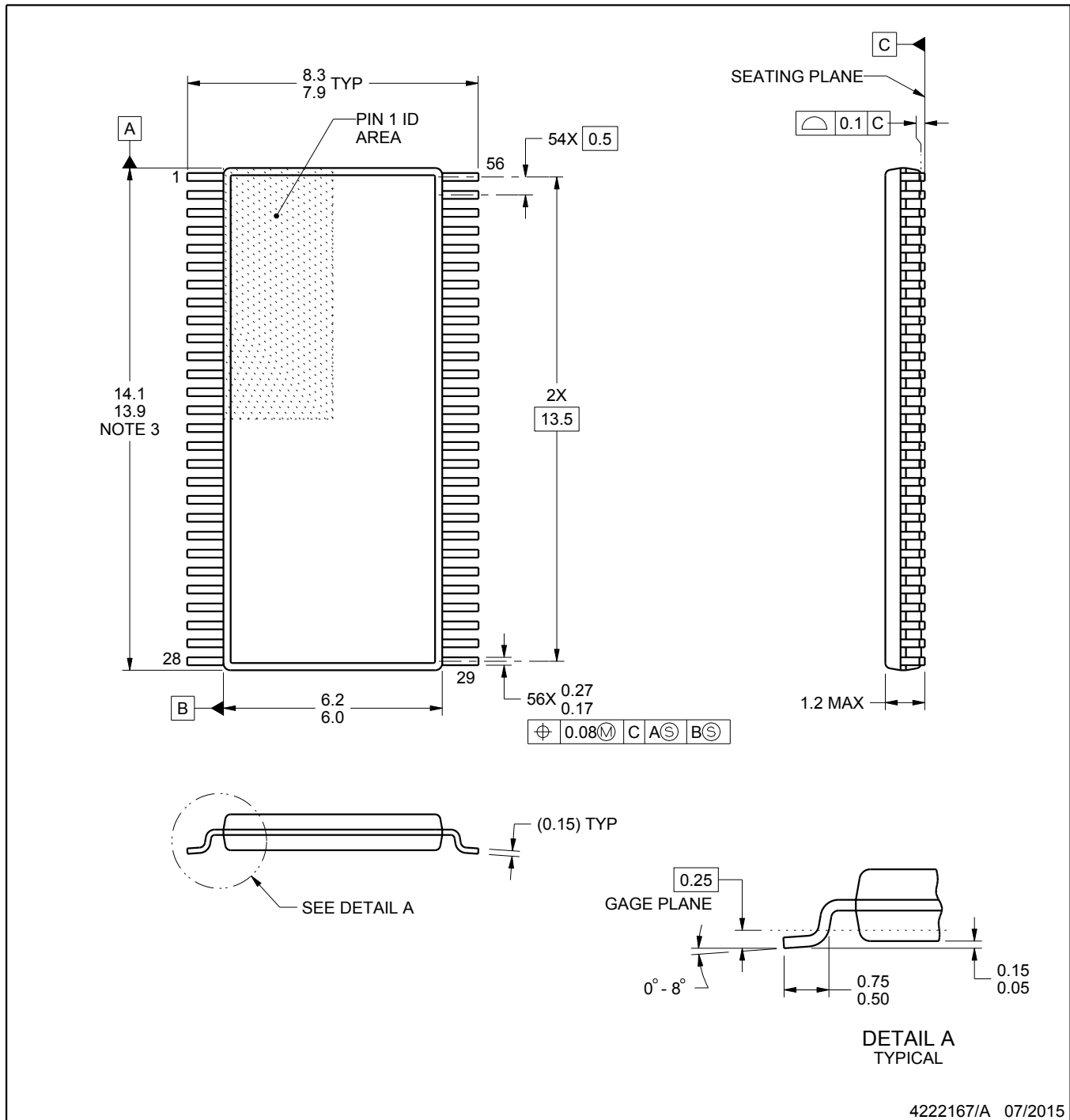
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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
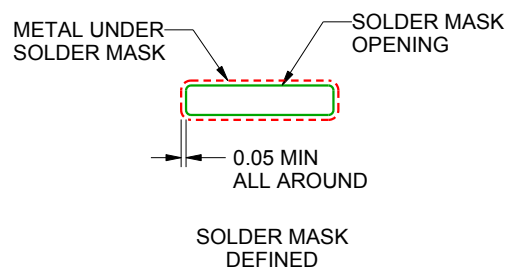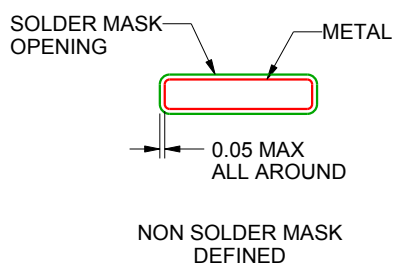4. Reference JEDEC registration MO-153.

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56X (1.5)

1

SYMM

56

56X (0.3)

54X (0.5)

(R0.05)
TYP

SYMM

28

29

(7.5)

LAND PATTERN EXAMPLE
SCALE:6X

SOLDER MASK
OPENING

METAL

0.05 MAX
ALL AROUND

NON SOLDER MASK
DEFINED

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

0.05 MIN
ALL AROUND

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

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NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

DGG0056A

TSSOP - 1.2 mm max height

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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