

1A LOW DROPOUT POSITIVE FIXED 1.8V REGULATOR

PRELIMINARY DATA SHEET

FEATURES

- Guaranteed < 1.3V Dropout at Full Load Current
- Fast Transient Response
- 1% Voltage Reference Initial Accuracy
- Built-In Thermal Shutdown
- Available in SOT-223, D-Pak, Ultra Thin-Pak and 8-Pin SOIC Surface-Mount Packages

APPLICATIONS

- Low Voltage IC Supply Applications
- DSP Core Voltage

DESCRIPTION

The IRU1010-18 is a low dropout three-terminal fixed output regulator with minimum of 1A output current capability. This product is specifically designed to provide well regulated supply for low voltage IC applications as well as generating clock supply for PC applications. The IRU1010-18 is guaranteed to have <1.3V dropout at full load current making it ideal to provide well regulated with 3.8V input supply. The IRU1010-18 is specifically designed to be stable with low cost aluminum capacitors while maintaining stability with low ESR tantalum caps.

TYPICAL APPLICATION

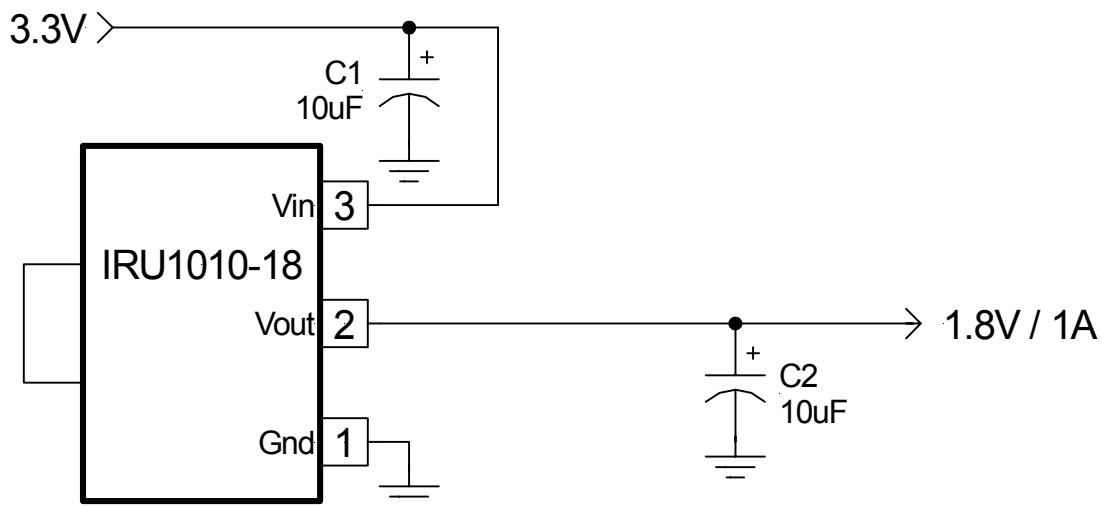


Figure 1 - Typical set-up of the IRU1010-18 in a 3.3V to 1.8V regulator application

PACKAGE ORDER INFORMATION

Tj (°C)	2-PIN PLASTIC TO-252 (D-Pak)	3-PIN PLASTIC SOT-223 (Y)	2-PIN PLASTIC Ultra Thin-Pak (P)	8-PIN PLASTIC SOIC (S)
0 To 125	IRU1010-18CD	IRU1010-18CY	IRU1010-18CP	IRU1010-18CS

IRU1010-18

ABSOLUTE MAXIMUM RATINGS

Input Voltage (Vin)	7V
Power Dissipation	Internally Limited
Storage Temperature Range	-65°C To 150°C
Operating Junction Temperature Range	0°C To 125°C

PACKAGE INFORMATION

2-PIN PLASTIC TO-252 (D-Pak)	3-PIN PLASTIC SO-223 (Y)	2-PIN ULTRA THIN-PAK (P)	8-PIN PLASTIC SOIC (S)
<p>FRONT VIEW</p> <p>Tab is Vout</p> <p>1 Gnd</p> <p>3 Vin</p> <p>$\theta_{JA}=70^{\circ}\text{C/W}$ for 0.5" Sq pad</p>	<p>TOP VIEW</p> <p>Tab is Vout</p> <p>1 Gnd</p> <p>2 Vout</p> <p>3 Vin</p> <p>$\theta_{JA}=90^{\circ}\text{C/W}$ for 0.4" Sq pad</p>	<p>FRONT VIEW</p> <p>Tab is Vout</p> <p>1 Gnd</p> <p>3 Vin</p> <p>$\theta_{JA}=70^{\circ}\text{C/W}$ for 0.5" Sq pad</p>	<p>TOP VIEW</p> <p>1 Vin</p> <p>2 NC</p> <p>3 NC</p> <p>4 Gnd</p> <p>5 Vout</p> <p>6 Vout</p> <p>7 Vout</p> <p>8 Vout</p> <p>$\theta_{JA}=55^{\circ}\text{C/W}$ for 1" Sq pad</p>

ELECTRICAL SPECIFICATIONS

Unless otherwise specified, these specifications apply over $C_{in}=1\mu\text{F}$, $V_{in}=5\text{V}$, $C_{out}=10\mu\text{F}$ and $T_j=0$ to 125°C . Typical values refer to $T_j=25^{\circ}\text{C}$.

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS
Output Voltage	V_o	$I_o=10\text{mA}$, $T_j=25^{\circ}\text{C}$ $I_o=10\text{mA}$	1.782 1.764	1.800 1.800	1.818 1.836	V
Line Regulation		$I_o=10\text{mA}$, $4.75\text{V}<V_{in}<7\text{V}$			7	mV
Load Regulation (Note 1)		$10\text{mA}<I_o<1\text{A}$			17	mV
Dropout Voltage (Note 2)		$I_o=1\text{A}$			1.3	V
Current Limit		$dV_o=100\text{mV}$	1.1			A
Thermal Regulation		30ms Pulse, $I_o=1\text{A}$		0.01		%/W
Ripple Rejection		$f=120\text{Hz}$, $C_o=25\mu\text{F}$ Tantalum, $I_o=0.5\text{A}$		70		dB
Temperature Stability		$I_o=10\text{mA}$		0.5		%
Long Term Stability		$T_j=125^{\circ}\text{C}$, 1000Hrs		0.3		%
RMS Output Noise		$T_j=25^{\circ}\text{C}$, $10\text{Hz}<f<10\text{KHz}$		0.003		% V_o

Note 1: Low duty cycle pulse testing with Kelvin connections is required in order to maintain accurate data.

Note 2: Dropout voltage is defined as the minimum differential voltage between V_{in} and V_{out} required to maintain regulation at V_{out} . It is measured when the output voltage drops 1% below its nominal value.

PIN DESCRIPTIONS

PIN#	PIN SYMBOL	PIN DESCRIPTION
1	Gnd	Ground pin. This pin must be connected to ground plane using a low inductance short connection.
2	Vout	The output of the regulator. This pin is also connected to the tab of the package. An output capacitor must be connected to this pin to insure stability of the regulator.
3	Vin	Input pin of the regulator. Typically a large storage capacitor is connected from this pin to ground to insure that the input voltage does not sag below the minimum dropout voltage during the load transient response. This pin must always be 1.3V higher than Vout in order for the device to regulate properly.

BLOCK DIAGRAM

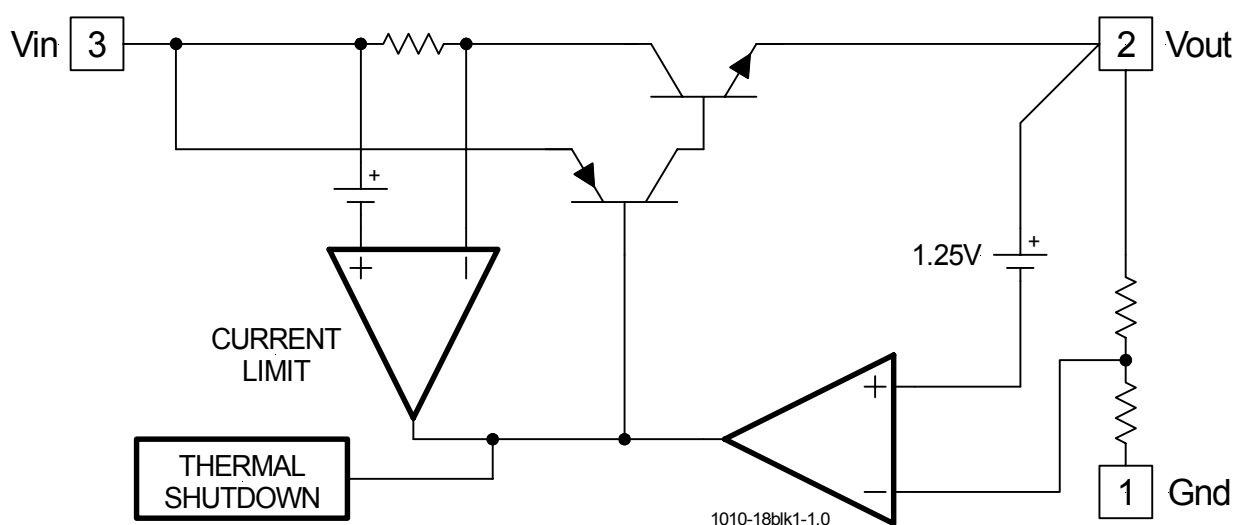


Figure 2 - Simplified block diagram of the IRU1010-18

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IR WORLD HEADQUARTERS : 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
TAC Fax: (310) 252-7903

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