

- 5- $\Omega$  Switch Connection Between Two Ports
- TTL-Compatible Input Levels
- Outputs Are Precharged by Bias Voltage to Minimize Signal Distortion During Live Insertion
- Package Options Include Plastic Shrink Small-Outline (DB, DBQ), Small-Outline (DW), and Thin Shrink Small-Outline (PW) Packages

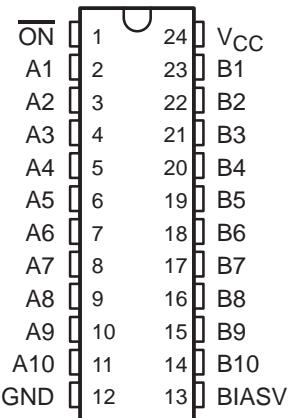
### description

The SN74CBT6800A provides ten bits of high-speed TTL-compatible bus switching. The low on-state resistance of the switch allows bidirectional connections to be made while adding near-zero propagation delay. The device also precharges the B port to a user-selectable bias voltage (BIASV) through the equivalent of a 10-k $\Omega$  resistor to minimize live-insertion noise.

The SN74CBT6800A is organized as one 10-bit switch with a single enable ( $\overline{ON}$ ) input. When  $\overline{ON}$  is low, the switch is on and port A is connected to port B. When  $\overline{ON}$  is high, the switch between port A and port B is open. When  $\overline{ON}$  is high or  $V_{CC}$  is 0 V, B port is precharged to BIASV through the equivalent of a 10-k $\Omega$  resistor.

The SN74CBT6800A is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

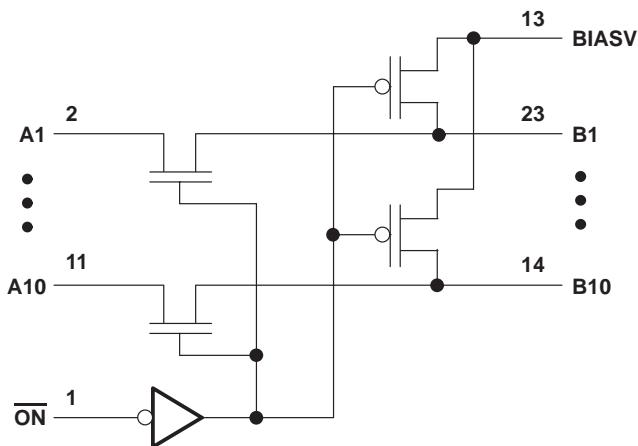
DB, DBQ, DW, OR PW PACKAGE  
(TOP VIEW)



FUNCTION TABLE

INPUT $\overline{ON}$	FUNCTION
L	A port = B port
H	A port = Z B port = BIASV

### logic diagram (positive logic)



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**SN74CBT6800A  
10-BIT FET BUS SWITCH  
WITH PRECHARGED OUTPUTS**

SCDS005L – MARCH 1993 – REVISED JULY 1999

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
2. The package thermal impedance is calculated in accordance with JEDEC 51.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage	4	5.5	V
$BIASV$	Supply voltage	1.3	$V_{CC}$	V
$V_{IH}$	High-level control input voltage	2		V
$V_{IL}$	Low-level control input voltage		0.8	V
$T_A$	Operating free-air temperature	-40	85	°C

NOTE 3: All unused control inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP‡	MAX	UNIT
V <sub>IK</sub>		V <sub>CC</sub> = 4.5 V, I <sub>I</sub> = -18 mA					-1.2	V
I <sub>I</sub>		V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 5.5 V or GND					±5	µA
I <sub>O</sub>		V <sub>CC</sub> = 4.5 V, BIASV = 2.4 V, V <sub>O</sub> = 0			0.25			mA
I <sub>CC</sub>		V <sub>CC</sub> = 5.5 V, I <sub>O</sub> = 0, V <sub>I</sub> = V <sub>CC</sub> or GND					50	µA
ΔI <sub>CC</sub> §	Control inputs	V <sub>CC</sub> = 5.5 V, One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND					2.5	mA
C <sub>i</sub>	Control inputs	V <sub>I</sub> = 3 V or 0					3.5	pF
C <sub>o</sub> (OFF)		V <sub>O</sub> = 3 V or 0, Switch off					4.5	pF
r <sub>on</sub> ¶		V <sub>CC</sub> = 4 V, TYP at V <sub>CC</sub> = 4 V	V <sub>I</sub> = 2.4 V, I <sub>I</sub> = 15 mA		11		20	Ω
		V <sub>CC</sub> = 4.5 V	V <sub>I</sub> = 0	I <sub>I</sub> = 64 mA	3		7	
				I <sub>I</sub> = 30 mA	3		7	
			V <sub>I</sub> = 2.4 V,	I <sub>I</sub> = 15 mA	6		15	

<sup>†</sup>All typical values are at  $V_{CC} = 5$  V (unless otherwise noted),  $T_A = 25^\circ\text{C}$ .

§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

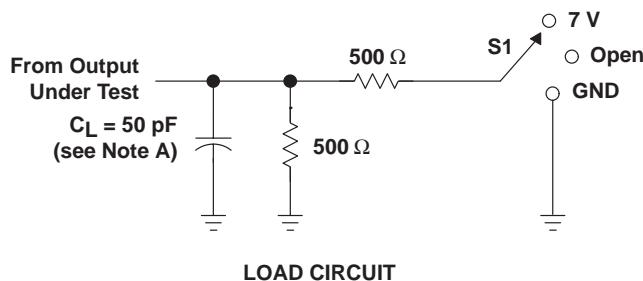
¶ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range,  $C_L = 50 \text{ pF}$  (unless otherwise noted) (see Figure 1)

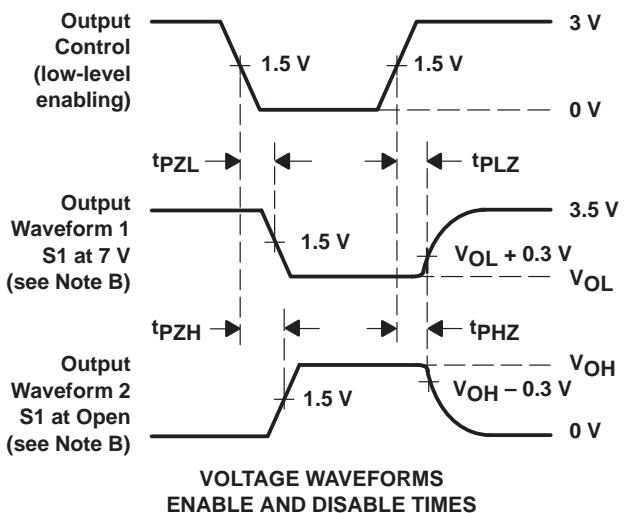
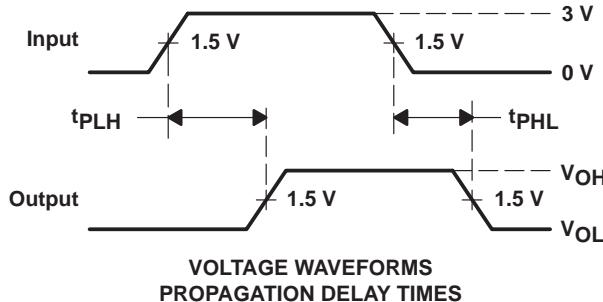
PARAMETER	TEST CONDITIONS	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4 \text{ V}$		$V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$		UNIT
				MIN	MAX	MIN	MAX	
$t_{pd}^{\dagger}$		A or B	B or A	0.35		0.25		ns
$t_{PZH}$	BIASV = GND	ON	A or B	6		2	5.1	ns
$t_{PZL}$	BIASV = 3 V			6		2	5.6	
$t_{PHZ}$	BIASV = GND	ON	A or B	5.5		1	5	ns
$t_{PLZ}$	BIASV = 3 V			5.5		2	5.9	

<sup>†</sup> The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

### PARAMETER MEASUREMENT INFORMATION



TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	7 V
$t_{PHZ}/t_{PZH}$	Open



NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .  
 D. The outputs are measured one at a time with one transition per measurement.  
 E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .  
 F.  $t_{PLZ}$  and  $t_{PZH}$  are the same as  $t_{en}$ .  
 G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 1. Load Circuit and Voltage Waveforms

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