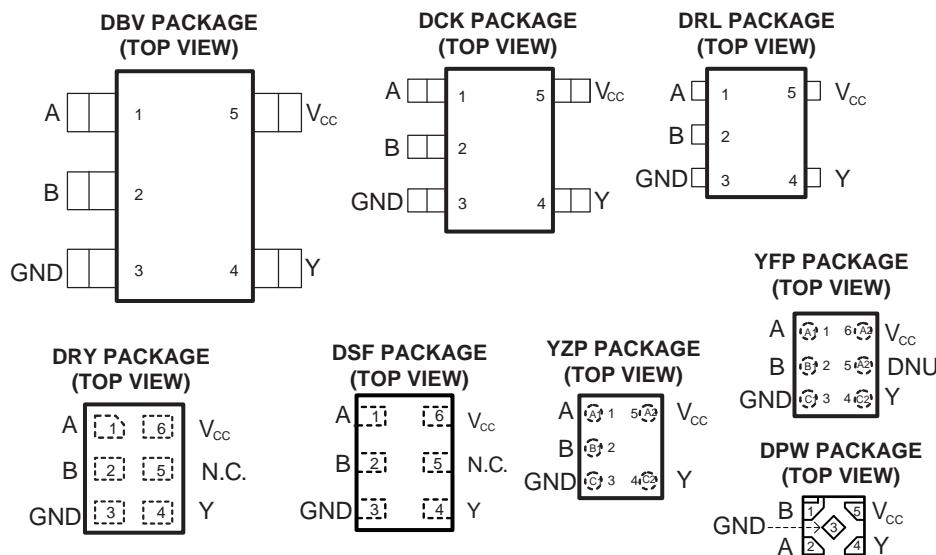


LOW-POWER SINGLE 2-INPUT POSITIVE-AND GATE

Check for Samples: [SN74AUP1G08](#)

FEATURES

- Available in the Texas Instruments NanoStar™ Package
- Low Static-Power Consumption: $I_{cc} = 0.9 \mu A$ Max
- Low Dynamic-Power Consumption: $C_{pd} = 4.3 \text{ pF}$ Typ at 3.3 V
- Low Input Capacitance: $C_i = 1.5 \text{ pF}$ Typ
- Low Noise: Overshoot and Undershoot <10% of V_{cc}
- I_{off} Supports Partial-Power-Down Mode Operation
- Schmitt-Trigger Action Allows Slow Input Transition and Better Switching Noise Immunity at the Input ($V_{hys} = 250 \text{ mV}$ Typ at 3.3 V)
- Wide Operating V_{cc} Range of 0.8 V to 3.6 V
- Optimized for 3.3-V Operation
- 3.6-V I/O Tolerant to Support Mixed-Mode Signal Operation
- $t_{pd} = 4.3 \text{ ns}$ Max at 3.3 V
- Suitable for Point-to-Point Applications
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
 - 2000-V Human-Body Model (A114-B, Class II)
 - 1000-V Charged-Device Model (C101)



DNU – Do not use

N.C. – No internal connection

See mechanical drawings for dimensions.

DESCRIPTION/ORDERING INFORMATION

The AUP family is TI's premier solution to the industry's low-power needs in battery-powered portable applications. This family ensures a very low static- and dynamic-power consumption across the entire V_{cc} range of 0.8 V to 3.6 V, resulting in increased battery life (see [Figure 1](#)). This product also maintains excellent signal integrity (see the very low undershoot and overshoot characteristics shown in [Figure 2](#)).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

NanoStar is a trademark of Texas Instruments.

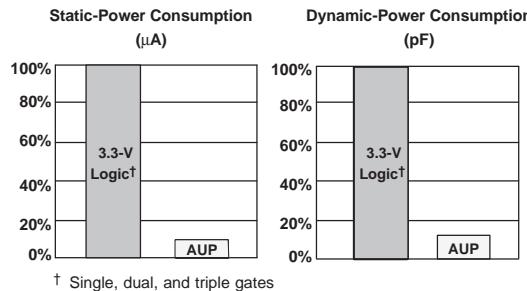


Figure 1. AUP – The Lowest-Power Family

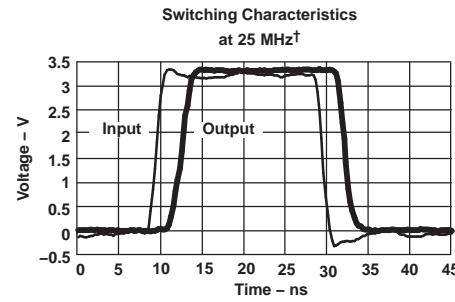


Figure 2. Excellent Signal Integrity

This single 2-input positive-AND gate performs the Boolean function $Y = A \bullet B$ or $Y = \overline{\overline{A}} + \overline{\overline{B}}$ in positive logic.

NanoStar™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

ORDERING INFORMATION⁽¹⁾

T_A	PACKAGE ⁽²⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING ⁽³⁾
-40°C to 85°C	NanoStar™ – W CSP (DSBGA) 0.23-mm Large Bump – YFP (Pb-free)	Reel of 3000	SN74AUP1G08YFPR	_ _ _ HE _
	NanoStar™ – W CSP (DSBGA) 0.23-mm Large Bump – YZP (Pb-free)	Reel of 3000	SN74AUP1G08YZPR	_ _ _ HE _
	QFN – DRY	Reel of 5000	SN74AUP1G08DRYR	HE
	uQFN – DSF	Reel of 5000	SN74AUP1G08DSFR	HE
			SN74AUP1G08DSF2 ⁽⁴⁾	
	uQFN – DPW	Reel of 5000	SN74AUP1G08DPWR	HE
	SOT (SOT-23) – DBV	Reel of 3000	SN74AUP1G08DBVR	H08 _
	SOT (SC-70) – DCK	Reel of 3000	SN74AUP1G08DCKR	HE _
	SOT (SOT-553) – DRL	Reel of 4000	SN74AUP1G08DRLR	

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

(3) DBV/DCK/DRL: The actual top-side marking has one additional character that designates the wafer fab/assembly site.

YFP/YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the wafer fab/assembly site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, • = Pb-free).

(4) Pin 1 orientation at quadrant 3 in Tape.

FUNCTION TABLE

INPUTS		OUTPUT Y
A	B	
L	L	L
L	H	L
H	L	L
H	H	H

LOGIC DIAGRAM (POSITIVE LOGIC)



ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply voltage range	-0.5	4.6	V
V_I	Input voltage range ⁽²⁾	-0.5	4.6	V
V_O	Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾	-0.5	4.6	V
V_O	Output voltage range in the high or low state ⁽²⁾	-0.5	$V_{CC} + 0.5$	V
I_{IK}	Input clamp current	$V_I < 0$	-50	mA
I_{OK}	Output clamp current	$V_O < 0$	-50	mA
I_O	Continuous output current		± 20	mA
	Continuous current through V_{CC} or GND		± 50	mA
θ_{JA}	Package thermal impedance ⁽³⁾	DBV package	206	°C/W
		DCK package	252	
		DRL package	142	
		DRY package	234	
		DSF package	300	
		YFP package	132	
		YZP package	132	
T_{stg}	Storage temperature range	-65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

(3) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS⁽¹⁾

		MIN	MAX	UNIT
V_{CC}	Supply voltage	0.8	3.6	V
V_{IH}	High-level input voltage	$V_{CC} = 0.8\text{ V}$	V_{CC}	V
		$V_{CC} = 1.1\text{ V to }1.95\text{ V}$	$0.65 \times V_{CC}$	
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	1.6	
		$V_{CC} = 3\text{ V to }3.6\text{ V}$	2	
V_{IL}	Low-level input voltage	$V_{CC} = 0.8\text{ V}$	0	V
		$V_{CC} = 1.1\text{ V to }1.95\text{ V}$	$0.35 \times V_{CC}$	
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	0.7	
		$V_{CC} = 3\text{ V to }3.6\text{ V}$	0.9	
V_I	Input voltage	0	3.6	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 0.8\text{ V}$	-20	μA
		$V_{CC} = 1.1\text{ V}$	-1.1	
		$V_{CC} = 1.4\text{ V}$	-1.7	
		$V_{CC} = 1.65$	-1.9	
		$V_{CC} = 2.3\text{ V}$	-3.1	
		$V_{CC} = 3\text{ V}$	-4	
I_{OL}	Low-level output current	$V_{CC} = 0.8\text{ V}$	20	μA
		$V_{CC} = 1.1\text{ V}$	1.1	
		$V_{CC} = 1.4\text{ V}$	1.7	
		$V_{CC} = 1.65\text{ V}$	1.9	
		$V_{CC} = 2.3\text{ V}$	3.1	
		$V_{CC} = 3\text{ V}$	4	
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 0.8\text{ V to }3.6\text{ V}$	200	ns/V
T_A	Operating free-air temperature		-40	85 °C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See the TI application report *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			T _A = -40°C to 85°C		UNIT
			MIN	TYP	MAX	MIN	MAX	
V _{OH}	I _{OH} = -20 µA	0.8 V to 3.6 V	V _{CC} – 0.1			V _{CC} – 0.1		V
	I _{OH} = -1.1 mA	1.1 V	0.75 × V _{CC}			0.7 × V _{CC}		
	I _{OH} = -1.7 mA	1.4 V		1.11			1.03	
	I _{OH} = -1.9 mA	1.65 V		1.32			1.3	
	I _{OH} = -2.3 mA	2.3 V		2.05			1.97	
	I _{OH} = -3.1 mA			1.9			1.85	
	I _{OH} = -2.7 mA	3 V		2.72			2.67	
	I _{OH} = -4 mA			2.6			2.55	
V _{OL}	I _{OL} = 20 µA	0.8 V to 3.6 V			0.1		0.1	V
	I _{OL} = 1.1 mA	1.1 V			0.3 × V _{CC}		0.3 × V _{CC}	
	I _{OL} = 1.7 mA	1.4 V			0.31		0.37	
	I _{OL} = 1.9 mA	1.65 V			0.31		0.35	
	I _{OL} = 2.3 mA	2.3 V			0.31		0.33	
	I _{OL} = 3.1 mA				0.44		0.45	
	I _{OL} = 2.7 mA	3 V			0.31		0.33	
	I _{OL} = 4 mA				0.44		0.45	
I _I	A or B input	V _I = GND to 3.6 V	0 V to 3.6 V		0.1		0.5	µA
I _{off}		V _I or V _O = 0 V to 3.6 V	0 V		0.2		0.6	µA
ΔI _{off}		V _I or V _O = 0 V to 3.6 V	0 V to 0.2 V		0.2		0.6	µA
I _{CC}		V _I = GND or (V _{CC} to 3.6 V), I _O = 0	0.8 V to 3.6 V		0.5		0.9	µA
ΔI _{CC}		V _I = V _{CC} – 0.6 V ⁽¹⁾ , I _O = 0	3.3 V		40		50	µA
C _i		V _I = V _{CC} or GND	0 V		1.5			pF
			3.6 V		1.5			
C _o		V _O = GND	0 V		3			pF

(1) One input at V_{CC} – 0.6 V, other input at V_{CC} or GND.

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, C_L = 5 pF (unless otherwise noted) (see [Figure 3](#) and [Figure 4](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC}	T _A = 25°C			T _A = -40°C to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t _{pd}	A or B	Y	0.8 V		18				ns
			1.2 V ± 0.1 V	2.6	7.3	12.8	2.1	15.6	
			1.5 V ± 0.1 V	1.4	5.2	8.7	0.9	10.3	
			1.8 V ± 0.15 V	1	4.2	6.6	0.5	8.2	
			2.5 V ± 0.2 V	1	3	4.4	0.5	5.5	
			3.3 V ± 0.3 V	1	2.4	3.5	0.5	4.3	

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, $C_L = 10 \text{ pF}$ (unless otherwise noted) (see [Figure 3](#) and [Figure 4](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C} \text{ to } 85^\circ\text{C}$		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A or B	Y	0.8 V		21				ns
			$1.2 \text{ V} \pm 0.1 \text{ V}$	1.5	8.5	14.7	1	17.2	
			$1.5 \text{ V} \pm 0.1 \text{ V}$	1	6.2	10	0.5	11.3	
			$1.8 \text{ V} \pm 0.15 \text{ V}$	1	5	7.7	0.5	9	
			$2.5 \text{ V} \pm 0.2 \text{ V}$	1	3.6	5.2	0.5	6.1	
			$3.3 \text{ V} \pm 0.3 \text{ V}$	1	2.9	4.2	0.5	4.7	

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, $C_L = 15 \text{ pF}$ (unless otherwise noted) (see [Figure 3](#) and [Figure 4](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C} \text{ to } 85^\circ\text{C}$		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A or B	Y	0.8 V		24				ns
			$1.2 \text{ V} \pm 0.1 \text{ V}$	3.6	9.9	16.3	3.1	19.9	
			$1.5 \text{ V} \pm 0.1 \text{ V}$	2.3	7.2	11.1	1.8	13.2	
			$1.8 \text{ V} \pm 0.15 \text{ V}$	1.6	5.8	8.7	1.1	10.6	
			$2.5 \text{ V} \pm 0.2 \text{ V}$	1	4.3	5.9	0.5	7.3	
			$3.3 \text{ V} \pm 0.3 \text{ V}$	1	3.4	4.8	0.5	5.9	

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, $C_L = 30 \text{ pF}$ (unless otherwise noted) (see [Figure 3](#) and [Figure 4](#))

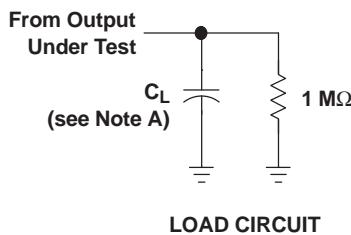
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C} \text{ to } 85^\circ\text{C}$		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A or B	Y	0.8 V		32.8				ns
			$1.2 \text{ V} \pm 0.1 \text{ V}$	4.9	13.1	20.9	4.4	25.5	
			$1.5 \text{ V} \pm 0.1 \text{ V}$	3.4	9.5	14.2	2.9	16.9	
			$1.8 \text{ V} \pm 0.15 \text{ V}$	2.5	7.7	11	2	13.5	
			$2.5 \text{ V} \pm 0.2 \text{ V}$	1.8	5.7	7.6	1.3	9.4	
			$3.3 \text{ V} \pm 0.3 \text{ V}$	1.5	4.7	6.2	1	7.5	

OPERATING CHARACTERISTICS

$T_A = 25^\circ\text{C}$

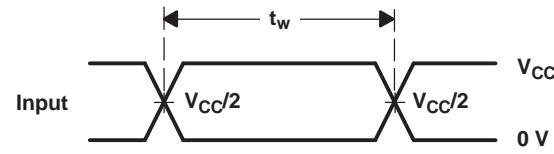
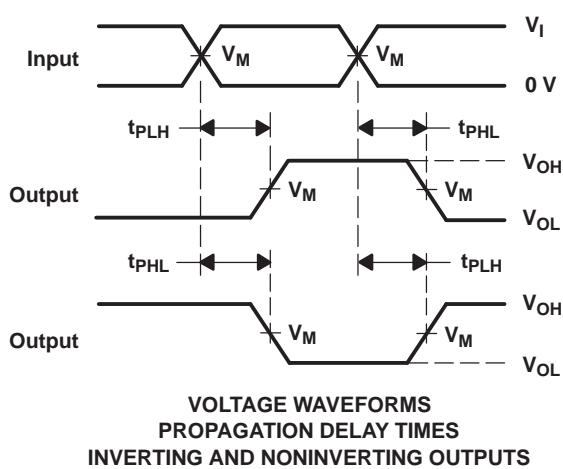
PARAMETER			TEST CONDITIONS			V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance		$f = 10 \text{ MHz}$			0.8 V	4	pF
						$1.2 \text{ V} \pm 0.1 \text{ V}$	4	
						$1.5 \text{ V} \pm 0.1 \text{ V}$	4	
						$1.8 \text{ V} \pm 0.15 \text{ V}$	4	
						$2.5 \text{ V} \pm 0.2 \text{ V}$	4.1	
						$3.3 \text{ V} \pm 0.3 \text{ V}$	4.3	

PARAMETER MEASUREMENT INFORMATION
(Propagation Delays, Setup and Hold Times, and Pulse Duration)

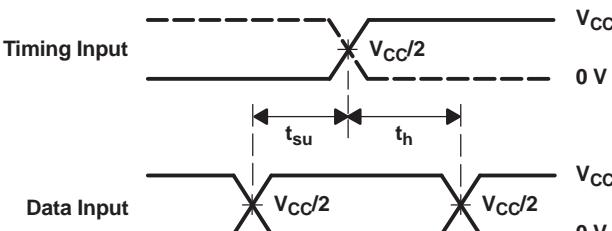


LOAD CIRCUIT

	$V_{CC} = 0.8 \text{ V}$	$V_{CC} = 1.2 \text{ V} \pm 0.1 \text{ V}$	$V_{CC} = 1.5 \text{ V} \pm 0.1 \text{ V}$	$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$	$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$
C_L	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF
V_M	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$
V_I	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}



**VOLTAGE WAVEFORMS
PULSE DURATION**



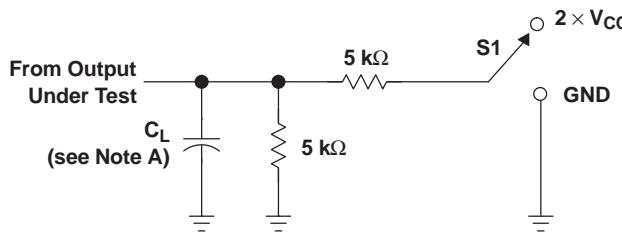
**VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES**

NOTES:

- C_L includes probe and jig capacitance.
- All input pulses are supplied by generators having the following characteristics: PRR $\leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, slew rate $\geq 1 \text{ V/ns}$.
- The outputs are measured one at a time, with one transition per measurement.
- t_{PLH} and t_{PHL} are the same as t_{pd} .
- All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuit and Voltage Waveforms

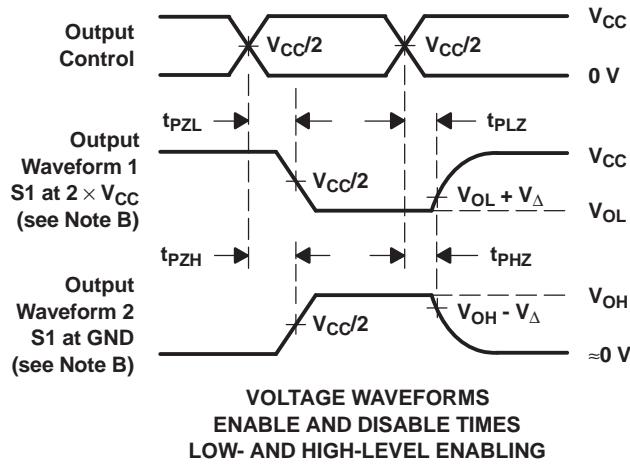
PARAMETER MEASUREMENT INFORMATION (Enable and Disable Times)



TEST	S1
t_{PLZ}/t_{PZL} t_{PHZ}/t_{PZH}	2 × VCC GND

LOAD CIRCUIT

	$V_{CC} = 0.8 \text{ V}$	$V_{CC} = 1.2 \text{ V} \pm 0.1 \text{ V}$	$V_{CC} = 1.5 \text{ V} \pm 0.1 \text{ V}$	$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$	$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$
C_L	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF
V_M	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$
V_I	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}
V_Δ	0.1 V	0.1 V	0.1 V	0.15 V	0.15 V	0.3 V



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES:

- C_L includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics: PRR $\leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, slew rate $\geq 1 \text{ V/ns}$.
- The outputs are measured one at a time, with one transition per measurement.
- t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- t_{PZL} and t_{PZH} are the same as t_{en} .
- All parameters and waveforms are not applicable to all devices.

Figure 4. Load Circuit and Voltage Waveforms

REVISION HISTORY**Changes from Revision J (May 2010) to Revision K** Page

- Added new orderable package type SN74AUP1G08DSF2. [2](#)

Changes from Revision K (October 2011) to Revision L Page

- Revised document to fix package addendum issue. [1](#)

Changes from Revision L (May 2012) to Revision M Page

- Added DPW package ordering information. [2](#)

Changes from Revision M (September 2012) to Revision N Page

- Changed DPW package pinout [1](#)

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
SN74AUP1G08DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(H08F ~ H08R)	Samples
SN74AUP1G08DBVRE4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(H08F ~ H08R)	Samples
SN74AUP1G08DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(H08F ~ H08R)	Samples
SN74AUP1G08DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	H08R	Samples
SN74AUP1G08DBVTE4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	H08R	Samples
SN74AUP1G08DBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	H08R	Samples
SN74AUP1G08DCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(HE5 ~ HEF ~ HEK ~ HER)	Samples
SN74AUP1G08DCKRE4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(HE5 ~ HEF ~ HEK ~ HER)	Samples
SN74AUP1G08DCKRG4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(HE5 ~ HEF ~ HEK ~ HER)	Samples
SN74AUP1G08DCKT	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(HE5 ~ HER)	Samples
SN74AUP1G08DCKTE4	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(HE5 ~ HER)	Samples
SN74AUP1G08DCKTG4	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(HE5 ~ HER)	Samples
SN74AUP1G08DRLR	ACTIVE	SOT	DRL	5	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(HE7 ~ HER)	Samples
SN74AUP1G08DRLRG4	ACTIVE	SOT	DRL	5	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(HE7 ~ HER)	Samples
SN74AUP1G08DRYR	ACTIVE	SON	DRY	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HE	Samples
SN74AUP1G08DSF2	ACTIVE	SON	DSF	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HE	Samples
SN74AUP1G08DSFR	ACTIVE	SON	DSF	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HE	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
SN74AUP1G08YFPR	ACTIVE	DSBGA	YFP	6	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM		(HE2 ~ HE7 ~ HEN)	Samples
SN74AUP1G08YZPR	ACTIVE	DSBGA	YZP	5	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	(HE7 ~ HEN)	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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OTHER QUALIFIED VERSIONS OF SN74AUP1G08 :

- Automotive: [SN74AUP1G08-Q1](#)

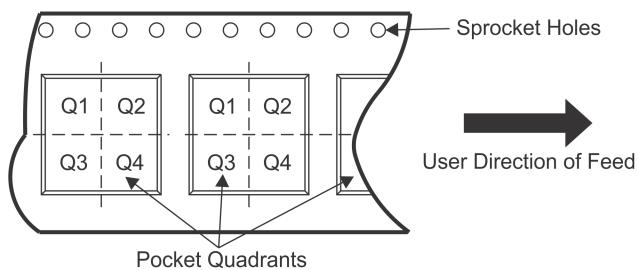
NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AUP1G08DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
SN74AUP1G08DBVT	SOT-23	DBV	5	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74AUP1G08DCKR	SC70	DCK	5	3000	180.0	9.2	2.3	2.55	1.2	4.0	8.0	Q3
SN74AUP1G08DCKR	SC70	DCK	5	3000	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74AUP1G08DCKT	SC70	DCK	5	250	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74AUP1G08DRLR	SOT	DRL	5	4000	180.0	9.5	1.78	1.78	0.69	4.0	8.0	Q3
SN74AUP1G08DRLR	SOT	DRL	5	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3
SN74AUP1G08DRYR	SON	DRY	6	5000	180.0	9.5	1.15	1.6	0.75	4.0	8.0	Q1
SN74AUP1G08DSF2	SON	DSF	6	5000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q3
SN74AUP1G08DSFR	SON	DSF	6	5000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
SN74AUP1G08YFPR	DSBGA	YFP	6	3000	178.0	9.2	0.89	1.29	0.62	4.0	8.0	Q1
SN74AUP1G08YZPR	DSBGA	YZP	5	3000	178.0	9.2	1.02	1.52	0.63	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS

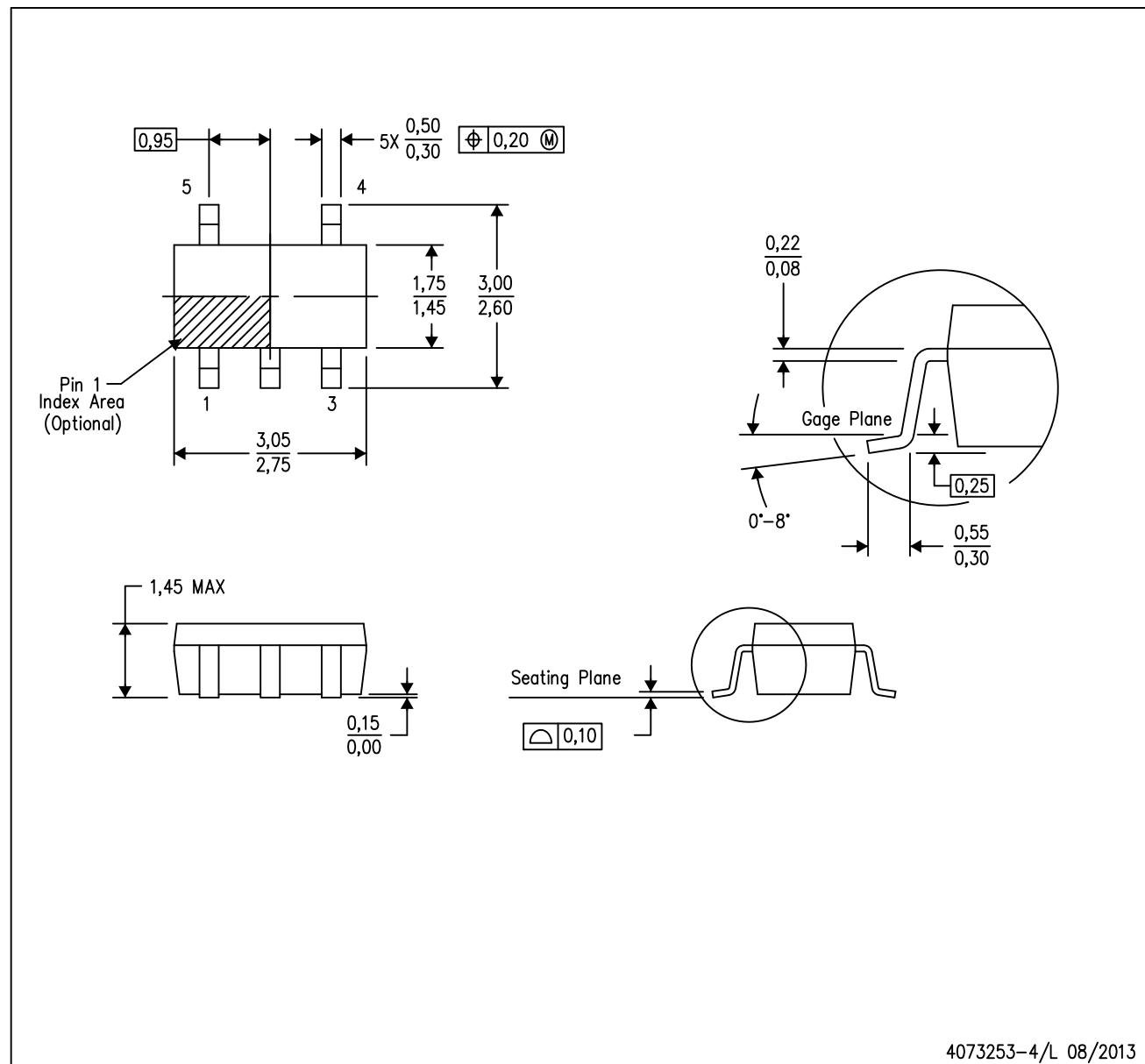

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AUP1G08DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
SN74AUP1G08DBVT	SOT-23	DBV	5	250	202.0	201.0	28.0
SN74AUP1G08DCKR	SC70	DCK	5	3000	205.0	200.0	33.0
SN74AUP1G08DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
SN74AUP1G08DCKT	SC70	DCK	5	250	180.0	180.0	18.0
SN74AUP1G08DRLR	SOT	DRL	5	4000	180.0	180.0	30.0
SN74AUP1G08DRLR	SOT	DRL	5	4000	202.0	201.0	28.0
SN74AUP1G08DRYR	SON	DRY	6	5000	180.0	180.0	30.0
SN74AUP1G08DSF2	SON	DSF	6	5000	180.0	180.0	30.0
SN74AUP1G08DSFR	SON	DSF	6	5000	180.0	180.0	30.0
SN74AUP1G08YFPR	DSBGA	YFP	6	3000	220.0	220.0	35.0
SN74AUP1G08YZPR	DSBGA	YZP	5	3000	220.0	220.0	35.0

MECHANICAL DATA

DBV (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



4073253-4/L 08/2013

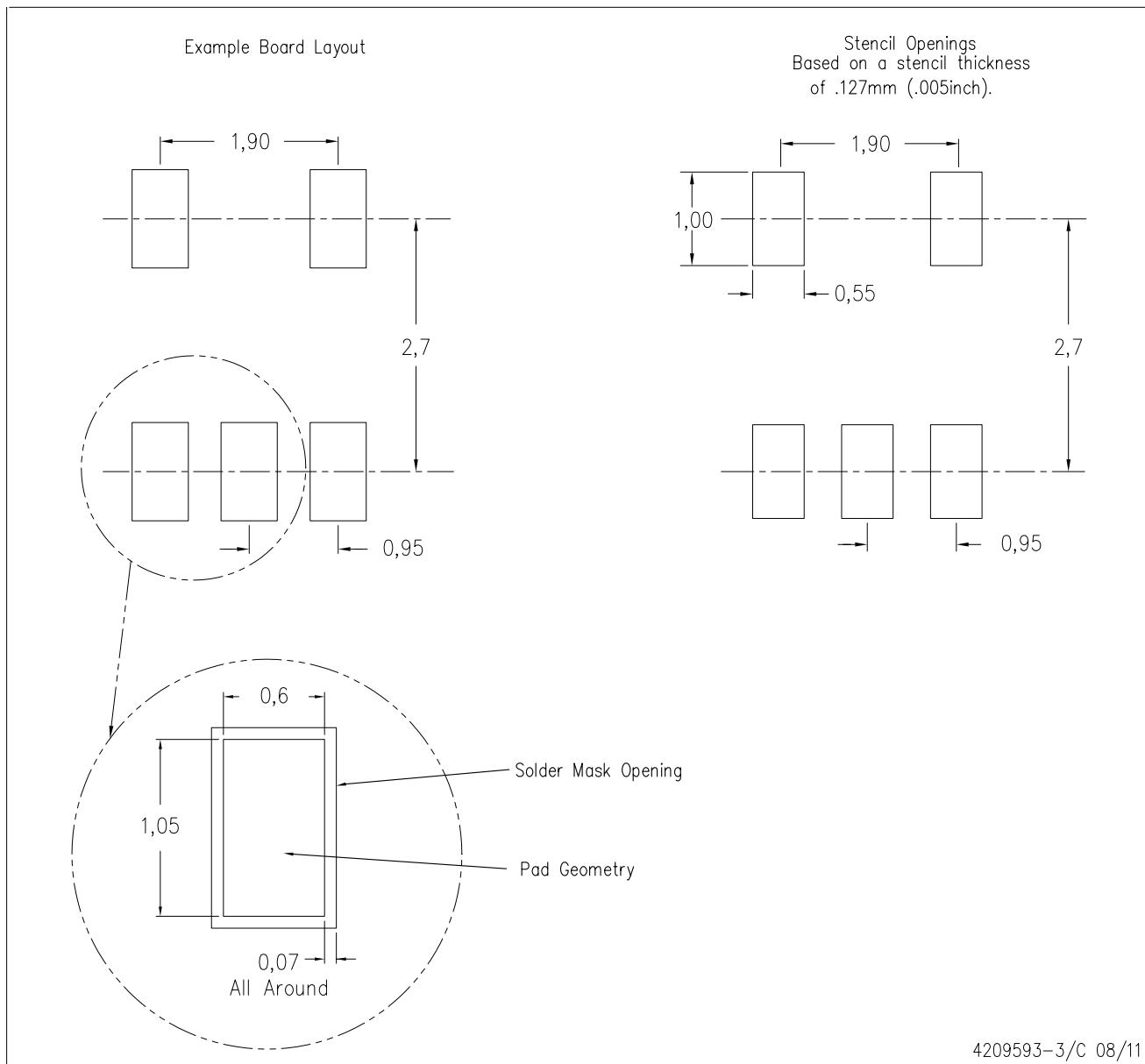
NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. Falls within JEDEC MO-178 Variation AA.

LAND PATTERN DATA

DBV (R-PDSO-G5)

PLASTIC SMALL OUTLINE

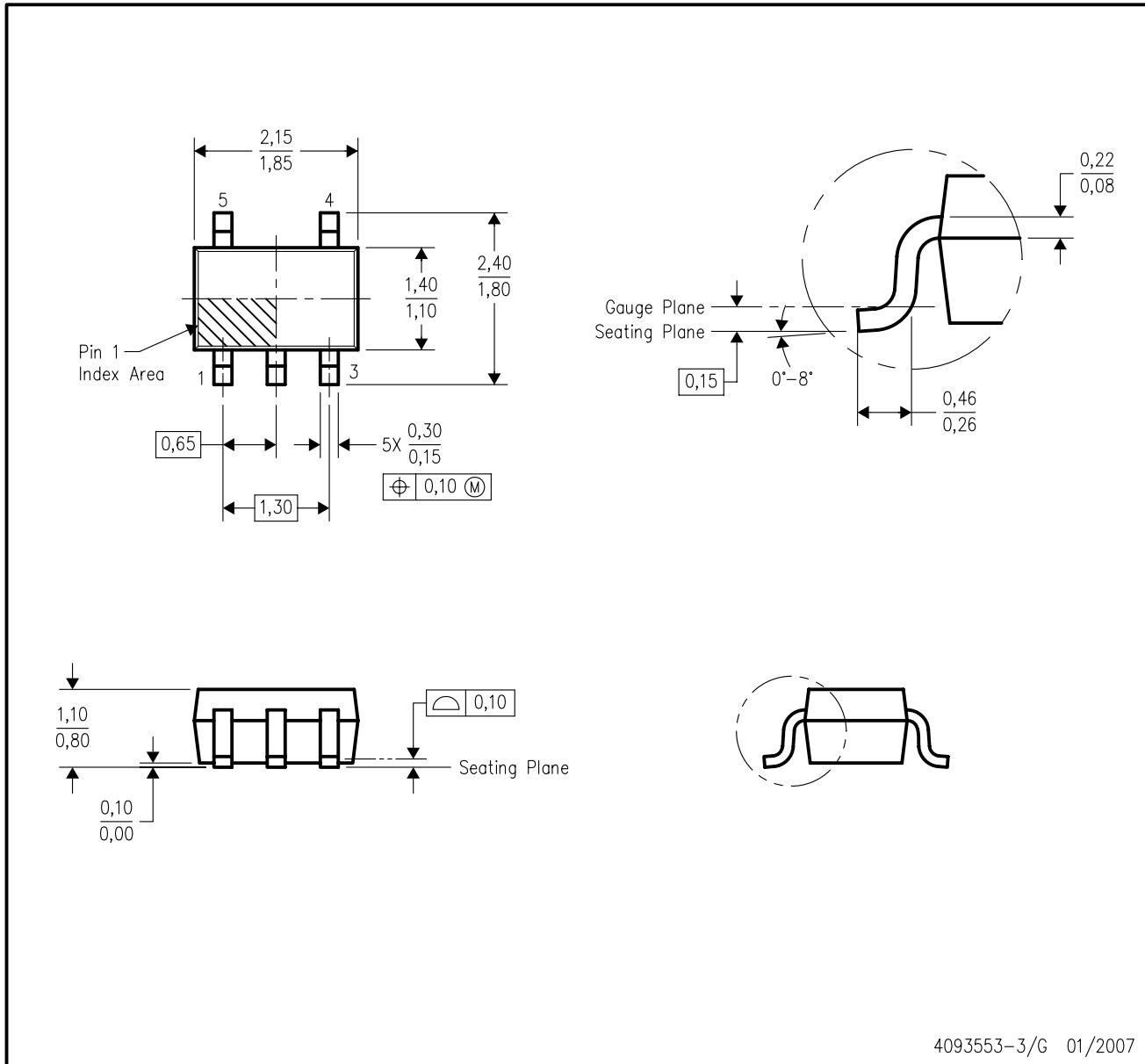


NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. Publication IPC-7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

DCK (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



4093553-3/G 01/2007

NOTES:

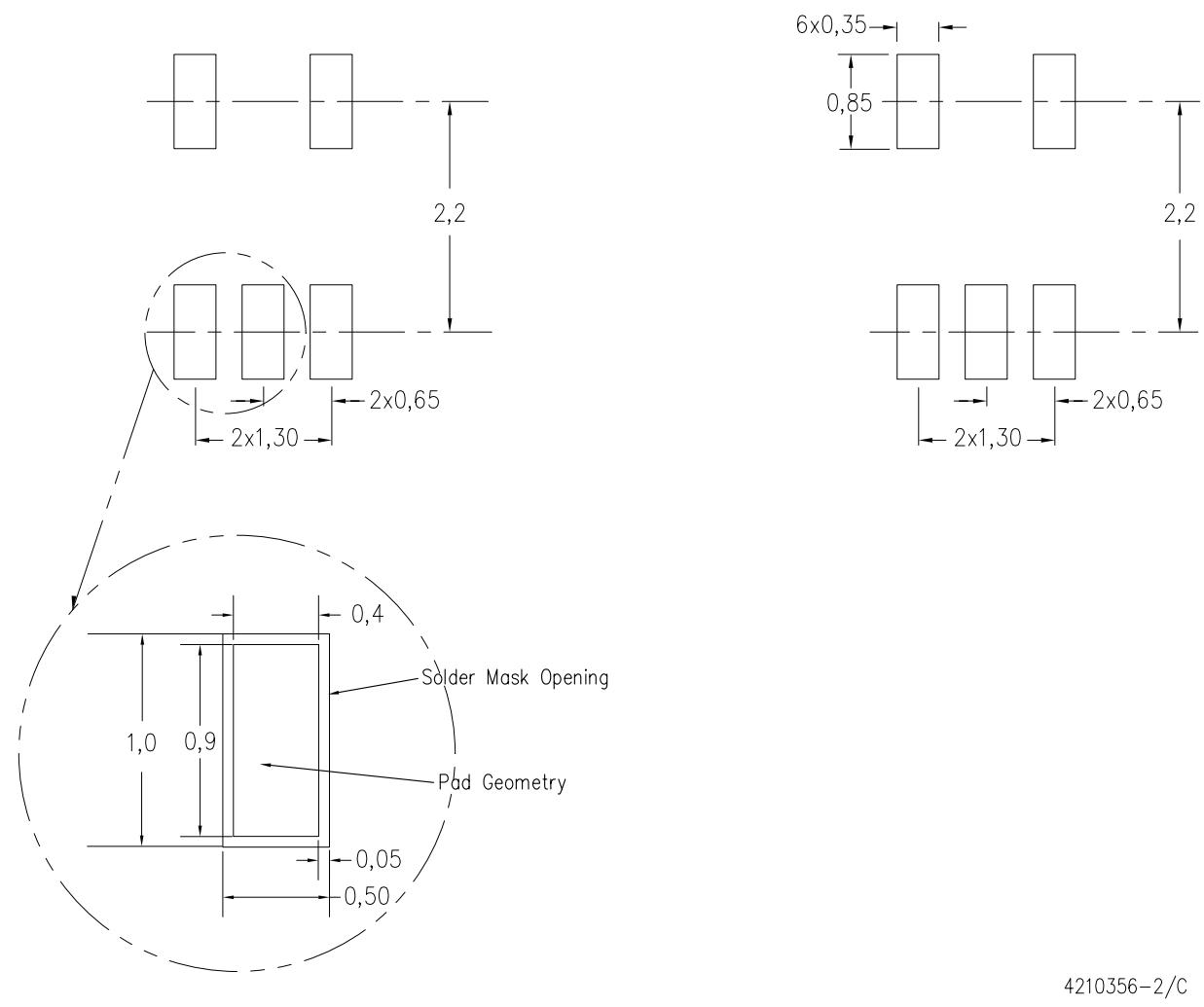
- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- Falls within JEDEC MO-203 variation AA.

DCK (R-PDSO-G5)

PLASTIC SMALL OUTLINE

Example Board Layout

Stencil Openings
Based on a stencil thickness
of .127mm (.005inch).



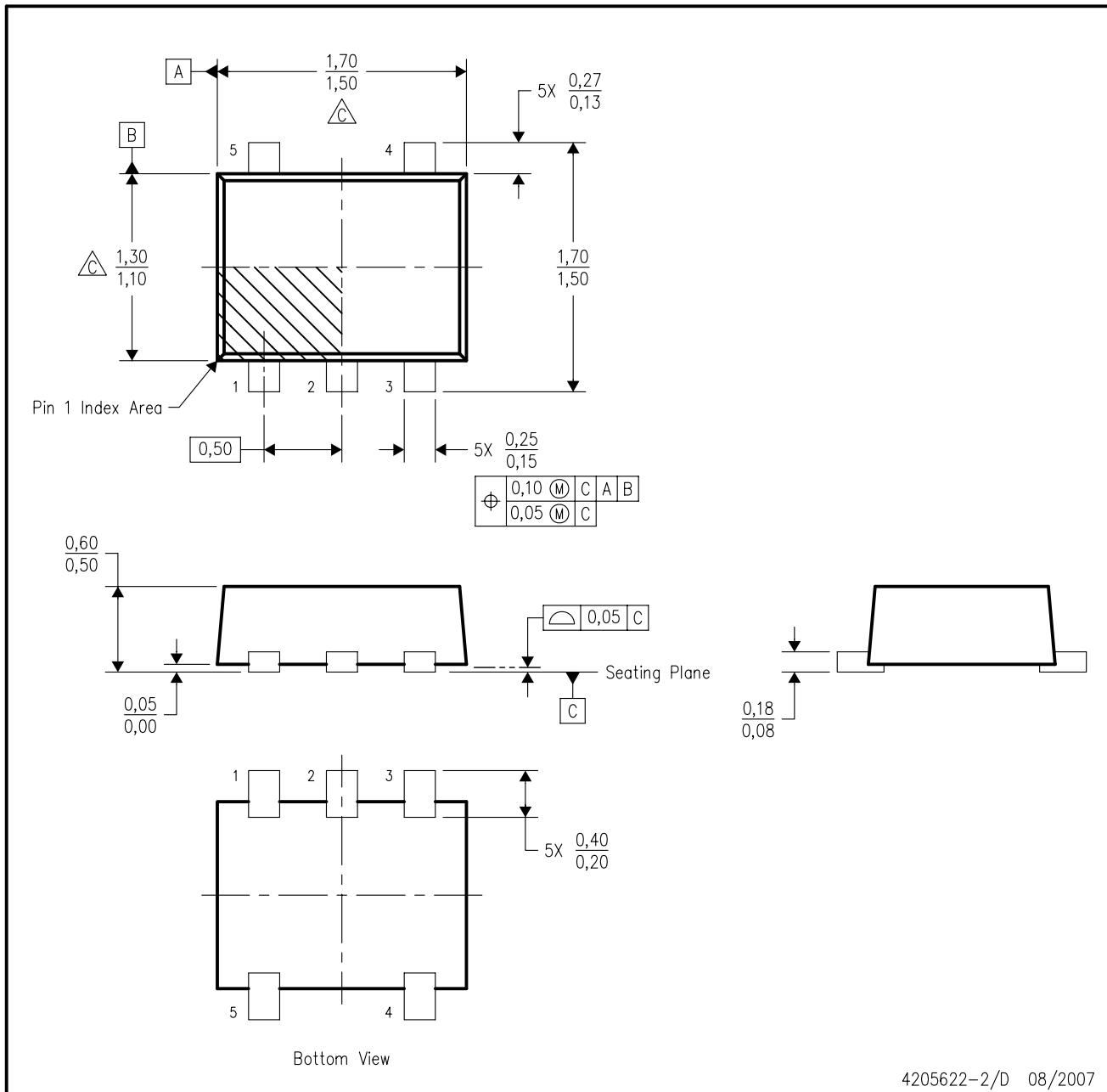
4210356-2/C 07/11

NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- Publication IPC-7351 is recommended for alternate designs.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

DRL (R-PDSO-N5)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

 THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.

 Body dimensions do not include mold flash, interlead flash, protrusions, or gate burrs. Mold flash, interlead flash, protrusions, or gate burrs shall not exceed 0,15 per end or side.

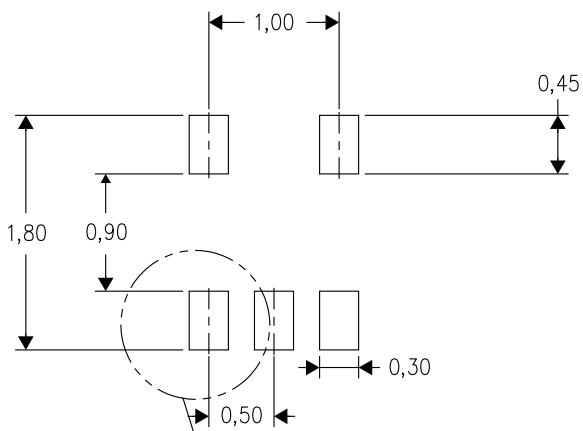
D. JEDEC package registration is pending.

D. JEDEC package registration is pending.

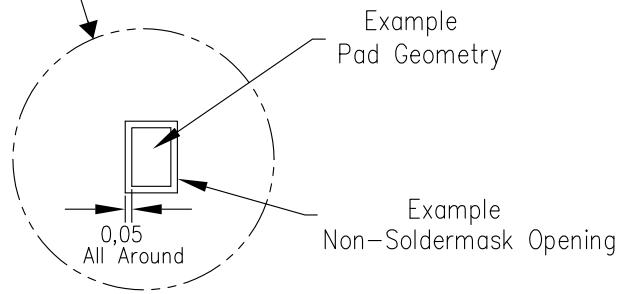
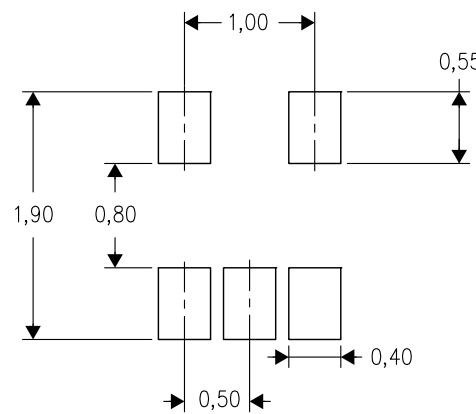
DRL (R-PDSO-N5)

PLASTIC SMALL OUTLINE

Example Board Layout



Example Non-Soldermask Defined Pad

Example Stencil Design
(Note E)

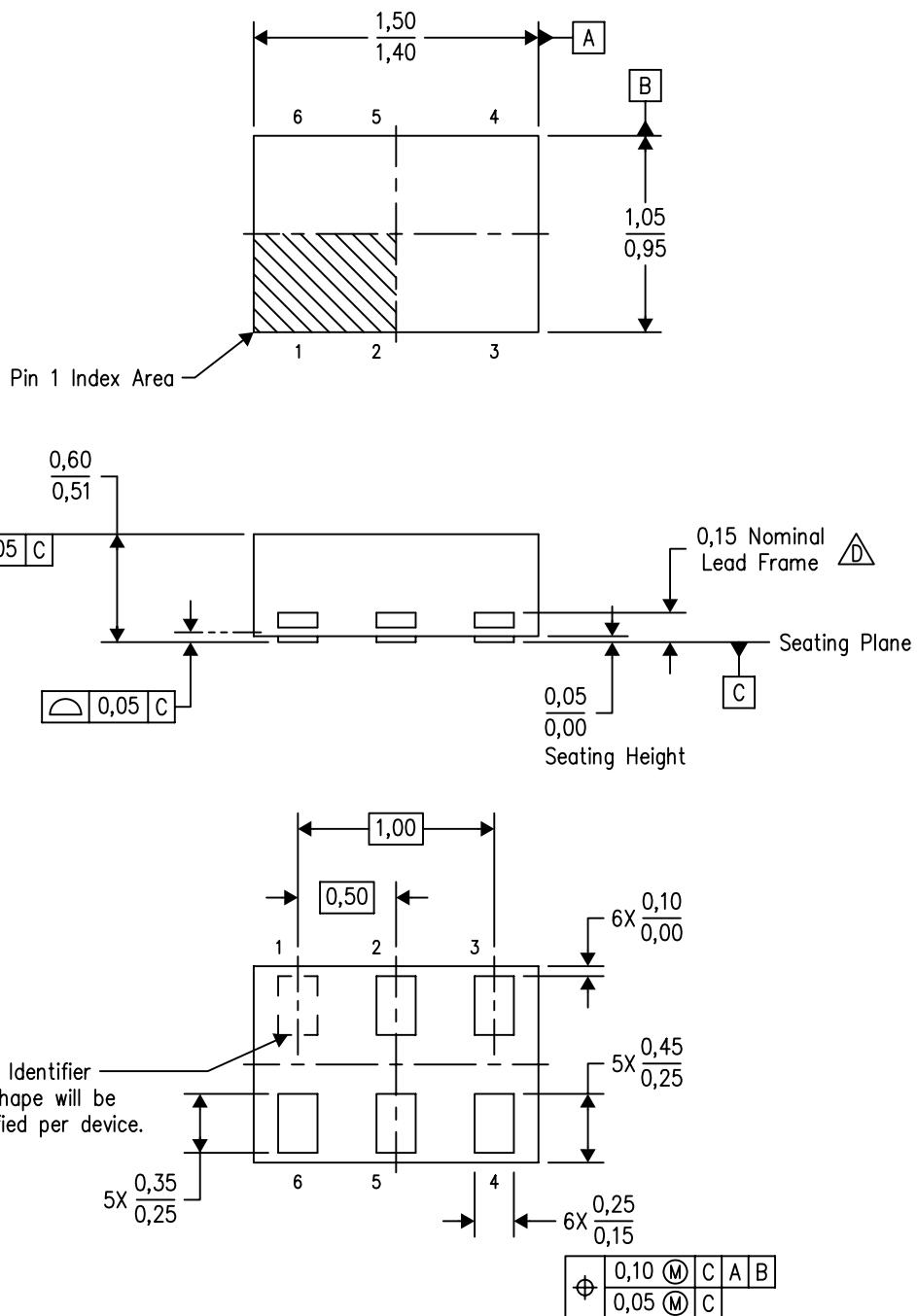
4208207-2/E 06/12

NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Publication IPC-7351 is recommended for alternate designs.
- Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
- Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- Side aperture dimensions over-print land for acceptable area ratio > 0.66 . Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

DRY (R-PUSON-N6)

PLASTIC SMALL OUTLINE NO-LEAD



Bottom View

4207181/F 12/11

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

B. This drawing is subject to change without notice.

C. SON (Small Outline No-Lead) package configuration.

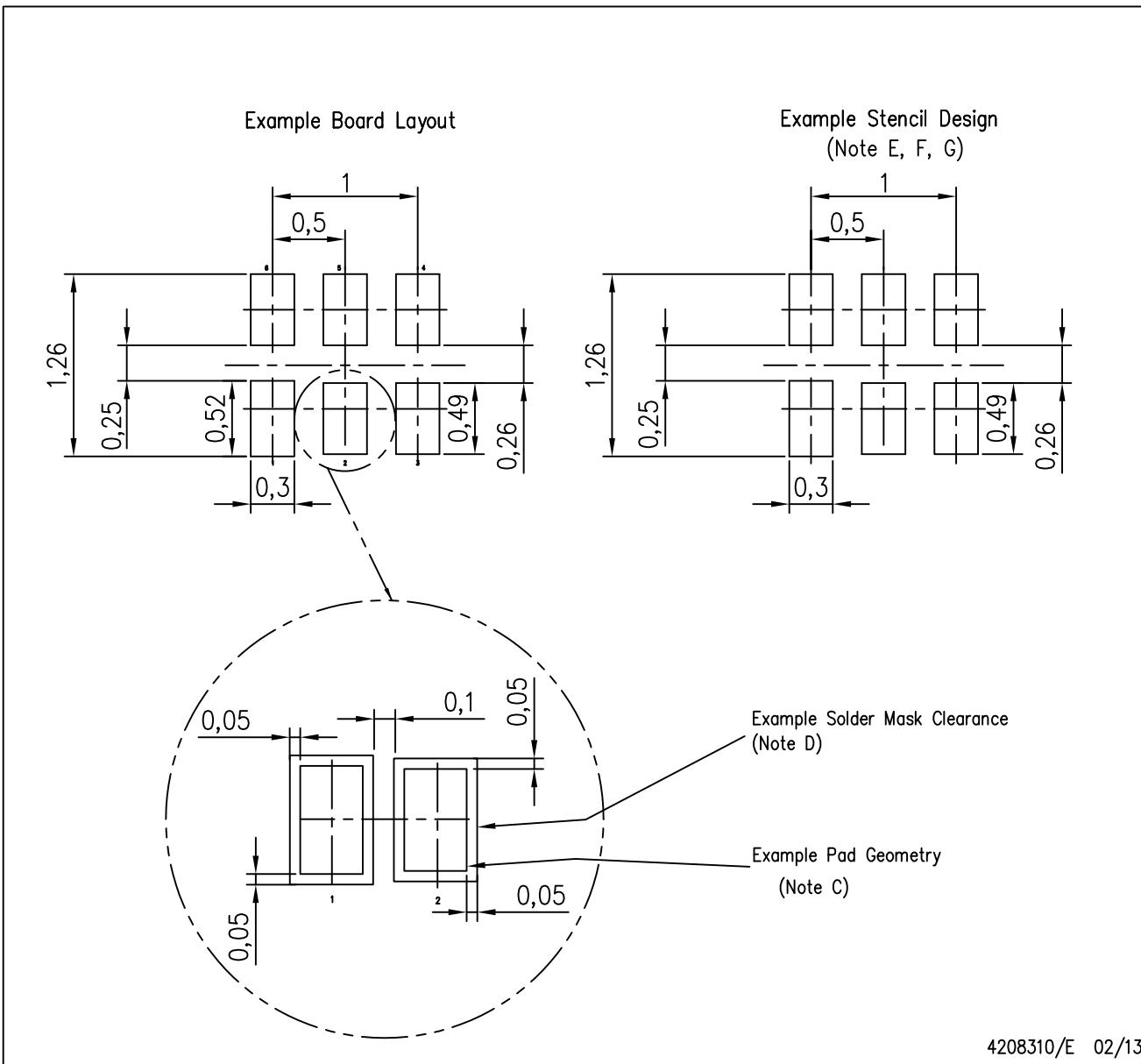
D. The exposed lead frame feature on side of package may or may not be present due to alternative lead frame designs.

E. This package complies to JEDEC MO-287 variation UFAD.

F. See the additional figure in the Product Data Sheet for details regarding the pin 1 identifier shape.

DRY (R-PUSON-N6)

PLASTIC SMALL OUTLINE NO-LEAD



4208310/E 02/13

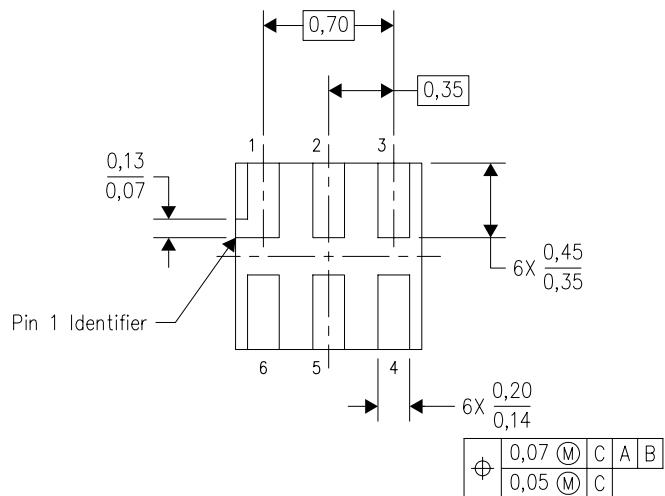
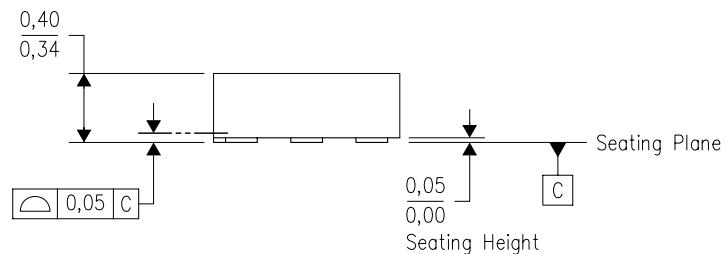
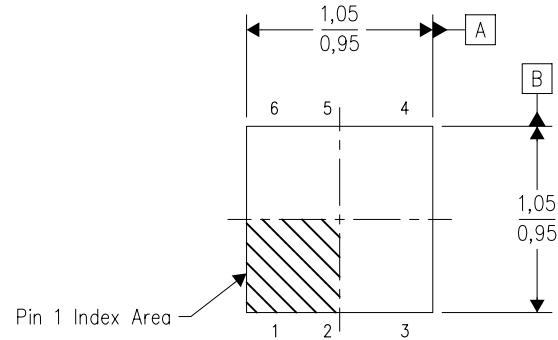
NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
- E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
- F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- G. Side aperture dimensions over-print land for acceptable area ratio > 0.66 . Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

MECHANICAL DATA

DSF (S-PX2SON-N6)

PLASTIC SMALL OUTLINE NO-LEAD



Bottom View

4208186/E 03/11

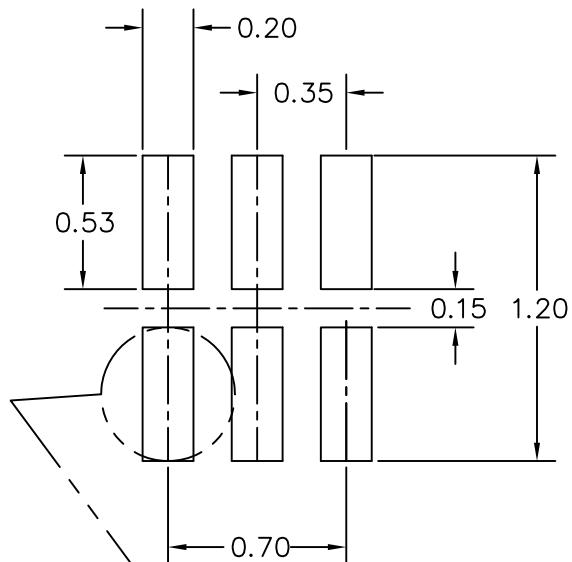
NOTES:

- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
- B. This drawing is subject to change without notice.
- C. SON (Small Outline No-Lead) package configuration.
- D. This package complies to JEDEC MO-287 variation X2AAF.

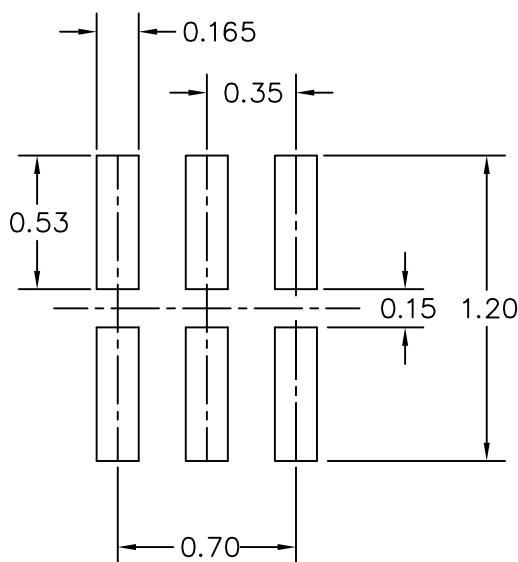
DSF (S-PX2SON-N6)

PLASTIC SMALL OUTLINE NO-LEAD

Land Pattern



Stencil Pattern



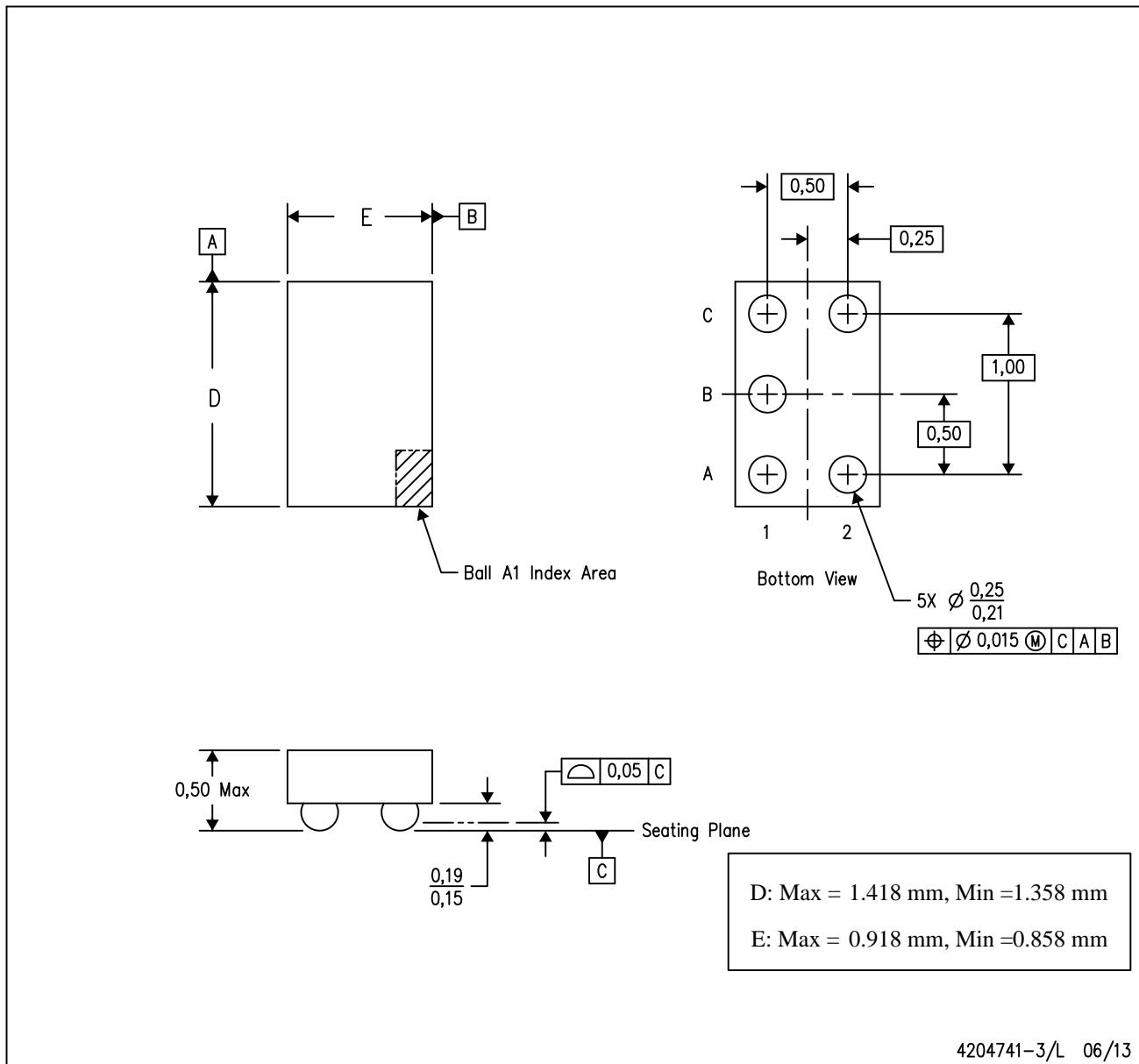
Contact your PCB vendor for
allowable Solder Mask clearance (Notes C, D.)

4210277/D 05/12

NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Publication IPC-7351 is recommended for alternate designs.
 D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
 If 2 mil solder mask is outside PCB vendor capability, it is advised to omit solder mask.
 E. Maximum stencil thickness 0,1016 mm (4 mils). All linear dimensions are in millimeters.
 F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 G. Suggest stencils cut with lasers such as Fiber Laser that produce the greatest positional accuracy.
 H. Component placement force should be minimized to prevent excessive paste block deformation.

YZP (R-XBGA-N5)

DIE-SIZE BALL GRID ARRAY

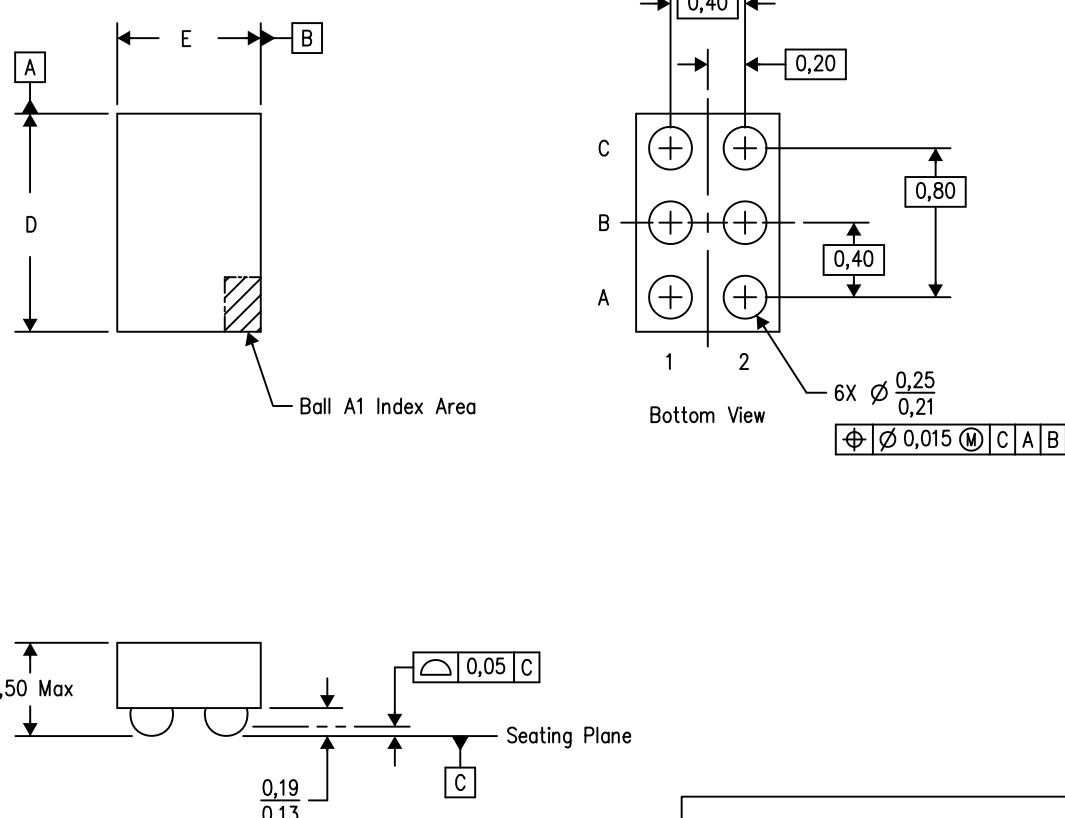


NanoFree is a trademark of Texas Instruments.

MECHANICAL DATA

YFP (R-XBGA-N6)

DIE-SIZE BALL GRID ARRAY



D: Max = 1.19 mm, Min = 1.13 mm
 E: Max = 0.79 mm, Min = 0.73 mm

4206986-3/T 05/13

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 B. This drawing is subject to change without notice.
 C. NanoFree™ package configuration.

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